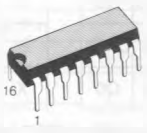
SGS-THOMSON MICROELECTRONICS

M54HC670
M74HC670

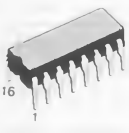
4-WORD X 4-BIT REGISTER FILE (3-STATE)

PRELIMINARY DATA

- HIGH SPEED
  t_{PD} = 21 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS670



B1N
Plastic Package



F1
Ceramic Frit Seal Package

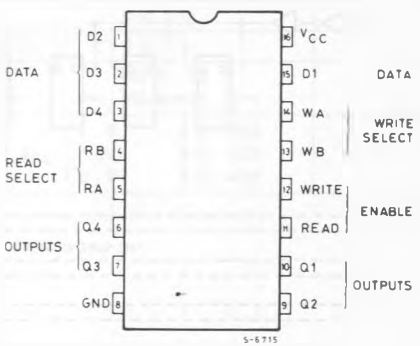
M1
Micro Package

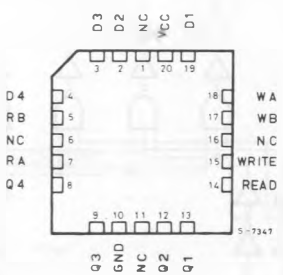
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC670 F1
M74HC670 B1N
M74HC670 F1
M74HC670 C1
M74HC670 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC670 is a high speed CMOS 4 WORD X 4 BIT REGISTER FILE (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC/74HC670 is a 4 x 4 Register File organised as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

WRITE FUNCTION TABLE

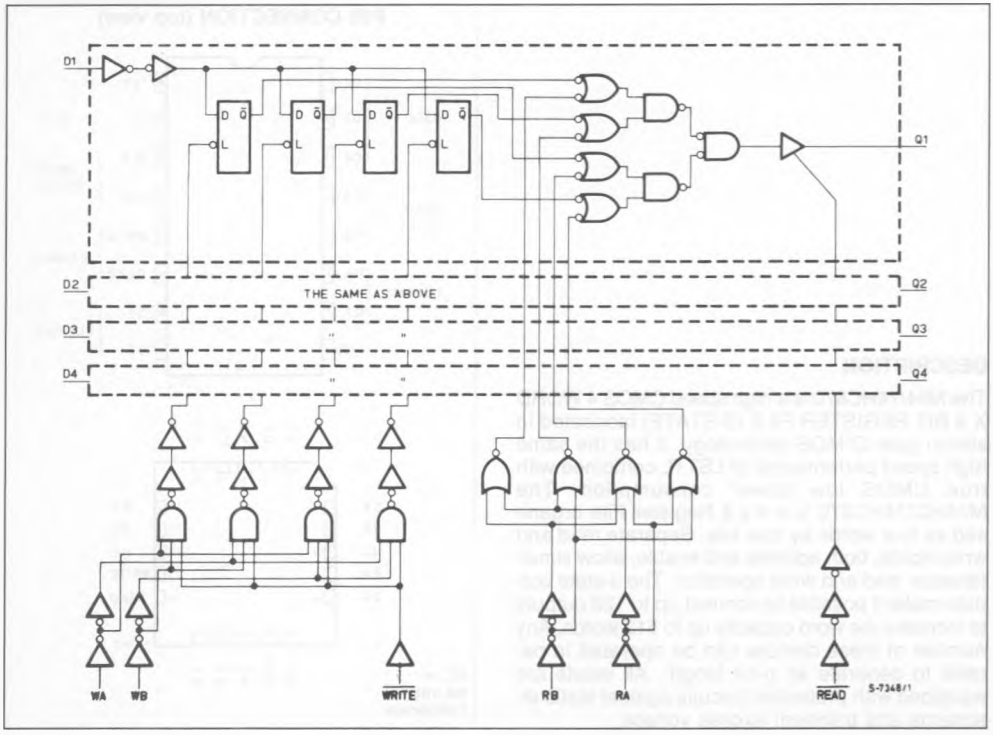
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes: 1 X: DON'T CARE. Z: HIGH IMPEDANCE
2 (Q = D) = THE FOUR SELECT INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3 Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4 W0B1 = THE FIRST BIT OF WORD 0, ETC.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

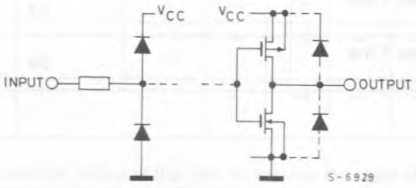
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000		ns
		V_{CC} = 4.5V	0 to 500		
		V_{CC} = 6 V	0 to 400		

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		− 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		− 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5.0	—	± 5.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

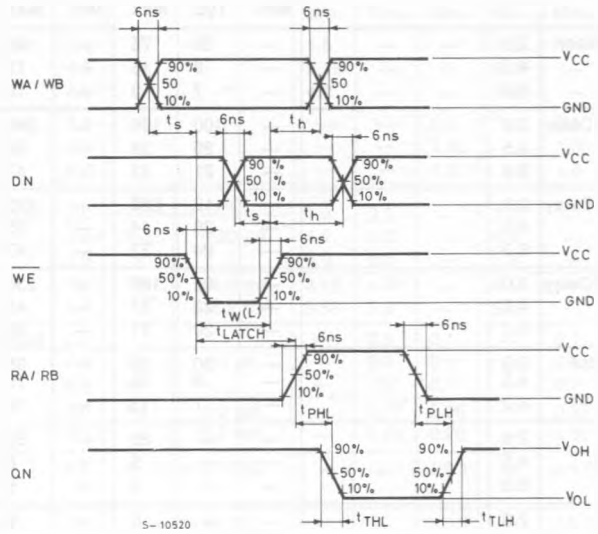
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RA,RB-Qn)		21	34	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{WE}$-Qn)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Dn-Qn)		20	32	ns

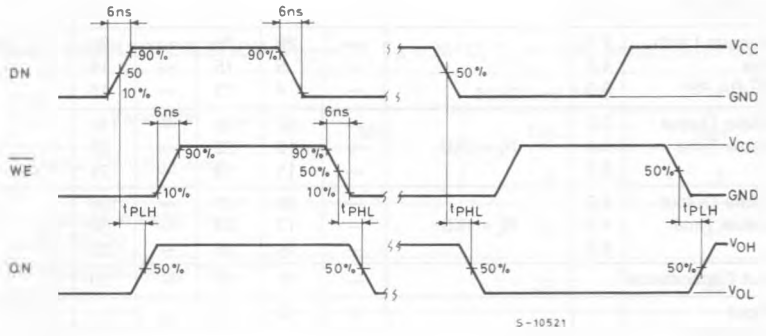
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (RA,RB-Qn)	2.0		—	100	195	—	245		295	ns
		4.5		—	25	39	—	49		59	
		6.0		—	21	33	—	42		50	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{WE}$-Qn)	2.0		—	112	220	—	275		330	ns
		4.5		—	28	44	—	55		66	
		6.0		—	24	37	—	47		36	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn-Qn)	2.0		—	92	185	—	230		280	ns
		4.5		—	23	37	—	46		56	
		6.0		—	20	31	—	39		48	
$t_{W(L)}$	Minimum Pulse Width ($\overline{WE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (Dn-$\overline{WE}$)	2.0		—	—	25	—	30		40	ns
		4.5		—	—	5	—	6		8	
		6.0		—	—	5	—	6		7	
t_s	Minimum Set-up Time (WA-WB-$\overline{WE}$)	2.0		—	—	0	—	0		0	ns
		4.5		—	—	0	—	0		0	
		6.0		—	—	0	—	0		0	
t_h	Minimum Hold Time (Dn-$\overline{WE}$)	2.0		—	15	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time (WA,WB-$\overline{WE}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{latch} (1)	Minimum Latch Time ($\overline{WE}$-RA,RB)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1K\Omega$	—	52	110	—	140	—	165	
		4.5		—	13	22	—	28	—	33	
		6.0		—	11	19	—	24	—	28	
t_{PLZ} t_{PHL}	3-State Output Disable Time	2.0	$R_L = 1K\Omega$	—	68	120	—	150	—	180	
		4.5		—	17	24	—	30	—	36	
		6.0		—	14	20	—	26	—	31	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (2)	Power Dissipation Capacitance			—	44	—	—	—			pF

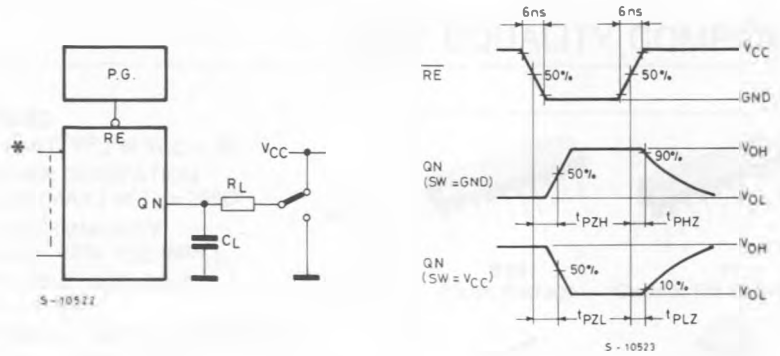
Note:
(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.
(2):C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load. Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



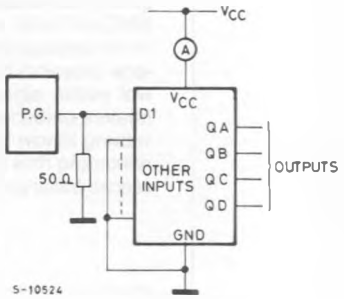


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



*: SUCH A LOGIC LEVEL, SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST