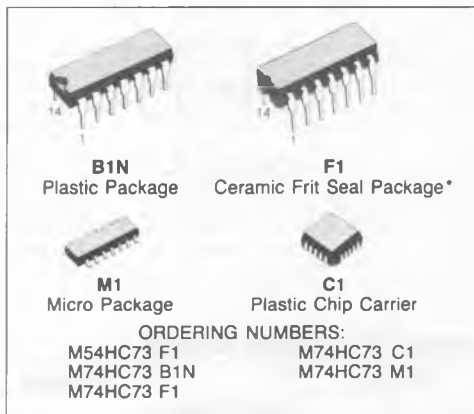


DUAL J-K FLIP FLOP WITH CLEAR

- HIGH SPEED
 $f_{MAX} = 60 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION
 $I_{CC} = 2 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2\text{V to } 6\text{V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS73



DESCRIPTION

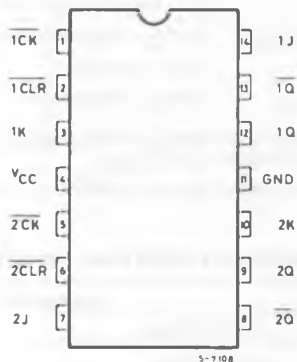
The M54/74HC73 is a high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse (CK). The clear function is accomplished independently of the clock condition when the clear input (CLR) is taken low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
CLR	J	K	Q	\bar{Q}	
L	X	X	L	H	CLEAR
H	L	L	\bar{Q}_n	\bar{Q}_n	NO CHANGE
H	L	H	L	H	—
H	H	L	\bar{Q}_n	\bar{Q}_n	—
H	H	H	\bar{Q}_n	\bar{Q}_n	TOGGLE
H	X	X	\bar{Q}_n	\bar{Q}_n	NO CHANGE

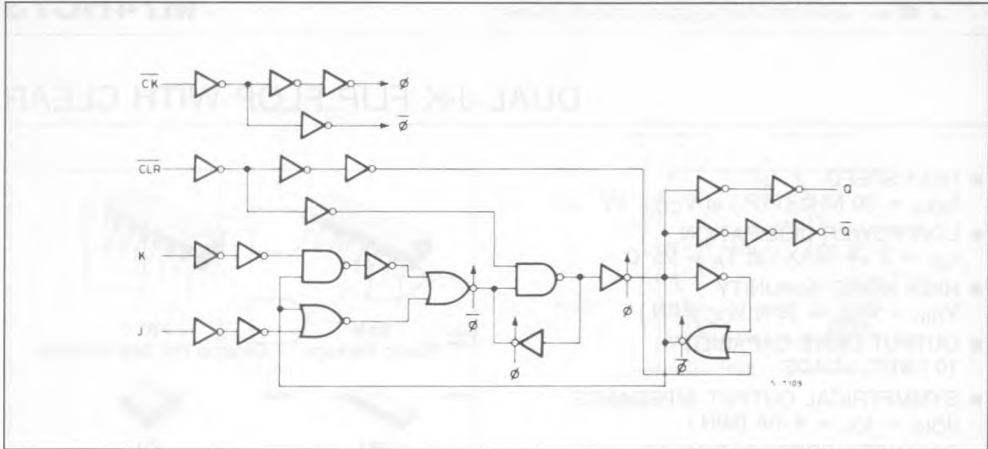
X DON'T CARE

PIN CONNECTIONS (top view)



FOR CHIP CARRIER
 INFORMATION CONTACT SGS-THOMSON

LOGIC DIAGRAM (1/2 of device show)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong 65^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: $65^{\circ}C$ to $85^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit						
V_{CC}	Supply Voltage	2 to 6	V						
V_I	Input Voltage	0 to V_{CC}	V						
V_O	Output Voltage	0 to V_{CC}	V						
T_A	Operating Temperature	74HC Series 54HC Series	$^{\circ}C$						
t_r, t_f	Input Rise and Fall Time	V_{CC} <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>2 V</td> <td>0 to 1000</td> </tr> <tr> <td>4.5V</td> <td>0 to 500</td> </tr> <tr> <td>6 V</td> <td>0 to 400</td> </tr> </table>	2 V	0 to 1000	4.5V	0 to 500	6 V	0 to 400	ns
2 V	0 to 1000								
4.5V	0 to 500								
6 V	0 to 400								

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V	
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
V _{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
			V _{IH} or V _{IL}	— 20 μA	4.4	4.5	—	4.4	—	4.4	—	
				— 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
				— 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V _{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V _{IH} or V _{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				— 4.0 mA	—	0	0.1	—	0.1	—	0.1	
				— 5.2 mA	—	0	0.1	—	0.1	—	0.1	
				— 4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
— 5.2 mA	—	0.18	0.26	—	0.33	—	0.40					
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	±0.1	—	±1	—	±1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	2	—	20	—	40	μA	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CK-Q, Q)		16	25	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLR-Q, Q)		20	32	ns
f _{MAX}	Maximum Clock Frequency	33	60		MHz

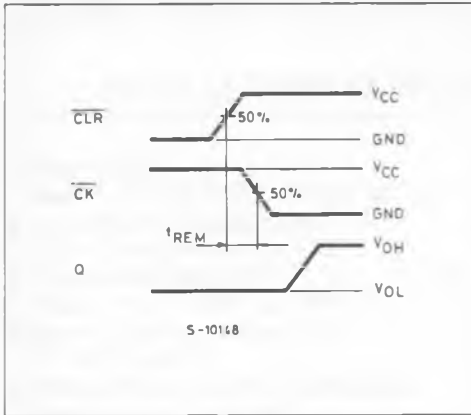
AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	90 18 15	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (\overline{CK} -Q, \overline{Q})	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (\overline{CLR} -Q, \overline{Q})	2.0 4.5 6.0		— — —	96 24 20	185 37 31	— — —	230 46 39	— — —	280 56 48	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	13 52 61	— — —	5 24 28	— — —	4 20 23	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (\overline{CK})	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (\overline{CL})	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-Up Time	2.0 4.5 6.0		— — —	35 9 8	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 1 1	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	42	—	—	—	—	—	pF

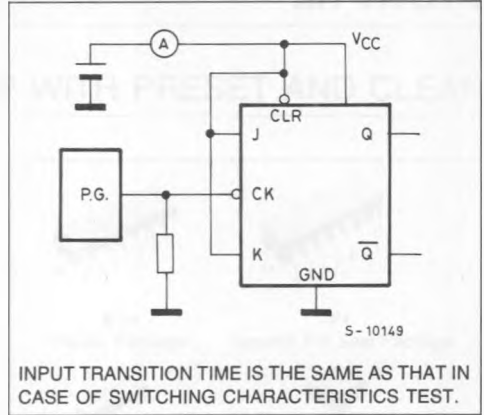
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation $I_{CC} (\text{Opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC(Opr)}



SWITCHING CHARACTERISTICS TEST WAVEFORMS

