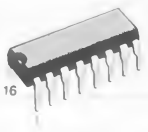
SGS-THOMSON MICROELECTRONICS

M54HCT137
M74HCT137

3 TO 8 LINE DECODER/LATCH

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS137



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

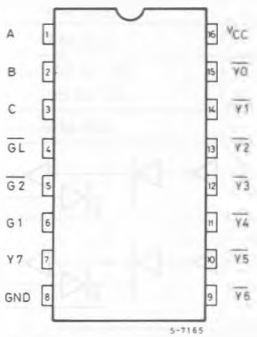
ORDERING NUMBERS:

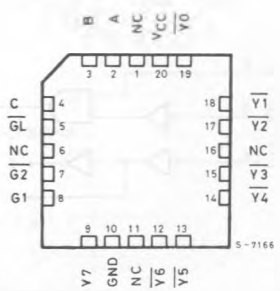
M54HCT137 F1
M74HCT137 B1N
M74HCT137 F1
M74HCT137 C1
M74HCT137 M1

DESCRIPTION

The M54/74HCT137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a three-to eight line decoder with latches on the three address inputs. When GL goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as GL remains high no address changes will be recognized. Output enable controls, G1 and G2, control the state of the outputs independently of the select or latch-enable inputs.
All of the outputs are high unless G1 is high and G2 is low. The HCT137 is ideally suited for the implementation of glitch-free decoders in stored address applications in bus oriented systems.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuits input and output characteristics are with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTIONS (top view)





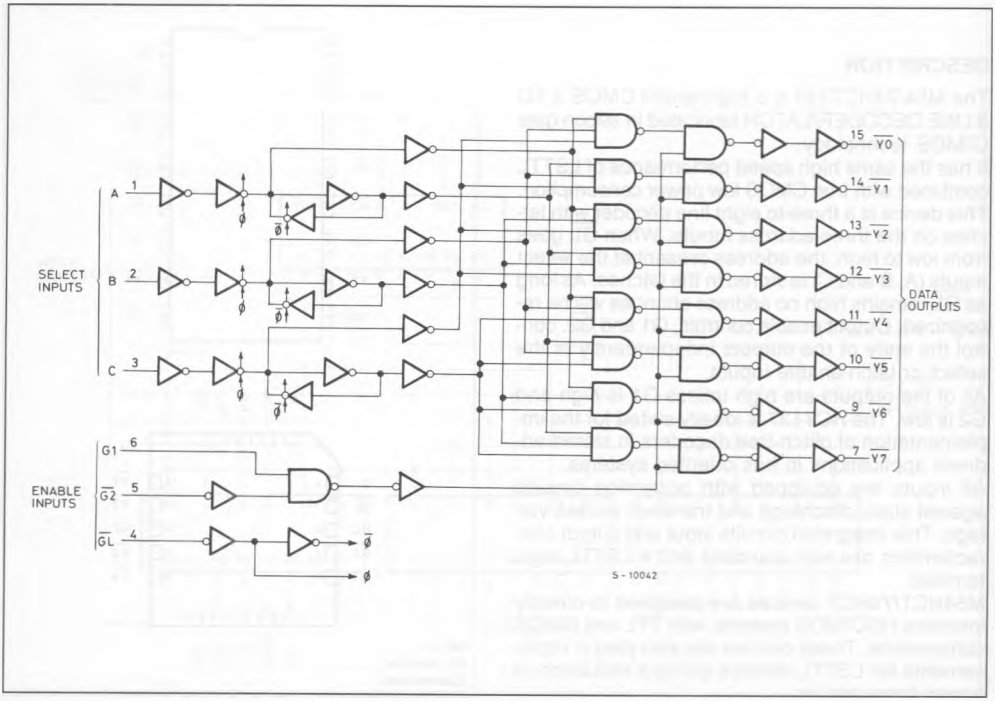
NC = No Internal Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

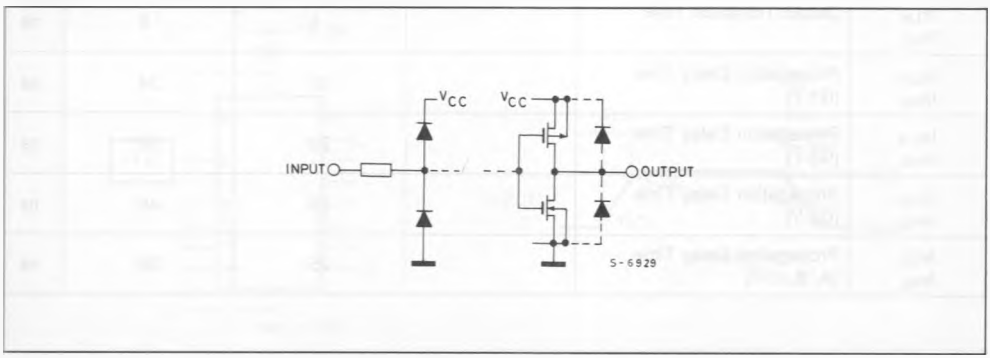
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

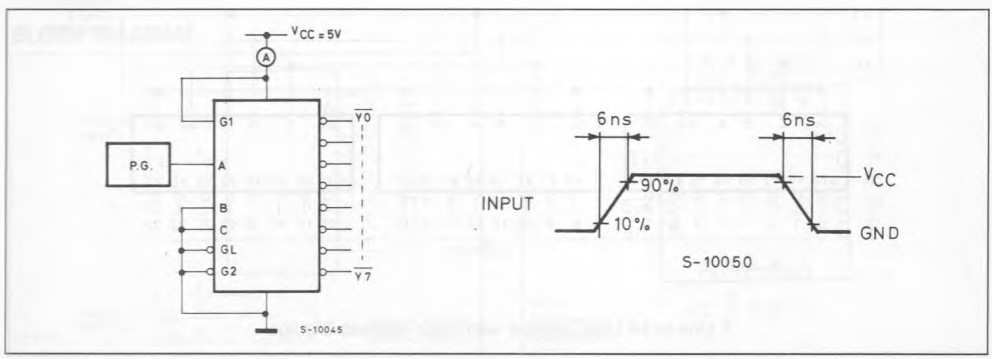
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)		21	34	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$-$\overline{Y}$)		20	32	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$-$\overline{Y}$)		29	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C-$\overline{Y}$)		25	39	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

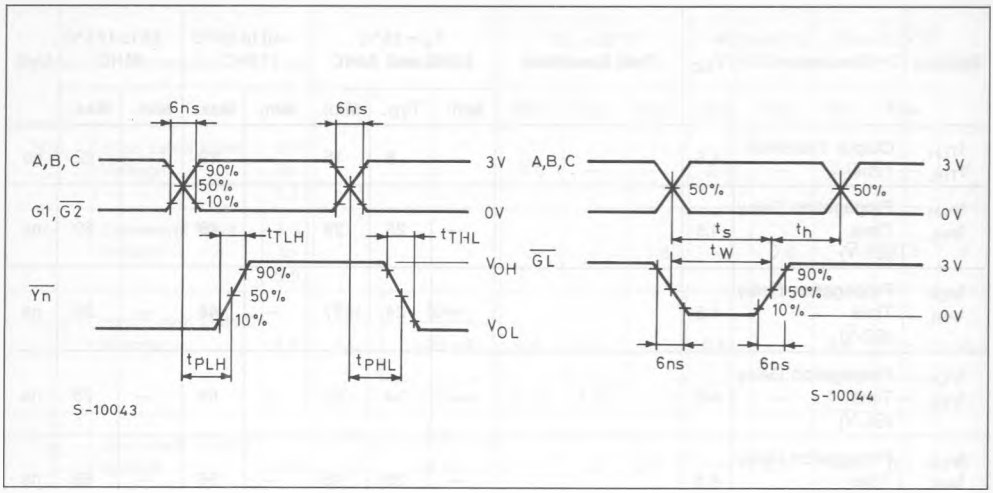
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1-$\overline{Y}$)	4.5		—	25	39	—	49	—	59	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G2-$\overline{Y}$)	4.5		—	24	37	—	46	—	56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (GL-$\overline{Y}$)	4.5		—	34	52	—	65	—	78	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C-$\overline{Y}$)	4.5		—	29	45	—	56	—	68	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	4.5		—	8	15	—	19	—	22	ns
t_s	Minimum Set-up Time (A, B, C-$\overline{GL}$)	4.5		—	2	10	—	13	—	15	ns
t_h	Minimum Hold Time (A, B, C-$\overline{GL}$)	4.5		—	—	5	—	5	—	5	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	68	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current can be obtained by the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

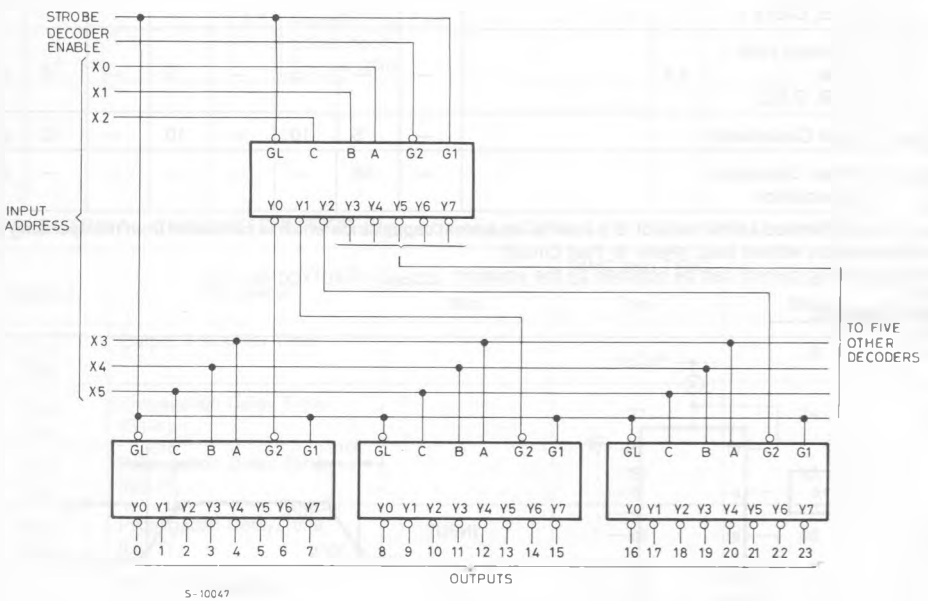
TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage