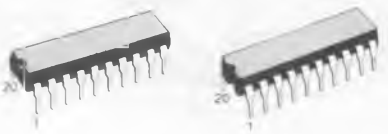
SGS-THOMSON MICROELECTRONICS

M54/74HCT540
M54/74HCT541

HCT540 OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
HCT541 OCTAL BUS BUFFER WITH NON INVERTED 3-STATE OUTPUTS

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LST540/541



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

The M54/74HCT540 and M54/74HCT541 are high speed CMOS OCTAL BUS BUFFER fabricated in silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices may be used as level converters for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible whith TTL, NMOS and CMOS output voltage levels.
The M54/74HCT540 is a non-inverting type. The M54/74HCT541 is an inverting type. If either G1 or G2 are high, the terminal outputs are in the high-impedance state.

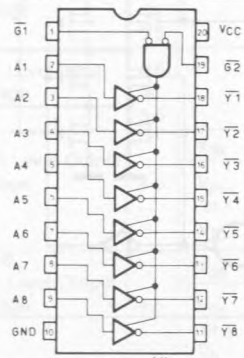
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

NOTICE FOR APPLICATION

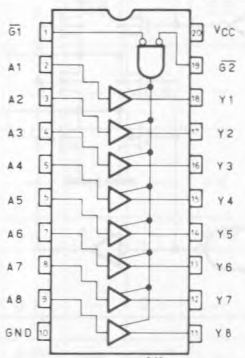
IT IS PROHIBITED TO APPLY A SIGNAL TO BUS TERMINAL WHEN IT IS IN OUTPUT MODE.
AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION

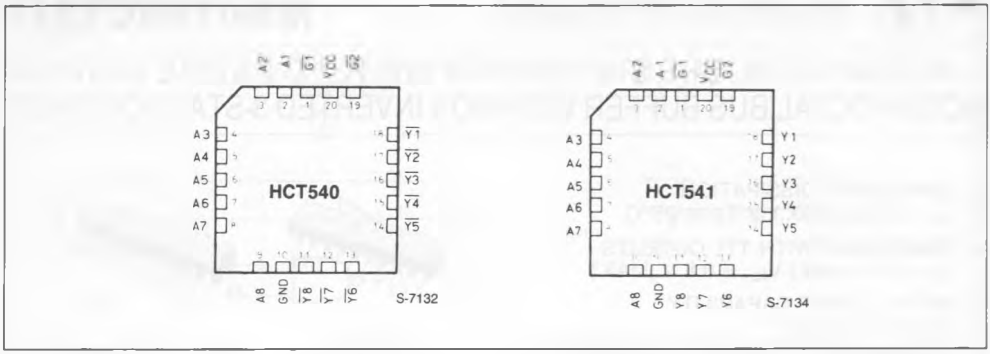
HCT540



HCT541



CHIP CARRIER

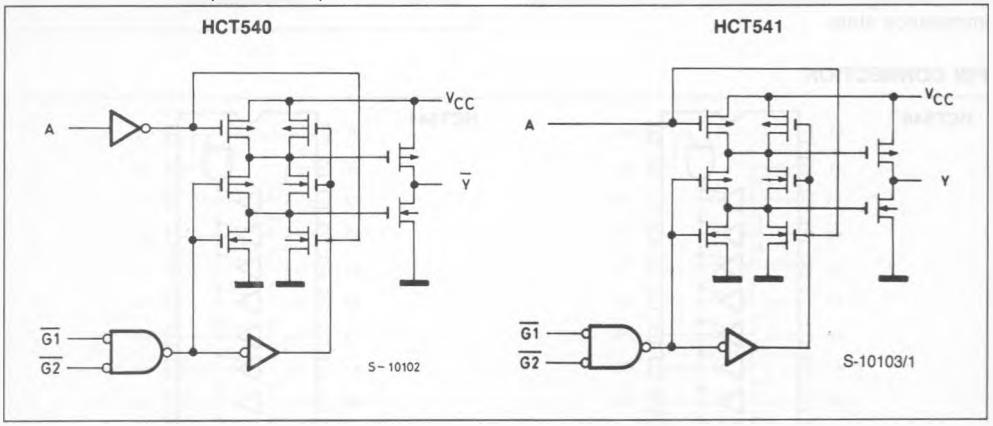


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: DONT'T CARE
Z: HIGH IMPEDANCE
*: Yn ... HCT541
$\overline{Yn}$ ... HCT540

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								V
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								V
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	

DC SPECIFICATIONS (Continued)

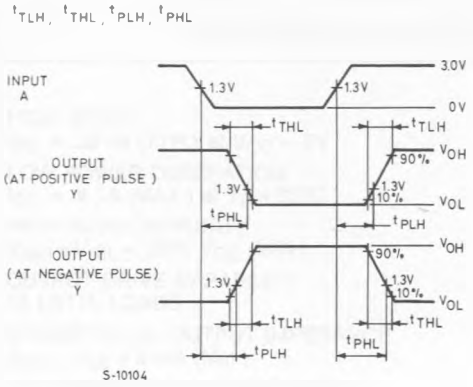
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{OZ}	3-State Output Off-State Current	5.5	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	—	—	±0.5	—	±5.0	—	±10.0	μA
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND	—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND	—	—	4.0	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND	—	—	2.0	—	2	—	3.0	mA

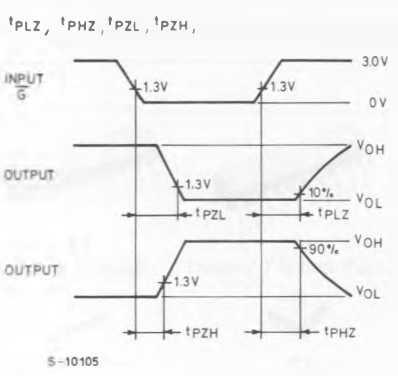
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	M54/74HCT540	—	16	26	—	33	—	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	M54/74HCT541	—	19	30	—	38	—	45	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	$R_L = 1k\Omega$	—	23	36	—	45	—	54	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	$R_L = 1k\Omega$	—	23	33	—	41	—	50	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HCT540	—	37	—	—	—	—	—	pF
			M54/74HCT541	—	39	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

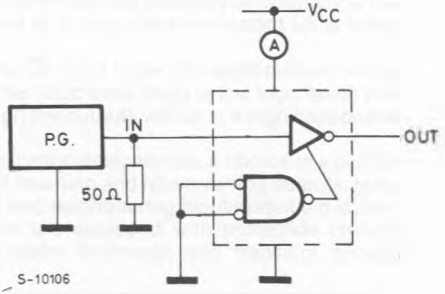
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

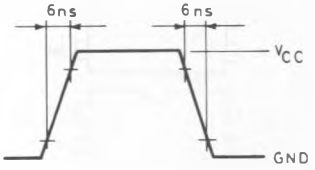




TEST CIRCUIT I_{CC} (Opr.)

HCT540





The other inputs are connected V_{CC} line or GND line.

TEST CIRCUIT OF THE HCT541 IS THE SAME AS THIS.