

## SERIAL INPUT LCD DRIVER

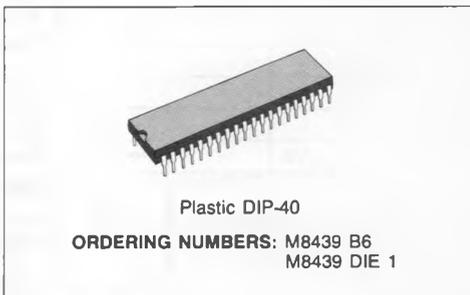
- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER: LATCH MODE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- - 40 TO 85°C TEMPERATURE RANGE

### DESCRIPTION

The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.

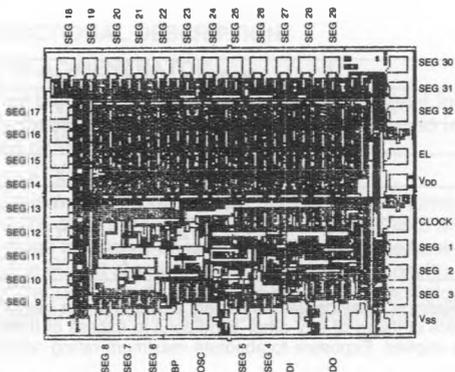
The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.



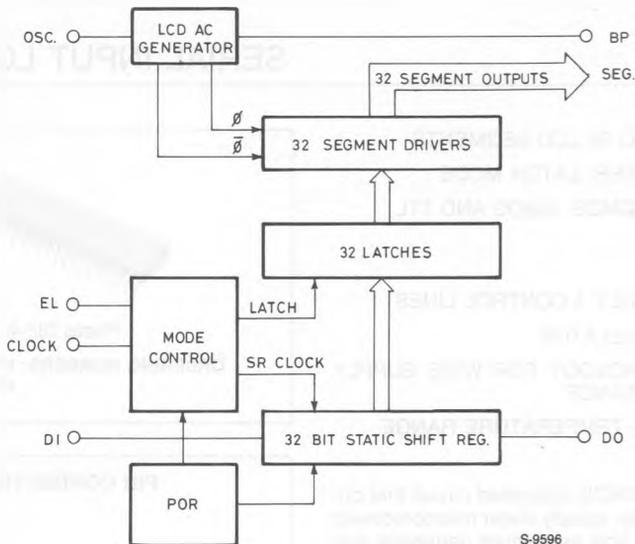
### PIN CONNECTIONS

*VDD	1	40	CLOCK
EL	2	39	SEG 1
SEG 32	3	38	SEG 2
SEG 31	4	37	SEG 3
SEG 30	5	36	V <sub>SS</sub>
SEG 29	6	35	DO
SEG 28	7	34	DI
SEG 27	8	33	SEG 4
SEG 26	9	32	SEG 5
SEG 25	10	31	OSC.
SEG 24	11	30	BP
SEG 23	12	29	SEG 6
SEG 22	13	28	SEG 7
SEG 21	14	27	SEG 8
SEG 20	15	26	SEG 9
SEG 19	16	25	SEG 10
SEG 18	17	24	SEG 11
SEG 17	18	23	SEG 12
SEG 16	19	22	SEG 13
SEG 15	20	21	SEG 14

5-8309



## BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)  
 EL :Enable/Latch control input  
 DI :Serial data input  
 DO :Serial data output  
 BP :Backplane output  
 SEG :Segment output signal

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	- 0.3 to +12	V
$V_I$	Input voltage	VSS - 0.3 to VDD + 0.3	V
$V_O$	Output voltage	VSS - 0.3 to VDD + 0.3	V
$P_D$	Power dissipation	250	mW
$T_{stg}$	Storage temperature	- 55 to +125	°C
$T_A$	Operating temperature	- 40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$  and  $V_{DD} = 5\text{V}$  unless otherwise noted)**STATIC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$V_{DD}$	Supply Voltage		3	10	V
$I_{DD}$	Supply Current	Oscillator $f < 15\text{kHz}$		60	$\mu\text{A}$
$I_Q$	Quiescent Current	$V_{DD} = 10\text{V}$		10	$\mu\text{A}$
$V_{IH}$	Input High Level	CLOCK DI EL	$.5V_{DD}$	$V_{DD}$	V
$V_{IL}$	Input Low Level		0	$.2V_{DD}$	V
$I_{IN}$	Input Current			$\pm 5$	$\mu\text{A}$
$C_I$	Input Capacitance			5	pF
$V_{IH}$	Input High Level	OSC	Driven mode	$9V_{DD}$	V
$V_{IL}$	Input Low Level		Driven mode	$.1V_{DD}$	V
$I_{IN}$	Input Current		Driven mode	$\pm 10$	$\mu\text{A}$
$R_{ON}$	Segment Output Impedance	$I_{IL} = 10\mu\text{A}$		40	$\text{k}\Omega$
$R_{ON}$	Backplane Output Impedance	$I_L = 100\mu\text{A}$		3	$\text{k}\Omega$
$V_{OFF}$	Output Offset Voltage	$C_L = 250\text{pF}$ between each SEG output and BP		$\pm 50$	mV
$R_{ON}$	Data Output Impedance	$I_L = 100\mu\text{A}$		3	$\text{k}\Omega$

**DYNAMIC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$t_{TR}$	Transition Time OSC	Driven mode		500	ns
$t_{SD}$	Data Set-up Time	Fig. 1 and 2	150		ns
$t_{HD}$	Data Hold Time	Fig. 1 and 2	50		ns
$t_{SE}$	EL Set-up Time	Fig. 1	100		ns
$t_{HE}$	EL Hold Time	Fig. 1	100		ns
$t_{WE}$	EL Pulse Width	Fig. 2	175		ns
$t_{CE}$	Clock to EL Time	Fig. 2	250		ns
$t_{pd}$	DO Propagation Delay	Fig. 1, 2; $C_L = 55\text{pF}$		500	ns
f	Clock Rate	$V_{DD} = 10$ 50% duty cycle;	DC	1.5	MHz

**FUNCTIONAL DESCRIPTION****LCD-AC-GENERATOR**

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

**OSCILLATOR MODE:**

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected bet-

ween input OSC and VSS. A value of 18pF gives a backplane frequency of  $80\text{Hz} \pm 30\%$  at  $V_{DD} = 5\text{V}$ . The variation of the backplane frequency over the entire temperature and supply voltage range is  $\pm 50\%$ .

**DRIVEN MODE:**

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

## FUNCTIONAL DESCRIPTION (continued)

### DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimum value. The signal at pin OSC swings within a range from  $0.3V_{DD}$  to  $0.7V_{DD}$ . If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

### SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

### MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.

Data is serially shifted in and out of the shift register on the negative transition of the clock.

Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

### POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.

The power on reset pulse resets all shift register stages and the latches that control the segment dri-

vers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

### CONDITIONS FOR POWER-ON RESET FUNCTION

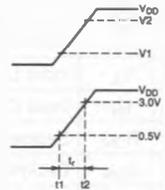
The POR circuit triggers on the rising slope of the positive supply voltage  $V_{DD}$ . A reset pulse will be generated, if conditions a) through d) are given:

a) Level

Rising slope from V1 to V2

V1 max = 0.5V

V2 min = 3.0V



b) Rise time

$t_r$  min = 10  $\mu$ s

$t_r$  max = 1 s

c) Rise function

The function of  $V_{DD}$  between  $t_1$  and  $t_2$  may be nonlinear, but should not show a maximum and should not exceed 0.25 V/ $\mu$ s.

d) Recovery time

The minimum time between turn-off and turn-on of  $V_{DD}$  is 1s.

### CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.

The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.

Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.

Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of latch mode: set-up and hold time

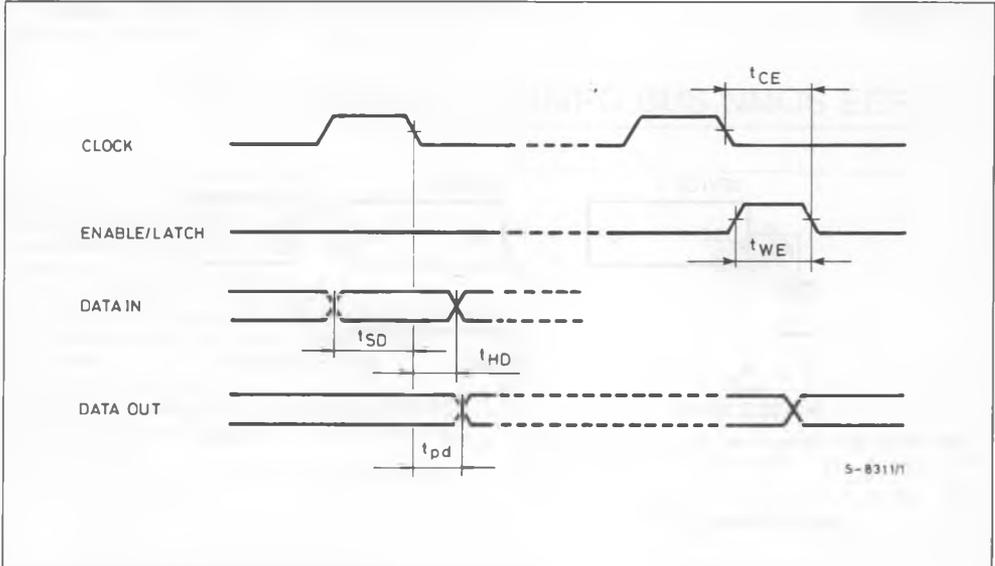


Fig. 2 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

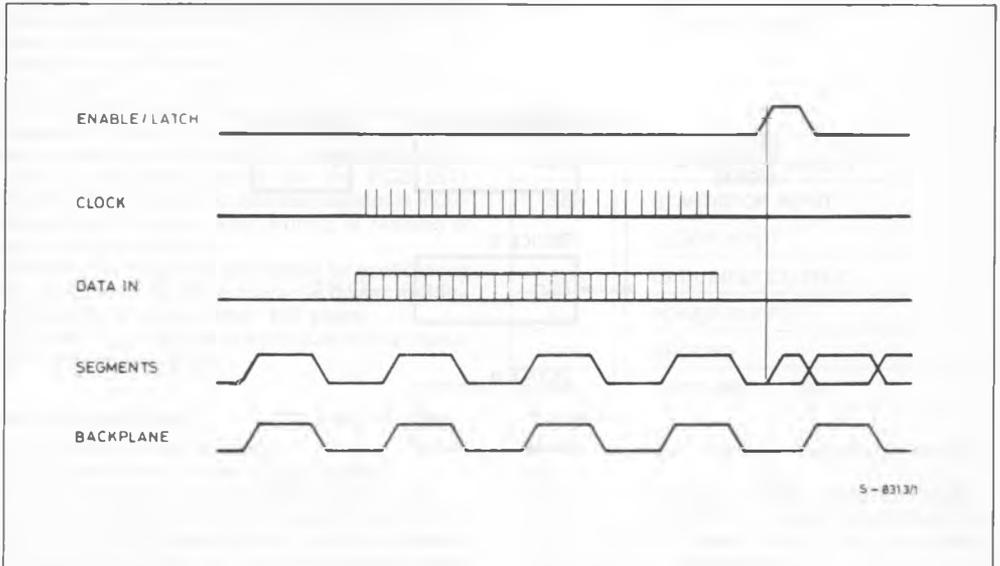


Fig. 3 - Cascade configuration, self oscillating

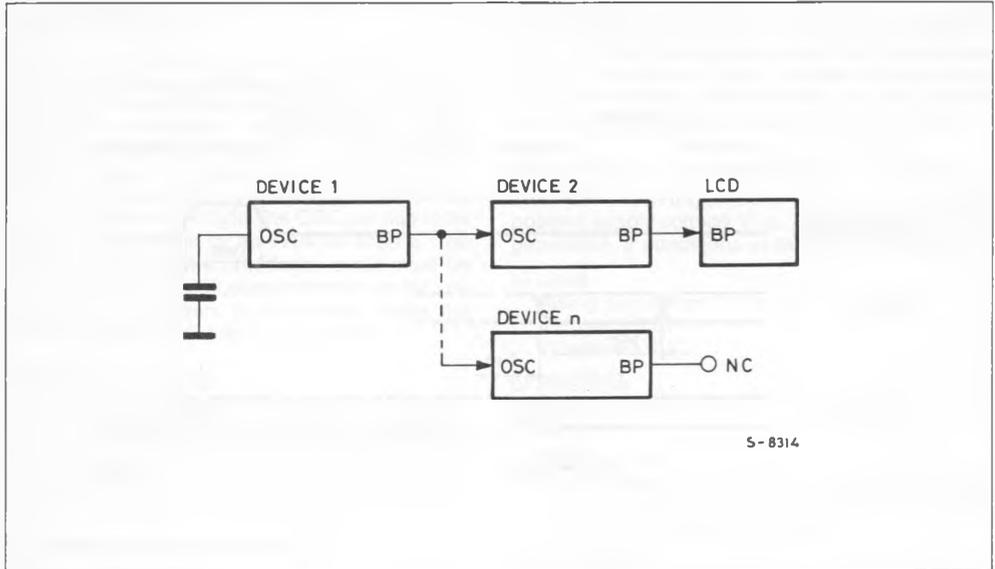


Fig. 4 - Cascade configuration, driven by external signal

