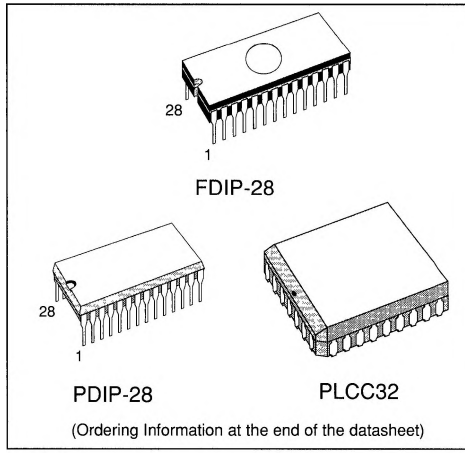
SGS-THOMSON MICROELECTRONICS

M87C257

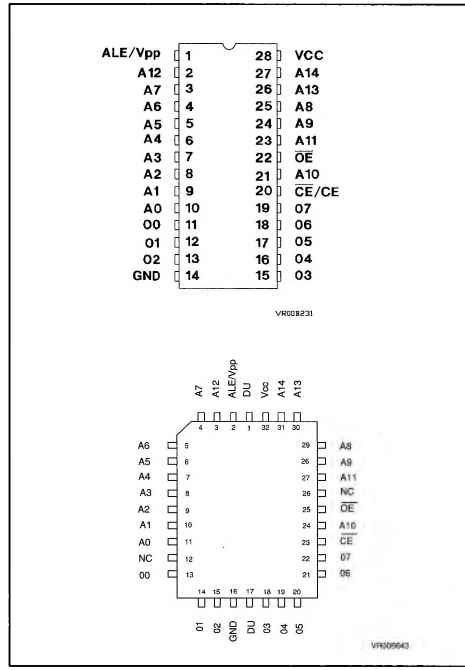
LATCHED 256K (32Kx8) CMOS UV EPROM - OTP ROM

- INTEGRATED ADDRESS LATCH.
- VERY FAST ACCESS TIME : 100 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Active Current 30mA
  - Standby Current 200µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIME OF AROUND 3 SECONDS (PRESTO II ALGORITHM).



(Ordering Information at the end of the datasheet)

Figure 1 : Pin Connection



DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically reprogrammable EPROM. The M87C257 incorporates latches on all addresses input to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

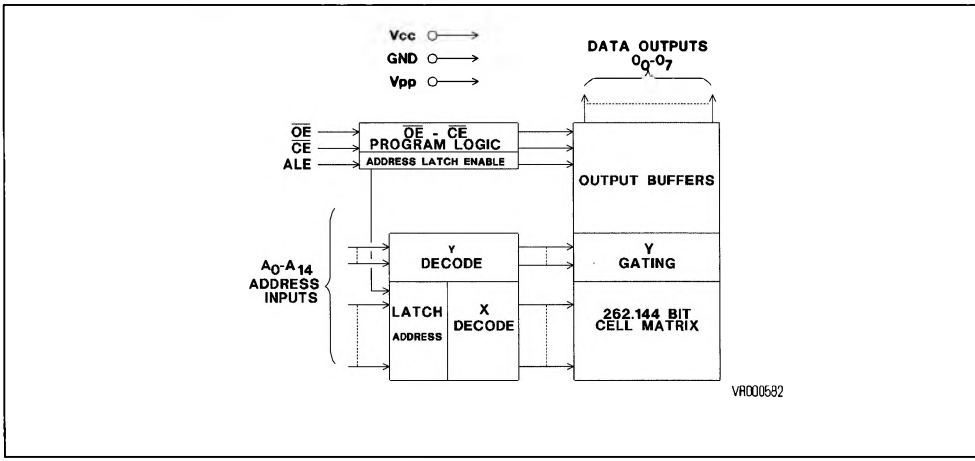
The M87C257 is housed in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIL or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A14	ADDRESS INPUTS
O0-O7	DATA INPUT/OUTPUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/V_{PP}	ADDRESS LATCH ENABLE/V_{PP}
NC	NON CONNECTED
V_{CC}	+ 5V POWER SUPLY
GND	GROUND
DU	DON'T USE

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltage with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
VA9	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
Tbias	Temperature range under bias	-50 to +125	°C
Tstg	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS				
	$\overline{CE}$	OE	A9	ALE/V_{PP}	OUTPUT
READ (LATCHED ADDRESS)	L	L	X	L	D_{OUT}
READ (CURRENT ADDRESS)	L	L	X	H	D_{OUT}
OUTPUT DISABLE	L	H	X	X	HIGH Z
STANDBY	H	X	X	X	HIGH Z
HIGH SPEED PROGRAMMING	L	H	X	V_{PP}	D_{IN}
PROGRAM VERIFY	H	L	X	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	H	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	X	CODE

NOTE : X Don't care ; V_H = 12V ± 0.5V; H = High ; L = Low

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**10XF1, 12XF1, 15XF1, 20XF1**		**10F1, 12F1, 15F1, 20F1**	
V_{CC} Power Supply (1)	5V ± 5%		5V ± 10%	

NOTE : "F" stands for ceramic package. Plastic packaged device code features B, M or C (see ordering information).

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} IOUT= 0 mA (F = 5MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH} - Stable Inputs		1	mA
I_{CC3}(4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2V - Stable Inputs		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC} - 0.8		V

AC CHARACTERISTICS

Symbol	Parameter	Test condition	87C257								Unit
			-10		-12		-15		-20		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		100		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		40		50		60		70	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	30	0	40	0	40	0	40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0		ns
t_{LL}	Latch deselect Width		35		35		35		50		ns
t_{AL}	Add to latch setup		7		7		7		15		ns
t_{LA}	Add Hold from latch		20		20		20		30		ns
t_{LOE}	ALE to Output Enable		20		20		20		30		ns

CAPACITANCE(3)

T_{AMB} = 25°C, f = 1 MHz

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From Date Code 9040.

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs 0.8 and 2V - Outputs 0.8 and 2V

AC TEST CONDITIONS

Figure 3 : AC Testing Input/Output Waveform

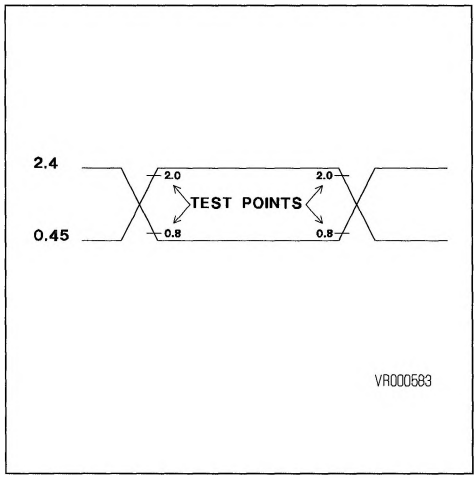


Figure 4 : AC Testing Load Circuit

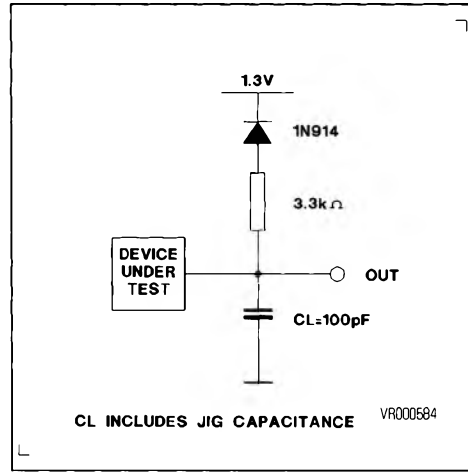
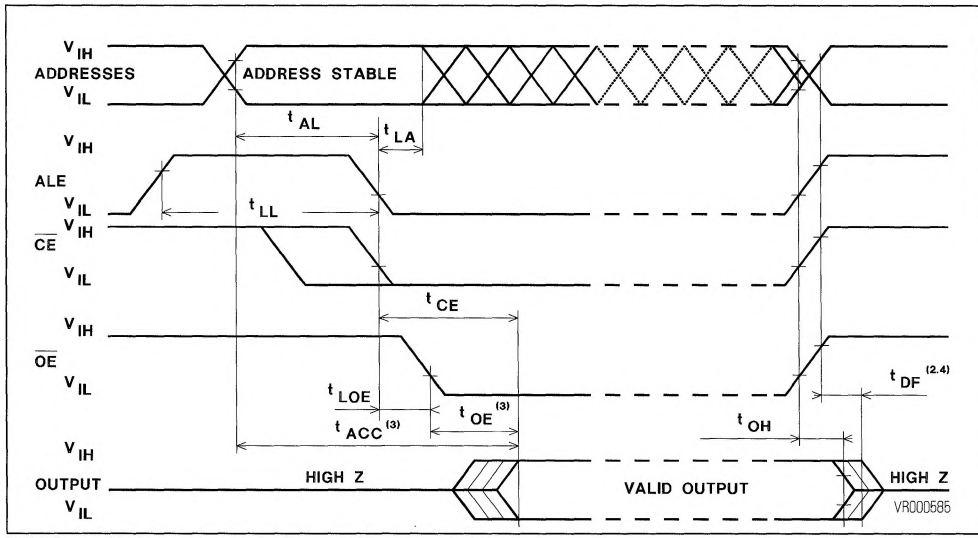


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ OPERATION

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for 12V on A9 for Electronic Signature.

READ MODE

The M87C257 has two control functions both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable ($ALE=V_{IH}$) or latched ($ALE=V_{IL}$), the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.
The M87C257 reduces the hardware interface in multiplexed address-data bus systems. Figure 6 shows a low power, small board space, minimal chip M87C257/microcontroller design. The processors multiplexed bus (AD0-7) is tied to the M87C257's address and data pins. No separate address latch is needed because the M87C257 latches all address inputs when ALE is low.

STANDBY MODE

The M87C257 has a standby mode which reduces the active current from 30mA to 0.2mA (from date code 9040). The M87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

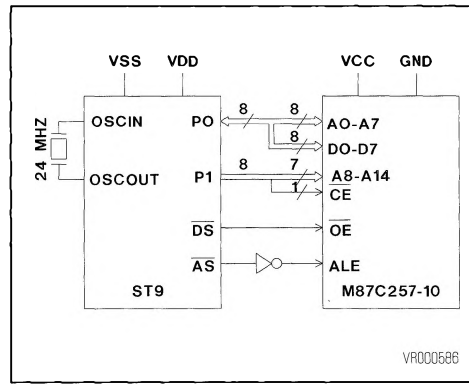
For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.
The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Figure 6 : M87C257 / ST9 Microcontroller system lay out



PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M87C257.

When delivered, (and after each erasure for UV EPROM), all bits of the M87C257 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by exposure ultraviolet light. The M87C257 is in the programming mode when V_{PP} input is at 12.75V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II programming algorithm, available for the M87C257 is an enhancement of the PRESTO algorithm used for the M27512.

During programming and verify operation a MARGIN MODE™ circuit is automatically activated. It provides adequate margin for the threshold voltage of programmed cells, thus the writing margin is independent from V_{CC} in verify mode and an overprogram pulse is not necessary, thus reducing programming time down to a theoretical value of 3 seconds.

PROGRAM INHIBIT

Programming of multiple M87C257s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel M87C257 may be common. A TTL low level pulse applied to a M87C257s $\overline{CE}$ input, with V_{PP} at 12.75V will program that M87C257. A high level CE input inhibits the other M87C257s from being programmed.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M87C257. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M87C257 with V_{PP} = V_{CC} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. When A9=V_H, ALE need not be toggled to latch each identifier address. For the SGS-THOMSON M87C257, these two identifier bytes are given below, and can be read out on the outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristic of the M87C257 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M87C257 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C257 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M87C257 window to prevent unintentional erasure. The recommended erasure procedure for the M87C257 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M87C257 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	0	0	0	0	80

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} , A1 - A8, A10 - A14 = V_{IL} ; V_{PP} = V_{CC} = 5V

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.5V)

DC AND OPERATING CHARACTERISTICS

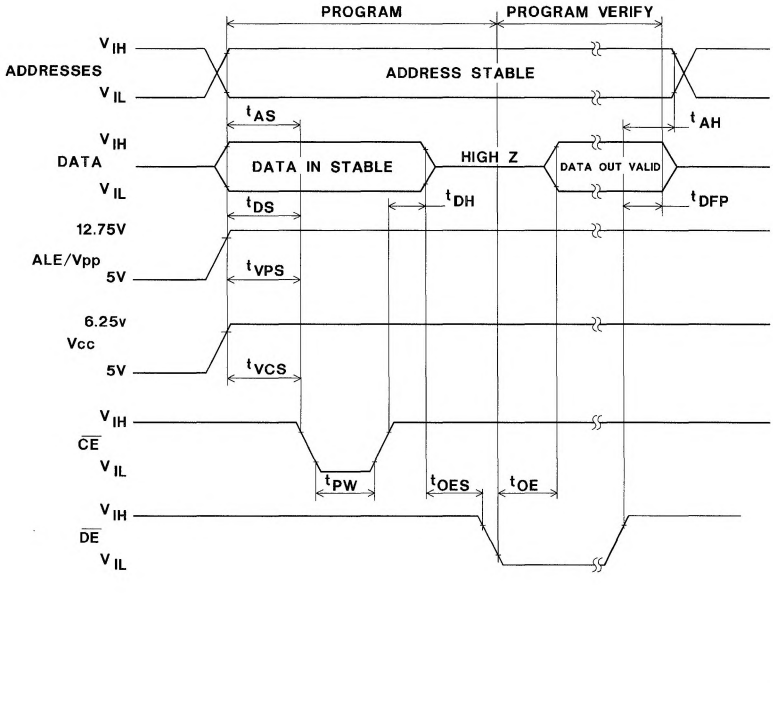
Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -1mA	V_{CC}-0.8		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	OE Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	µs
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from OE			100	ns

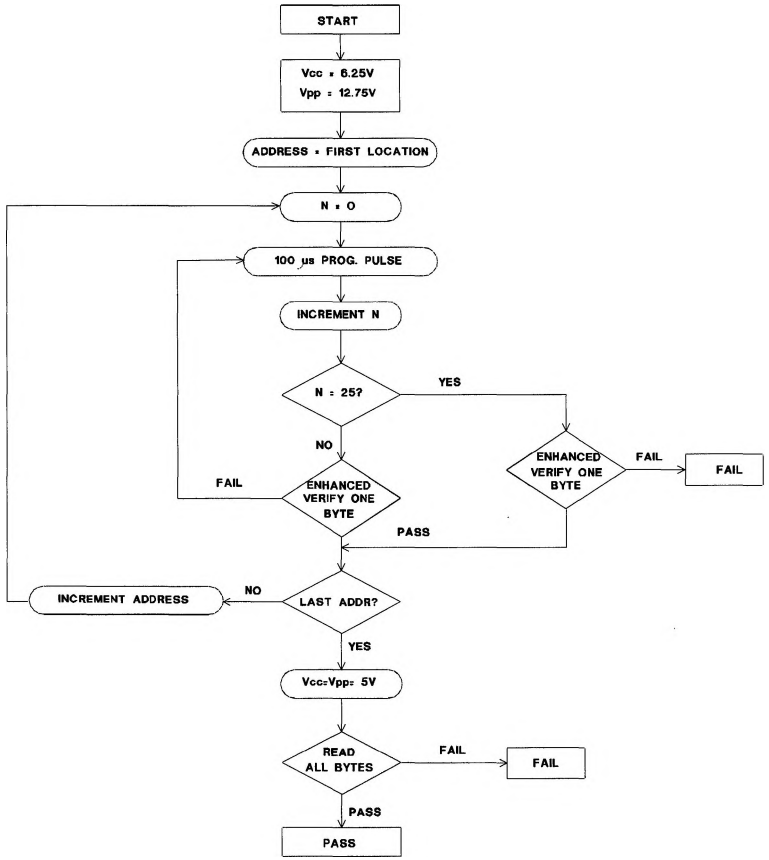
NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 7 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M87C257 a 0.1µF capacitor is required across V_{PP} and GROUND to supress spurious voltage transient which can damage the device.

Figure 8 : PRESTO II Programming Algorithm



VR000588

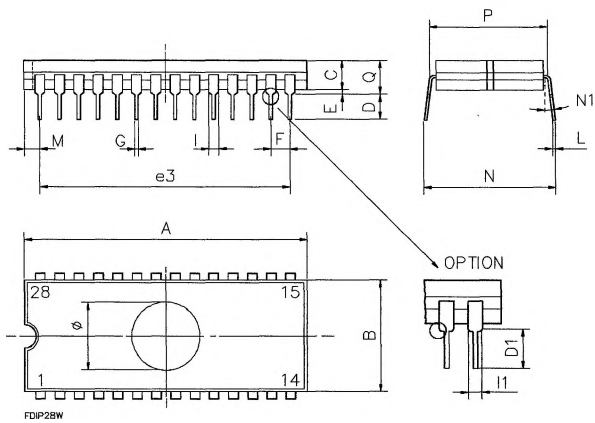
ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M87C257-10XF1	100 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-10F1	100 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-15XF6	150 ns	5V ± 5%	-40°C to + 85°C	FDIP28-W
M87C257-15F6	150 ns	5V ± 10%	-40°C to + 85°C	FDIP28-W
M87C257-20XF7	200 ns	5V ± 5%	-40°C to + 105°C	FDIP28-W
M87C257-20XF3	200 ns	5V ± 5%	-40°C to + 125°C	FDIP28-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 9 : 28-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e 3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

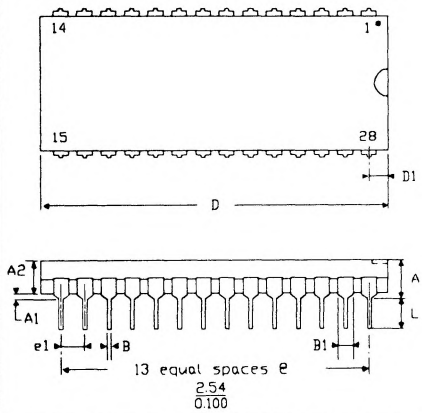
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M87C257-12XB1	120 ns	5V ± 5%	0°C to + 70°C	DIP28
M87C257-15XB1	150 ns	5V ± 5%	0°C to + 70°C	DIP28
M87C257-15B1	150 ns	5V ± 10%	0°C to + 70°C	DIP28
M87C257-15XB6	150 ns	5V ± 5%	-40°C to + 85°C	DIP28
M87C257-15B6	150 ns	5V ± 10%	-40°C to + 85°C	DIP28
M87C257-12XC1	120 ns	5V ± 5%	0°C to + 70°C	PLCC32
M87C257-15XC1	150 ns	5V ± 5%	0°C to + 70°C	PLCC32
M87C257-15C1	150 ns	5V ± 10%	0°C to + 70°C	PLCC32
M87C257-15XC6	150 ns	5V ± 5%	-40°C to + 85°C	PLCC32
M87C257-15C6	150 ns	5V ± 10%	-40°C to + 85°C	PLCC32

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

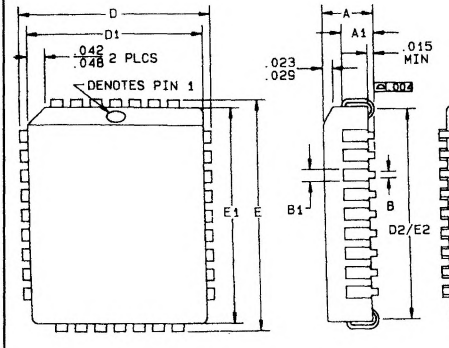
PACKAGE MECHANICAL DATA - OTP ROM

Figure 10 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 11 : PLCC32-32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.35		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530