M93C86, M93C76, M93C66
M93C56, M93C46, M93C06

16K/8K/4K/2K/1K/256 (x8/x16) Serial Microwire Bus EEPROM

- INDUSTRY STANDARD MICROWIRE BUS
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: by WORD (x16) or by BYTE (x8)
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M93Cx6 version
  - 2.5V to 5.5V for M93Cx6-W version
  - 1.8V to 3.6V for M93Cx6-R version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH-UP PERFORMANCES

PSDIP8 (BN)
0.25mm Frame

SO8 (MN)
150mil Width

DESCRIPTION

This M93C86/C76/C66/C56/C46/C06 specification covers a range of 16K/8K/4K/2K/1K/256 bit serial EEPROM products respectively. In this text, products are referred to as M93Cx6. The M93Cx6 is an Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. The M93Cx6 memory is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol.

Figure 1. Logic Diagram

AI01928

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground
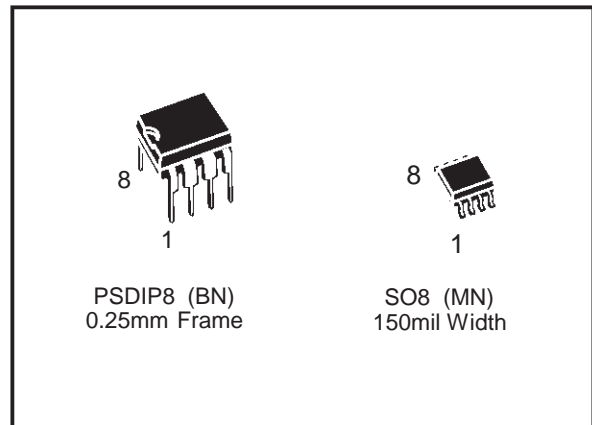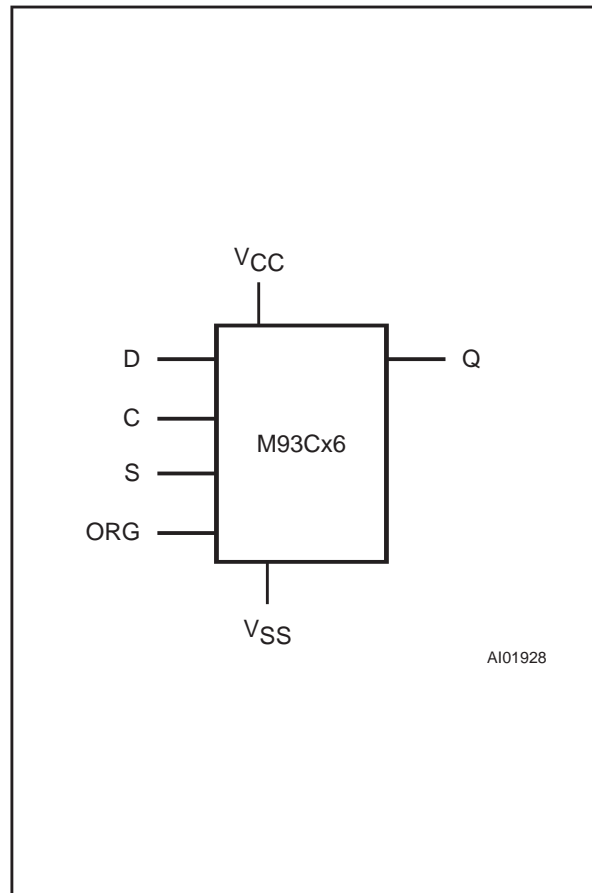
Figure 2A. DIP and SO Pin Connections

M93Cx6

```
S   [ 1      8 ] V_CC
C   [ 2      7 ] DU
D   [ 3      6 ] ORG
Q   [ 4      5 ] V_SS
```
AI01929B
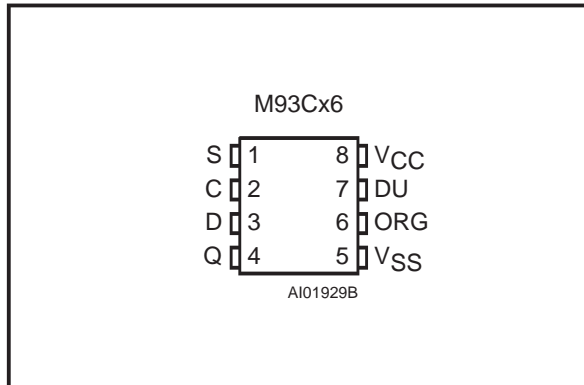
Warning: DU = Don't Use

Figure 2B. SO 90° Turn Pin Connections

M93Cx6

```
DU   [ ①     8 ] ORG
V_CC [ 2      7 ] V_SS
S    [ 3      6 ] Q
C    [ 4      5 ] D
```
AI00900
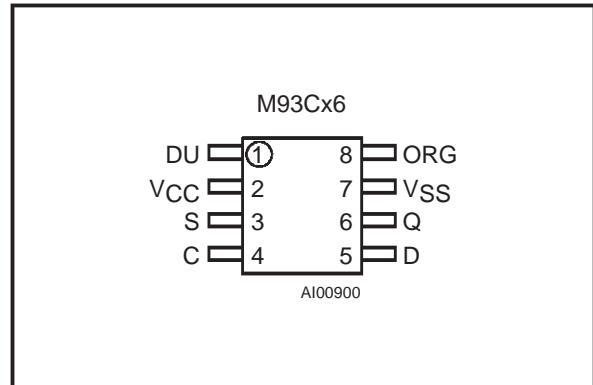
Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)	–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	4000	V
	Electrostatic Discharge Voltage (Machine model) [3]	500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The M93Cx6 specified at 5V±10%, the M93Cx6-W specified at 2.5V to 5.5V and the M93Cx6-R specified at 1.8V to 3.6V.

The M93Cx6 memory array organization may be divided into either bytes (x8) or words (x16) which may be selected by a signal applied on the ORG input. The M93C86/C76/C66/C56/C46/C06 is divided into either 2048/1024/512/256/128/32x8 bit bytes or 1024/512/256/128/64/16 x16 bit words respectively. These memory devices are available in both PSDIP8 and SO8 package.

The M93Cx6 memory is accessed by a set of instructions which includes Read a Byte/Word, Write a Byte/Word, Erase a Byte/Word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the M93Cx6 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 up to 16,384 bits long (for the M93C86 only), or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left

Table 3. AC Measurement Conditions

Input Rise and Fall Times	$\leq$ 50ns
Input Pulse Voltages (M93Cxx)	0.4V to 2.4V
Input Pulse Voltages (M93Cxx-W, M93Cxx-R)	$0.2V_{CC}$ to $0.8V_{CC}$
Input Timing Reference Voltages (M93Cxx)	1.0V to 2.0V
Output Timing Reference Voltages (M93Cxx)	0.8V to 2.0V
Input and Output Timing Reference Voltages (M93Cxx-W, M93Cxx-R)	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

AI02553
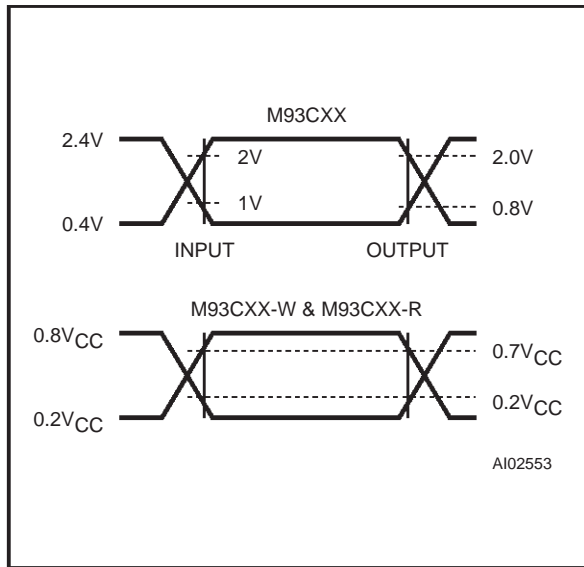
running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the byte or word locations of the M93Cx6. After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

An internal feature of the M93Cx6 provides Power-on Data Protection by inhibiting any operation when the Supply is too low for reliable operation. The design of the M93Cx6 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

The DU (Don't Use) pin does not affect the function of the memory. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The M93Cx6 is organised in either bytes (x8) or words (x16). If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected; when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6 is in standby mode, the ORG input should be set to either V_{SS} or V_{CC} in order to achieve minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to the ORG input pin may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode.

– At Power-up and Power-down, the device must NOT be selected (that is, the S input must be driven low) until the supply voltage reaches the operating value V_{CC} specified in the AC and DC tables.

– When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

For the M93Cx6 specified at 5V, the POR threshold voltage is around 3V. For all the other M93Cx6 specified at low V_{CC} (with -W and -R V_{CC} range options), the POR threshold voltage is around 1.5V.

Table 4. Capacitance [1]

(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5A. DC Characteristics for M93CXX

(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2.5	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		±2.5	μA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	μA
V_{IL}	Input Low Voltage (D, C, S)	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400μA	2.4		V

Table 5B. DC Characteristics for M93CXX

(T_A = –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2.5	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		±2.5	μA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	μA
V_{IL}	Input Low Voltage (D, C, S)	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400μA	2.4		V

Table 5C. DC Characteristics for M93CXX-W

(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	VCC = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	VCC = 2.5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		10	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC} – 0.2		V

Table 5D. DC Characteristics for M93CXX-R [1]

(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	VCC = 3.6V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	VCC = 1.8V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC} – 0.2		V

Note: 1. This is preliminary data.

Table 6A. AC Characteristics

Symbol	Alt	Parameter	M93C86/76/66/56/46/06				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = −40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = −40 to 125°C		
			Min	Max	Min	Max	
t_{SHCH}	t_{CSS}	Chip Select Set-up Time M93C06, M39C46, M93C56, M93C66	50		50		ns
		Chip Select Set-up time M93C76, M93C86	100		100		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		100		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		400	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		400	ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH} [1]		Chip Select Low to Clock High	250		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	250		250		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		400	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} [2]	t_{SKH}	Clock High Time	250		250		ns
t_{CLCH} [2]	t_{SKL}	Clock Low Time	250		250		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1μs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1μs. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns.

Table 6B. AC Characteristics

Symbol	Alt	Parameter	M93C86/76/66/56/46/06				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = −40 to 85°C		V_{CC} = 1.8V to 3.6V,[3] T_A = 0 to 70°C, T_A = −20 to 85°C		
			Min	Max	Min	Max	
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		100		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		100		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		500	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		500	ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH} [1]		Chip Select Low to Clock High	250		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	1000		1000		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} [2]	t_{SKH}	Clock High Time	350		350		ns
t_{CLCH} [2]	t_{SKL}	Clock Low Time	250		250		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1μs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1μs. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns.
3. This is preliminary data.

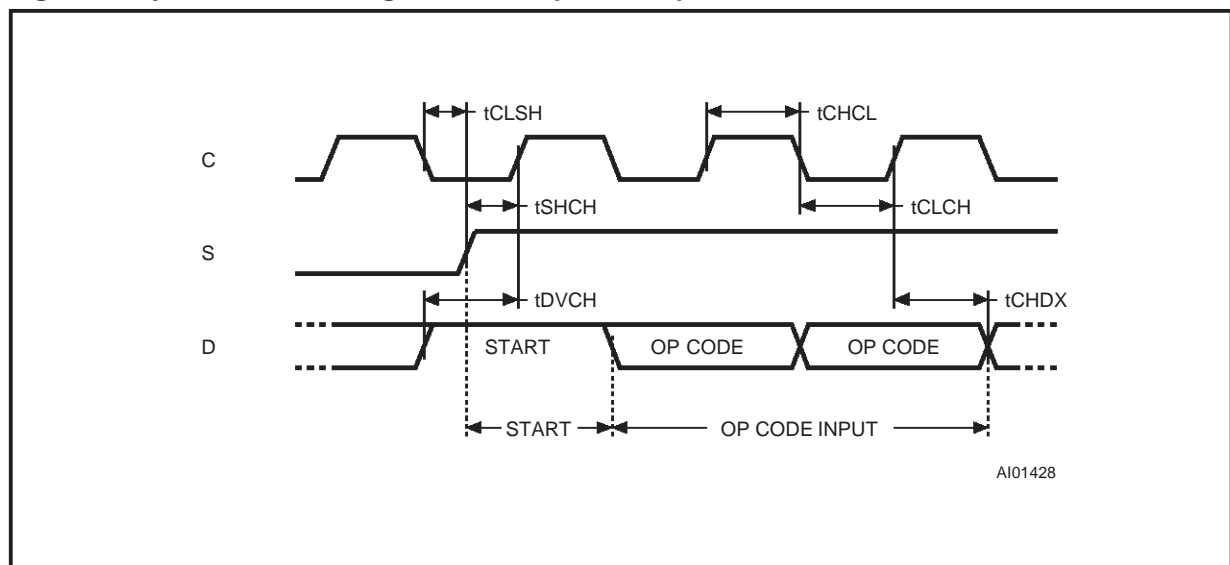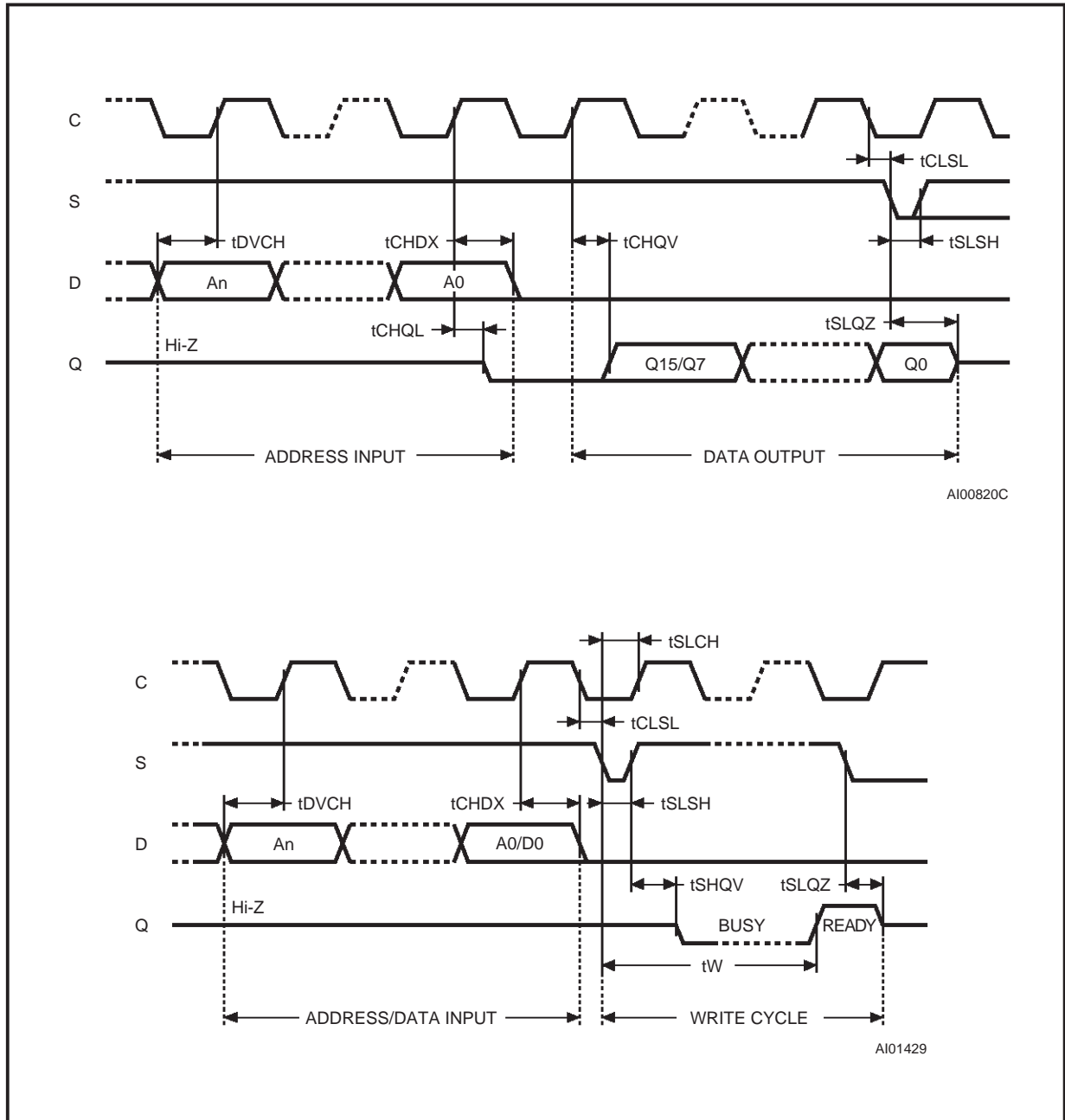## Figure 4. Synchronous Timing, Start and Op-Code Input

Figure 5. Synchronous Timing, Read or Write

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INSTRUCTIONS

The M93C86/C76/C66/C56/C46/C06 have seven instructions, as shown in Table 7. Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that the clock C is low). After the device is selected, the internal logic waits for the start bit, which defines the beginning of the instruction bit stream. The start bit is the first '1' read on the D input during the rising edge of the clock C. Following the start bit, the op-codes of the instructions are made up of the 2 following bits. Note that some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is then followed by the address of the byte/word to be accessed. For the M93C06 and M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see Table 7A). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see Table 7B). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see Table 7C).

The M93Cx6 is fabricated in CMOS technology and is therefore able to run from 0Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The M93Cx6 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed. The Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions and the internal programming cycle cannot run. When power is first applied, the M93Cx6 is in Erase/Write Disable mode and all Erase/Write instructions are inhibited. When the EWEN instruction is executed, Erase/Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below

the power-on reset Threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle. The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) starts a self-timed erase cycle. If the M93Cx6 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is composed of the Op-Code followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, *Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle.* This is important as, if S is brought low before or after this specific frame window, the addressed location will not be programmed.

If the M93Cx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle). The Write instruction includes an automatic Erase cycle before writing the data, it is therefore unnecessary to execute an Erase instruction before a Write instruction execution.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above. If the M93Cx6 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

Table 7A. Instruction Set for the M93C06 and M93C46

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) [1, 2]	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) [1, 3]	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
EWEN	Erase/Write Enable	1	00	11X XXXX		10	11 XXXX		9
EWDS	Erase/Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

Notes: 1. X = don't care bit.
2. Address bits A6 and A5 are not decoded by the M93C06.
3. Address bits A5 and A4 are not decoded by the M93C06.

Table 7B. Instruction Set for the M93C56 and M93C66

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) [1, 2]	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) [1, 3]	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
EWEN	Erase/Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
EWDS	Erase/Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXXX XXXX		12	10XX XXXX		11
WRAL	Write All Memory with same Data	1	00	0 1XXXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

Notes: 1. X = don't care bit.
2. Address bit A8 is not decoded by the M93C56.
3. Address bit A7 is not decoded by the M93C56.

Table 7C. Instruction Set for the M93C76 and M93C86

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) [1, 2]	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) [1, 3]	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0		A9-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
EWEN	Erase/Write Enable	1	00	11X XXXX XXXX		14	11 XXXX XXXX		13
EWDS	Erase/Write Disable	1	00	00X XXXX XXXX		14	00 XXXX XXXX		13
ERASE	Erase Byte or Word	1	11	A10-A0		14	A9-A0		13
ERAL	Erase All Memory	1	00	10X XXXX XXXX		14	10 XXXX XXXX		13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

Notes: 1. X = don't care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

Write All

The Write All instruction (WRAL) writes the Data Input byte or word into all the addresses of the memory device. As for the Erase All instruction, a dummy address is input during the instruction transfer.

If the M93Cx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Out-put (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the M93Cx6 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the STMicroelectronics application note AN394 "MICROWIRE EEPROM Common I/O Operation".

**Figure 6. READ, WRITE, EWEN, EWDS Sequences**

AI00878C
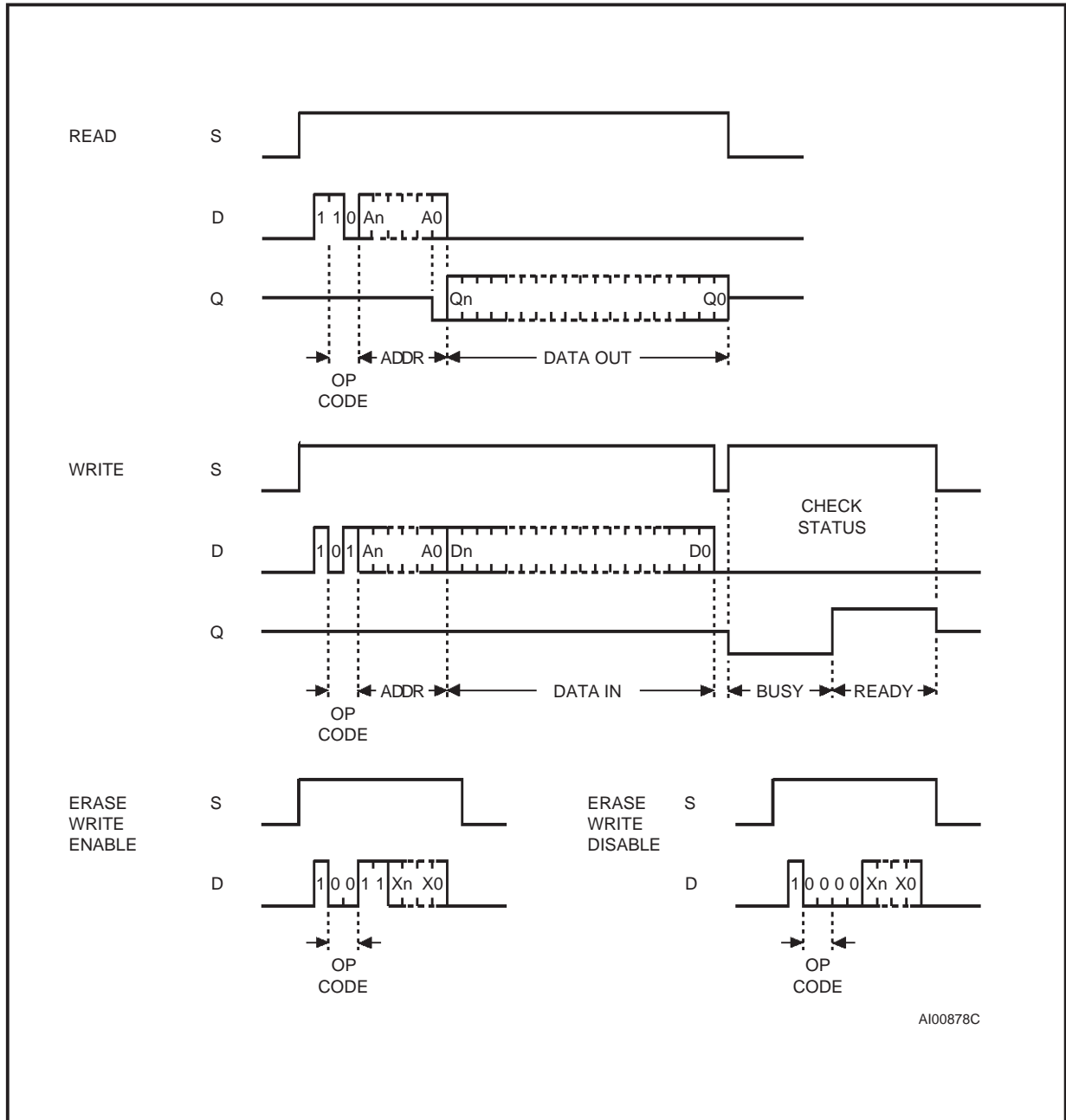
Note: An, Xn, Qn, Dn: Refer to Table 6a for the M93C06 and M93C46; to Table 6b for the M93C56 and M93C66; to Table 6c for the M93C76 and M93C86.

Figure 7. ERASE, ERAL Sequences

AI00879B
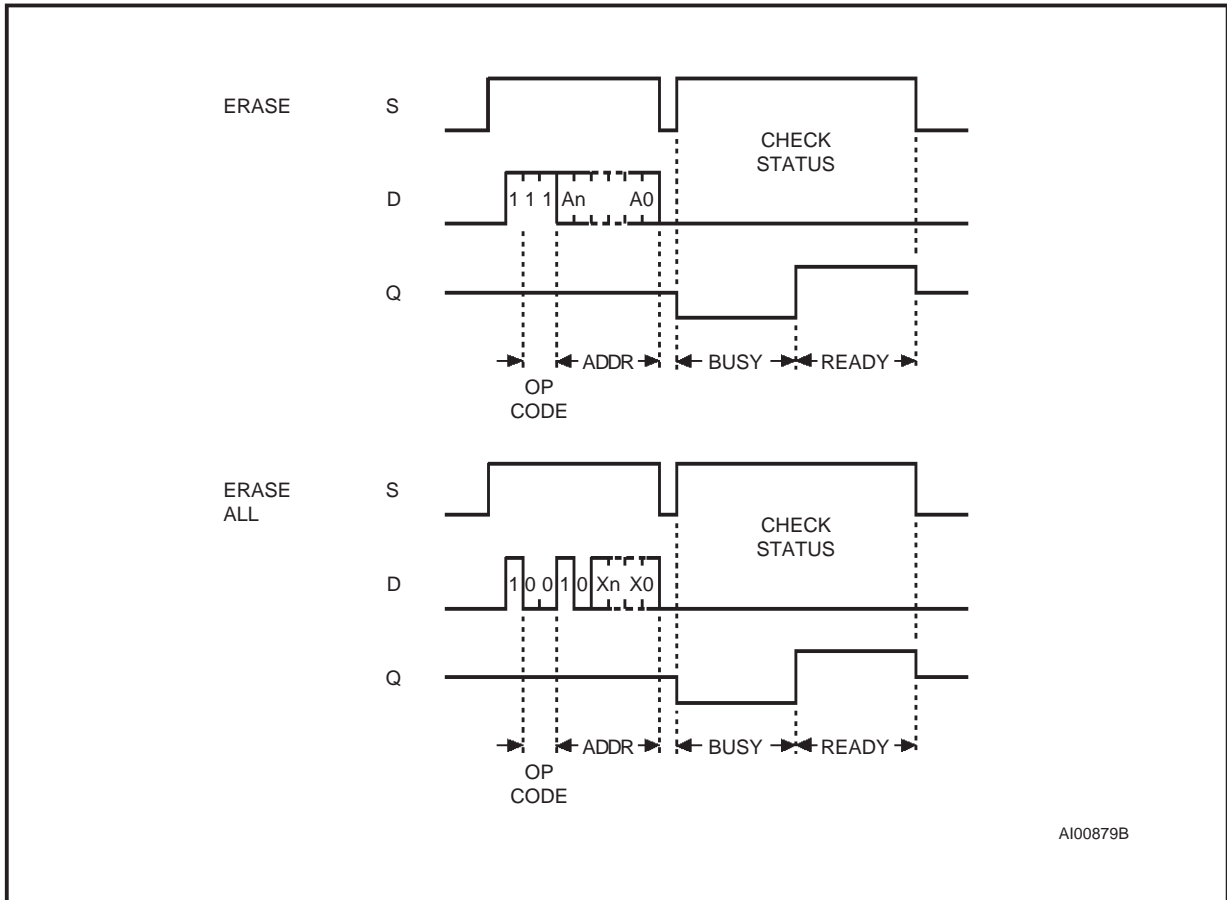
Note: An, Xn: Refer to Table 7a for the M93C06 and M93C46; to Table 7b for the M93C56 and M93C66; to Table 7c for the M93C76 and M93C86.

Figure 8. WRAL Sequence

AI00880C
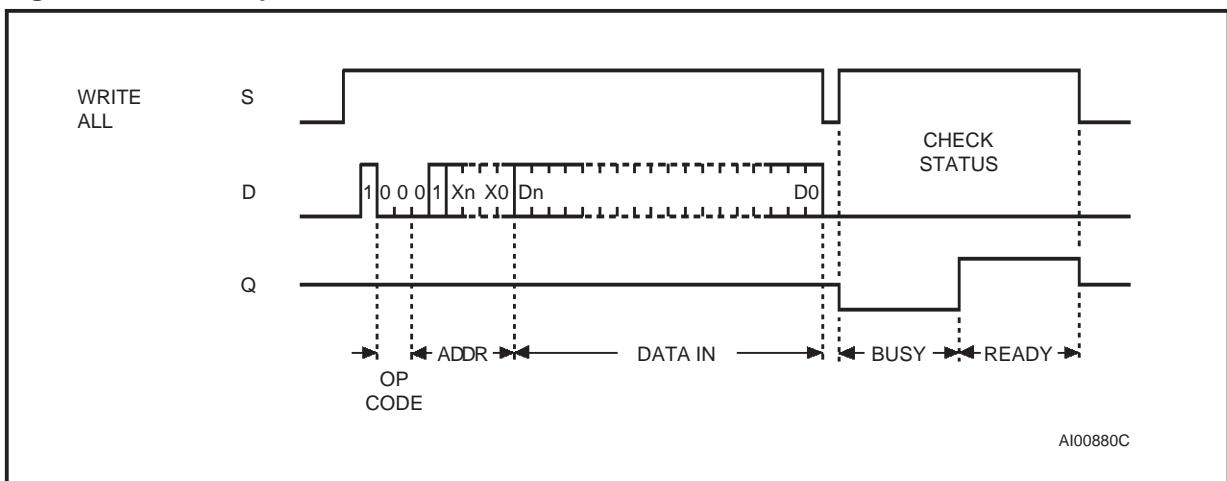
Note: Xn, Dn: Refer to Table 7a for the M93C06 and M93C46; to Table 7b for the M93C56 and M93C66; to Table 7c for the M93C76 and M93C86.

Figure 9. WRITE Sequence with One Clock Glitch

AI01395
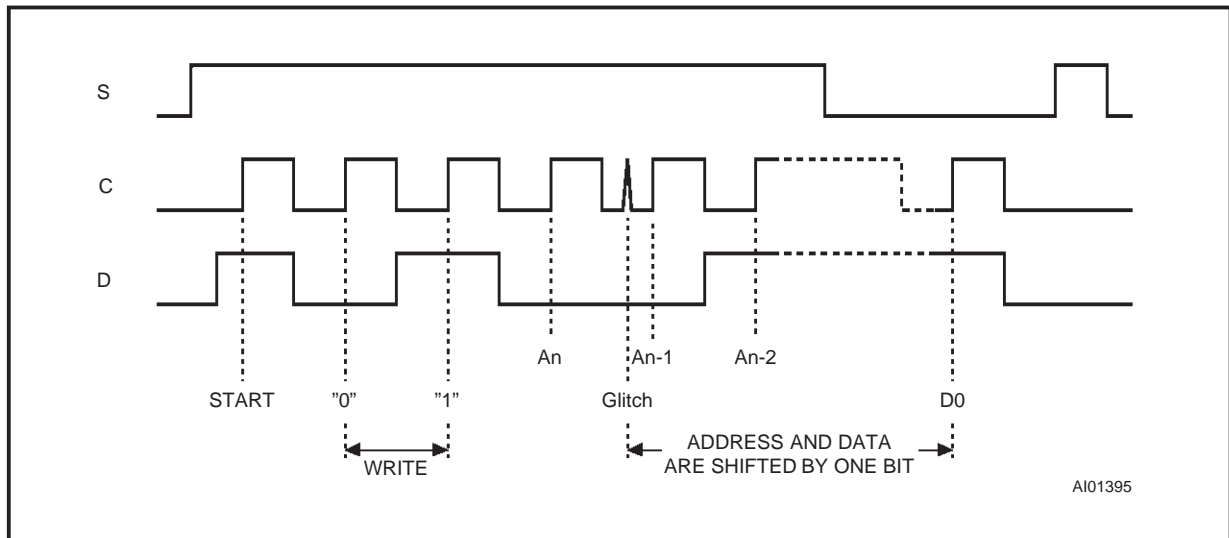
CLOCK PULSE COUNTER

The M93Cx6 offers a functional security block which filters glitches on the clock input (C), the clock pulse counter. In a normal environment, the M93Cx6 expects to receive the exact number of data bits on the D input (start bit, Op-Code, Address, Data); that is the exact amount of clock pulses on the C input.

In a noisy environment, the number of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the M93Cx6. In such a case, a part of the instruction can be delayed by one or more bits (see Figure 9), and may induce an erroneous write of data at an invalid address. The M93Cx6 has an on-chip counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal.
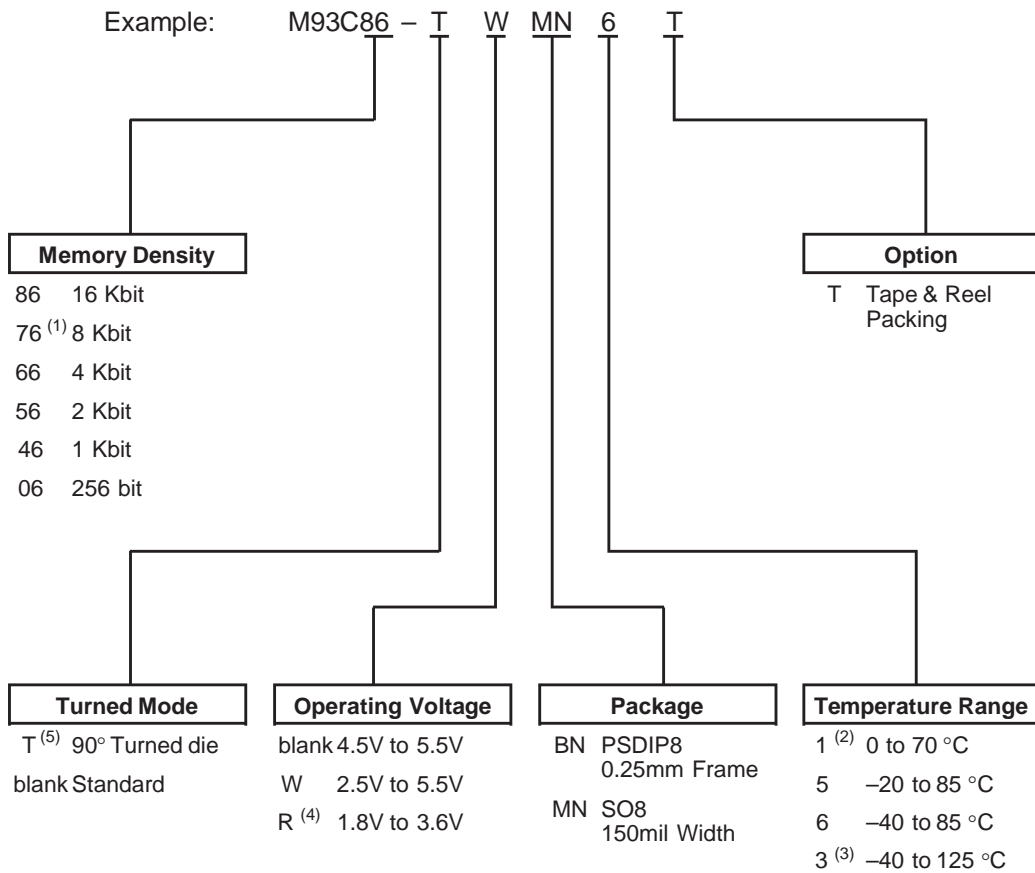
For the WRITE instructions with a M93C56 (or M93C66), the number of clock pulses incoming to the counter must be exactly 20 (with the organisation x8) from the Start bit to the falling edge of Chip

Select signal (1 Start bit + 2 Op-code bit + 9 Address bit + 8 Data bit = 20): if so, the M93C56 (or M93C66) executes the WRITE instruction; if the number of clock pulses is not equal to 20, the instruction will not be executed (and data will not be corrupted).

In the same way, when the organisation x16 is selected with the M93C56 (or M93C66), the number of clock pulses incoming to the counter must be exactly 27 (1 Start bit + 2 Op-code bit + 8 Address bit + 16 Data bit = 27) from the Start bit to the falling edge of Chip Select signal: if so, the M93C56 (or M93C66) executes the WRITE instruction; if the number of clock pulses is not equal to 27, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active on the WRITE, ERASE, ERAL and WRALL instructions.

In order to determine the exact number of clock pulses needed for all the M93Cx6 family on ERASE and WRITE instructions, refer to the Tables 7A, 7B and 7C, in the column: Requested Clock Cycles.

ORDERING INFORMATION SCHEME

Example: M93C86 – T W MN 6 T

Memory Density

86	16 Kbit
76 [1]	8 Kbit
66	4 Kbit
56	2 Kbit
46	1 Kbit
06	256 bit

Option

T	Tape & Reel Packing

Turned Mode

T [5]	90° Turned die
blank	Standard

Operating Voltage

blank	4.5V to 5.5V
W	2.5V to 5.5V
R [4]	1.8V to 3.6V

Package

BN	PSDIP8 0.25mm Frame
MN	SO8 150mil Width

Temperature Range

1 [2]	0 to 70 °C
5	−20 to 85 °C
6	−40 to 85 °C
3 [3]	−40 to 125 °C

Notes: 1. This is preliminary information on a new product now in development. Details are subject to change without notice.
2. Temperature range on request only.
3. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 1MHz only.
4. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.
5. Turned die option is not available for all devices. Please contact the STMicroelectronics Sales Office nearest to you.

Devices are shipped from the factory with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

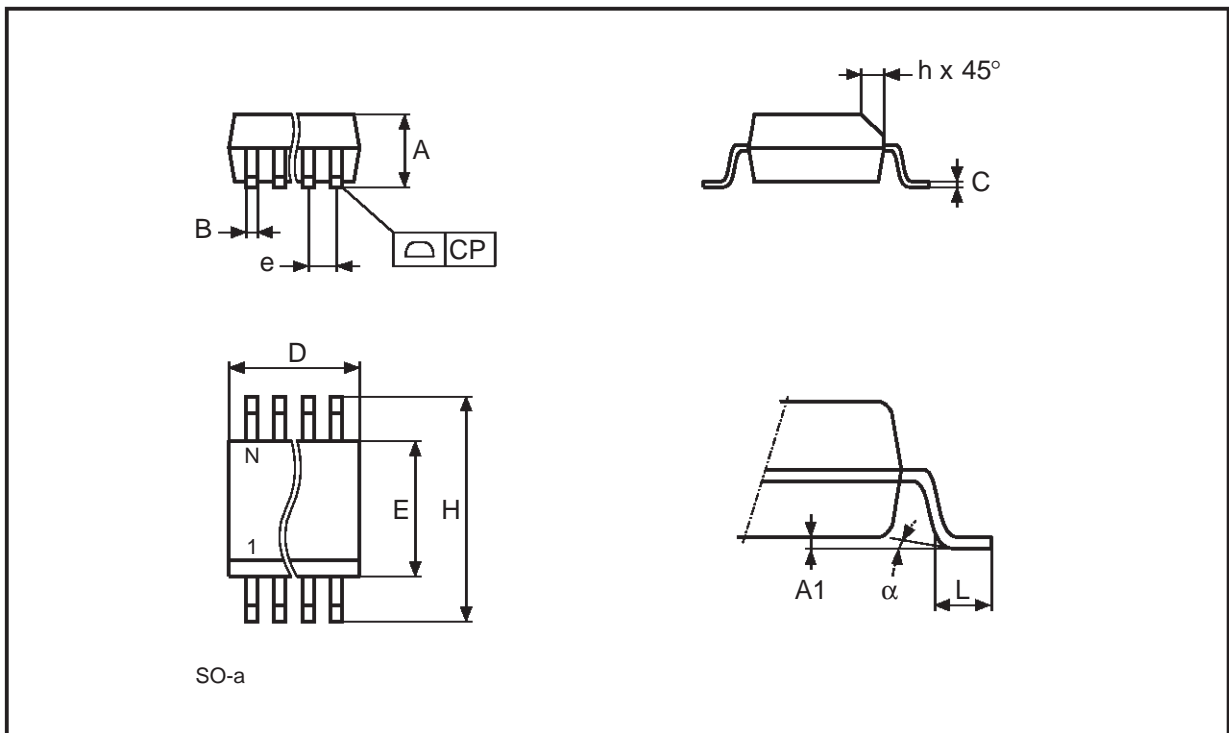## PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP-a
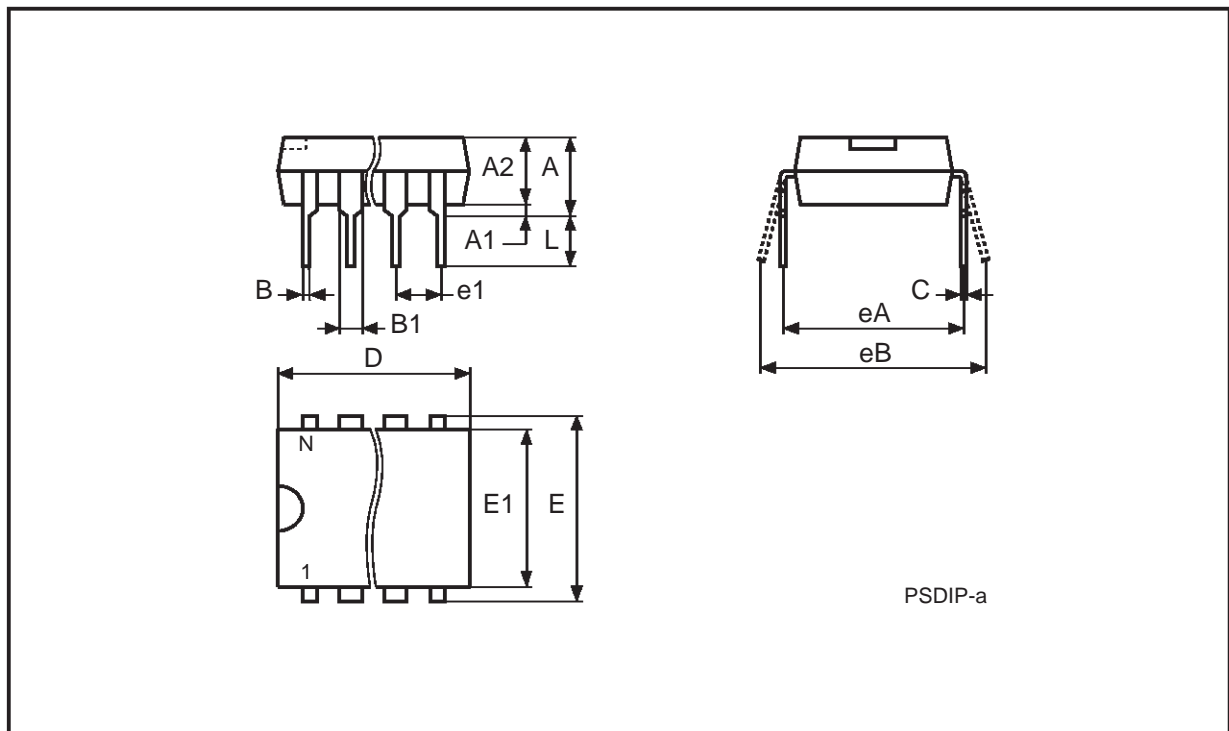
Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO-a

Drawing is not to scale