



M93S66, M93S56, M93S46

4K/2K/1K (x16) SERIAL MICROWIRE BUS EEPROM with BLOCK PROTECTION

PRELIMINARY DATA

- INDUSTRY STANDARD MICROWIRE BUS
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE ORGANIZATION by WORD (x16)
- WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
 - 4.5V to 5.5V for M93Sx6 version
 - 2.5V to 5.5V for M93Sx6-W version
 - 1.8V to 5.5V for M93Sx6-R version
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 words)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD and LATCH-UP PERFORMANCES

DESCRIPTION

This M93S46/S56/S66 specification covers a range of 4K/2K/1K bit serial EEPROM products respectively. In this text, products are referred to as M93Sx6. The M93Sx6 is an Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics' High Endurance Single Polysilicon CMOS technology.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

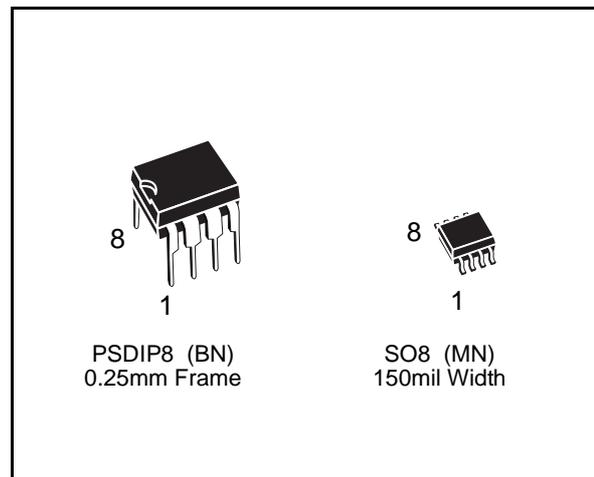


Figure 1. Logic Diagram

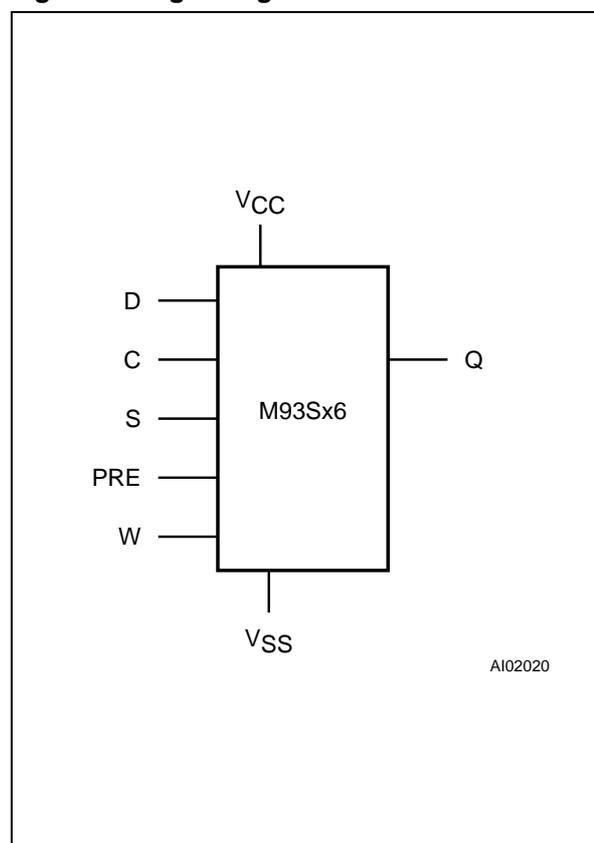


Figure 2A. DIP Pin Connections

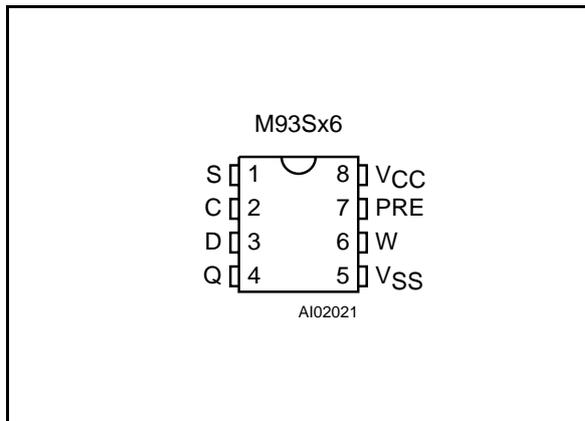


Figure 2B. SO Pin Connections

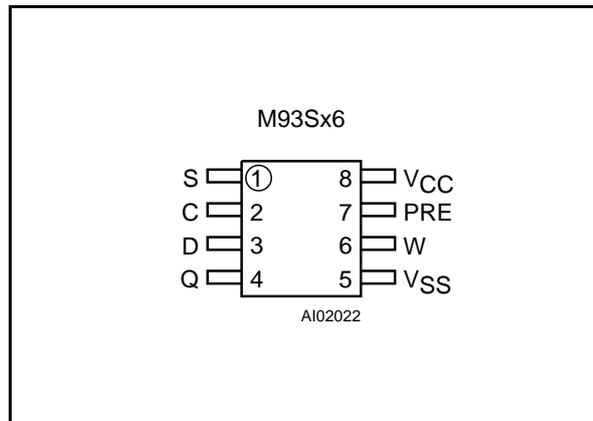


Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 125	°C
T _{STG}	Storage Temperature	-65 to 150	°C
T _{LEAD}	Lead Temperature, Soldering (SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V _{IO}	Input or Output Voltages (Q = V _{OH} or Hi-Z)	-0.3 to V _{CC} +0.5	V
V _{CC}	Supply Voltage	-0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ⁽²⁾	7000	V
	Electrostatic Discharge Voltage (Machine model) ⁽³⁾	1000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

- 2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
- 3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The M93Sx6 memory is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol. The M93Sx6 is specified at 5V ±10%, the M93Sx6-W specified at 2.5V to 5.5V and the M93Sx6-R specified at 1.8V to 5.5V.

The M93S66/S56/S46 memory is divided into 256/128/64 x16 bit words respectively. These memory devices are available in both PSDIP8 and SO8 package.

The M93Sx6 memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the

address of the first word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the M93Sx6 can output a sequential stream of data words. In this way, the memory can be read as a data stream from 16 to 4096 bits (for the M93S66), or continuously as the address counter automatically rolls over to '00' when the highest address is reached. Within the time required by a programming cycle (t_w), up to 4 words may be written with help of the Page Write instruction. the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Table 5B. DC Characteristics for M93Sx6-W version
 (T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}		±1	μA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC} , Q in Hi-Z		±1	μA
I _{CC}	Supply Current (Read)	V _{CC} = 5V, S = V _{IH} , f = 1 MHz		1	mA
		V _{CC} = 2.5V, S = V _{IH} , f = 1 MHz		0.75	mA
	Supply Current (Write, Erase)	V _{CC} = 5V, S = V _{IH} , f = 1 MHz		1.5	mA
		V _{CC} = 2.5V, S = V _{IH} , f = 1 MHz		1	mA
I _{CC1}	Supply Current (Standby)	V _{CC} = 5V, S = V _{SS} , C = V _{SS} , W = V _{SS} or V _{CC} , PRE = V _{SS} or V _{CC}		40	μA
		V _{CC} = 2.5V, S = V _{SS} , C = V _{SS} , W = V _{SS} or V _{CC} , PRE = V _{SS} or V _{CC}		10	μA
V _{IL}	Input Low Voltage (D, C, S, W, PRE)		-0.3	0.25 V _{CC}	V
V _{IH}	Input High Voltage (D, C, S, W, PRE)		0.7 V _{CC}	V _{CC} + 1	V
V _{OL}	Output Low Voltage (Q)	V _{CC} = 5V, I _{OL} = 2.1mA		0.2 V _{CC}	V
		V _{CC} < 4.5V, I _{OL} = 100μA		0.2	V
V _{OH}	Output High Voltage (Q)	V _{CC} = 5V, I _{OH} = -400μA	0.8 V _{CC}		V
		V _{CC} < 4.5V, I _{OH} = -100μA	V _{CC} - 0.2		V

DESCRIPTION (cont'd)

Within the memory, a user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programming bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time

into one of the 256/128/64 words of the M93S46/S56/S66 respectively, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when Chip Select (S) is driven High.

An internal feature of the M93Sx6 provides Power-on Data Protection by inhibiting any operation when the Supply is too low. The design of the M93Sx6 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

Table 5C. DC Characteristics for M93Sx6-R version
 ($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 1.8\text{V}$ to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{LO}	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		± 1	μA
I_{CC}	Supply Current (Read)	$V_{CC} = 5\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		1	mA
		$V_{CC} = 2.5\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		0.75	mA
		$V_{CC} = 1.8\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		0.75	mA
	Supply Current (Write, Erase)	$V_{CC} = 5\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		1.5	mA
		$V_{CC} = 2.5\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		1	mA
		$V_{CC} = 1.8\text{V}$, $S = V_{IH}$, $f = 1\text{ MHz}$		1	mA
I_{CC1}	Supply Current (Standby)	$V_{CC} = 5\text{V}$, $S = V_{SS}$, $C = V_{SS}$, $W = V_{SS}$ or V_{CC} , $PRE = V_{SS}$ or V_{CC}		40	μA
		$V_{CC} = 2.5\text{V}$, $S = V_{SS}$, $C = V_{SS}$, $W = V_{SS}$ or V_{CC} , $PRE = V_{SS}$ or V_{CC}		10	μA
		$V_{CC} = 1.8\text{V}$, $S = V_{SS}$, $C = V_{SS}$, $W = V_{SS}$ or V_{CC} , $PRE = V_{SS}$ or V_{CC}		5	μA
V_{IL}	Input Low Voltage (D, C, S, W, PRE)		-0.3	$0.3 V_{CC}$	V
V_{IH}	Input High Voltage (D, C, S, W, PRE)		$0.7 V_{CC}$	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage (Q)	$V_{CC} = 5\text{V}$, $I_{OL} = 2.1\text{mA}$		$0.2 V_{CC}$	V
		$V_{CC} < 4.5\text{V}$, $I_{OL} = 100\mu\text{A}$		0.2	V
V_{OH}	Output High Voltage (Q)	$V_{CC} = 5\text{V}$, $I_{OH} = -400\mu\text{A}$	$0.8 V_{CC}$		V
		$V_{CC} < 4.5\text{V}$, $I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V

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Table 6A. AC Characteristics for M93Sx6, M93Sx6-W, M93Sx6-R versions
($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 4.5\text{V}$ to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	Note 3		500	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_w	t_{WP}	Erase/Write Cycle time			10	ms
f_c	f_{SK}	Clock Frequency	V_{CC} min	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of t_{SLSH} between consecutive instructions cycles.
 2. The Clock frequency specification calls for a minimum clock period of $1/f_c$, therefore the sum of the timings $t_{CHCL}+t_{CLCH}$ must be greater or equal to $1/f_c$. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns for $f_c=1\text{MHz}$.
 3. Characterized but not 100% tested.

Table 6B. AC Characteristics for M93Sx6-W, M93Sx6-R versions
 ($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 2.5\text{V}$)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		100		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		50		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		50		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			250	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			250	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			250	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	Note 3		200	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	200		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	200		ns
t_w	t_{WP}	Erase/Write Cycle time			10	ms
f_c	f_{SK}	Clock Frequency	V_{CC} min	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of t_{SLSH} between consecutive instructions cycles.
 2. The Clock frequency specification calls for a minimum clock period of $1/f_c$, therefore the sum of the timings $t_{CHCL}+t_{CLCH}$ must be greater or equal to $1/f_c$. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns for $f_c=1\text{MHz}$.
 3. Characterized but not 100% tested.

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Table 6C. AC Characteristics for M93Sx6-R version
($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 1.8\text{V}$)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		100		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	Note 3		300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_w	t_{WP}	Erase/Write Cycle time			10	ms
f_c	f_{SK}	Clock Frequency	V_{CC} min	0	1	MHz

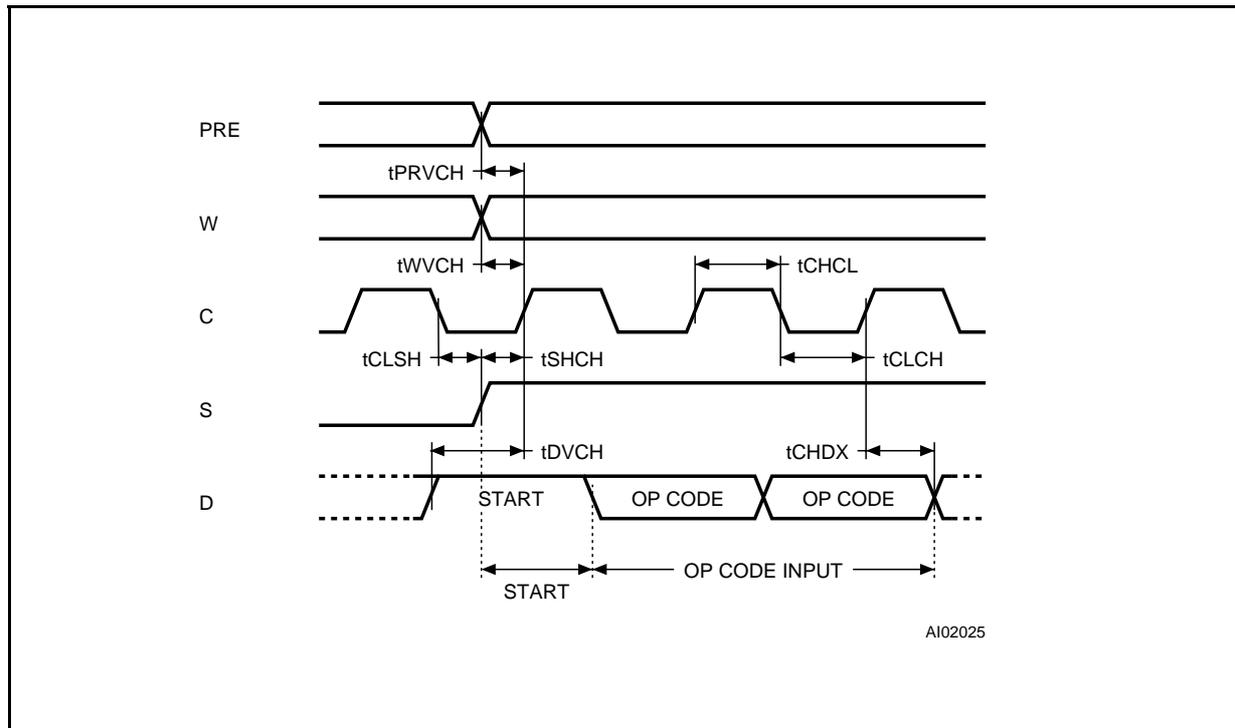
Notes: 1. Chip Select must be brought low for a minimum of t_{SLSH} between consecutive instructions cycles.
 2. The Clock frequency specification calls for a minimum clock period of $1/f_c$, therefore the sum of the timings $t_{CHCL}+t_{CLCH}$ must be greater or equal to $1/f_c$. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns for $f_c=1\text{MHz}$.
 3. Characterized but not 100% tested.

Table 6D. AC Characteristics for M93Sx6 version
 ($T_A = -40$ to 125°C ; $V_{CC} = 4.5\text{V}$ to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	Note 3		300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_w	t_{WP}	Erase/Write Cycle time			10	ms
f_c	f_{SK}	Clock Frequency	V_{CC} min	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of t_{SLSH} between consecutive instructions cycles.
 2. The Clock frequency specification calls for a minimum clock period of $1/f_c$, therefore the sum of the timings $t_{CHCL}+t_{CLCH}$ must be greater or equal to $1/f_c$. For example, if t_{CHCL} is 250ns, then t_{CLCH} must be at least 750ns for $f_c=1\text{MHz}$.
 3. Characterized but not 100% tested.

Figure 4. Synchronous Timing, Start and Op-Code Input



POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power-up and power-down, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode.

- At Power-up and Power-down, the device must NOT be selected (that is, the S input must be driven low) until the supply voltage reaches the operating value V_{CC} specified in the AC and DC tables.

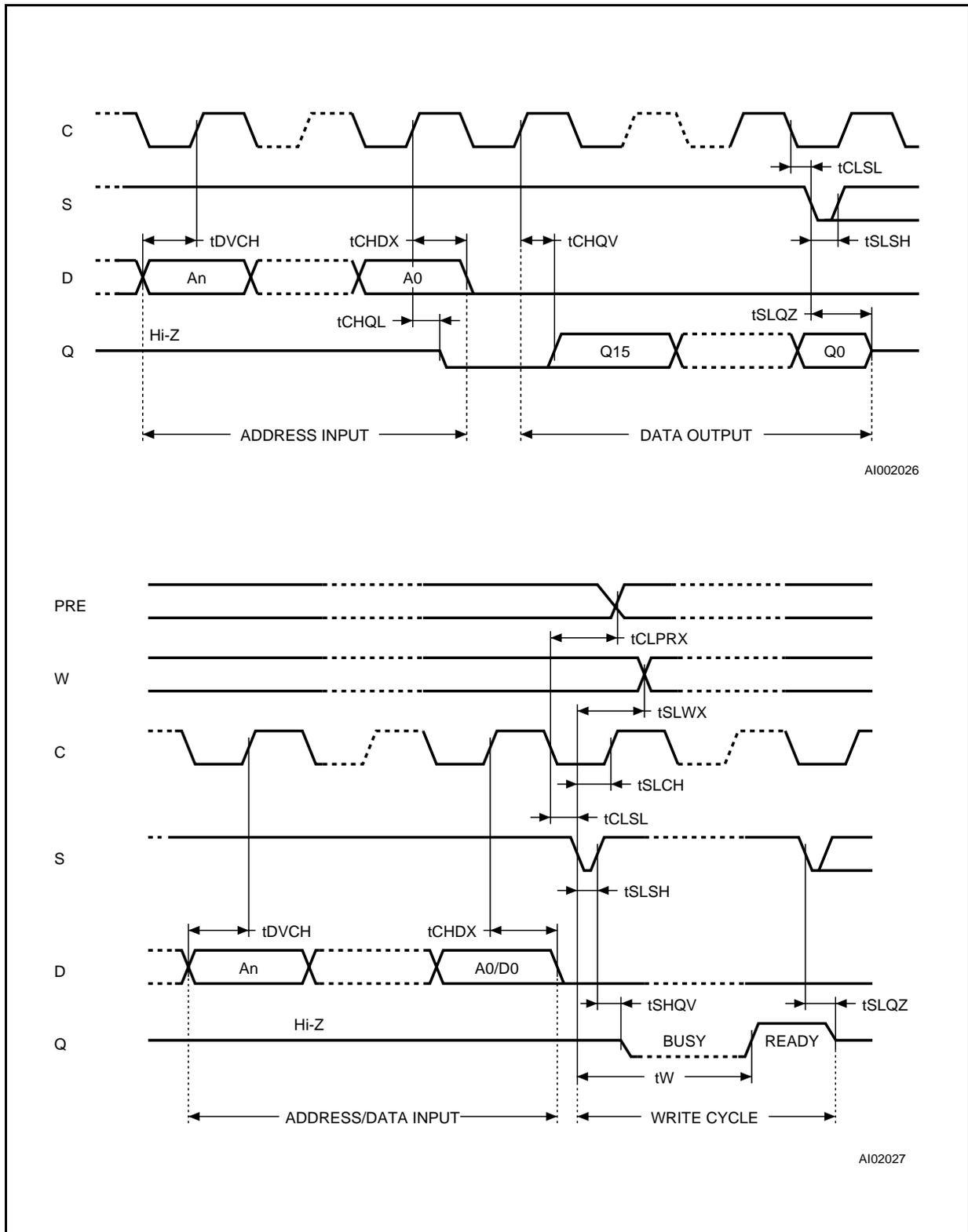
- When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

Below the Power On Reset threshold voltage, the M93Sx6 is in reset mode.

For the M93Sx6 specified at 5V, the POR threshold voltage is around 3V.

For all the other M93Sx6 specified at low V_{CC} (with -W and -R V_{CC} range options), the POR threshold voltage is around 1.5V.

Figure 5. Synchronous Timing, Read or Write



INSTRUCTIONS

The M93S66/S56/S46 have eleven instructions, as shown in Table 7. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the clock C is low). After the device is selected, the internal logic waits for the start bit, which define the beginning of the instruction bit stream. The start bit is the first '1' read on D input during the rising edge of the clock C. Following the start bit, the op-codes of the instructions are made up of the 2 following bits. Notice that

some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is then followed by the address of the word to be accessed.

For the M93S46, the address is made up of 6 bits (See Table 7a). For the M93S56 and M93S66, the address is made up of 8 bits (See Table 7b).

The M93Sx6 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Table 7A. Instruction Set for the M93S46

Instr.	Description	W	PRE	Start Bit	Op-Code	Address ⁽¹⁾	Data	Req. Clock Cycles	Additional Information
READ	Read Data from Memory	X	'0'	'1'	10	A5-A0	Q15-Q0		
WRITE	Write Data to Memory	'1'	'0'	'1'	01	A5-A0	D15-D0	25	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	'1'	11	A5-A0	N x D15-D0	9 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	'1'	00	01XXXX	D15-D0	25	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	'1'	00	11XXXX		9	
WDS	Write Disable	X	'0'	'1'	00	00XXXX		9	
PRREAD	Protect Register Read	X	'1'	'1'	10	XXXXXX	Q5-Q0 + Flag		Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	'1'	01	A5-A0		9	Data above specified address A5-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	'1'	11	111111		9	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	'1'	00	11XXXX		9	
PRDS	Protect Register Disable	'1'	'1'	'1'	00	000000		9	OTP bit is set permanently

Note: 1. X = don't care bit.

Table 7B. Instruction Set for the M93S56 and M93S66

Instr.	Description	W	PRE	Start Bit	Op-Code	Address ^(1,2)	Data	Req. Clock Cycles	Additional Information
READ	Read Data from Memory	X	'0'	'1'	10	A7-A0	Q15-Q0		
WRITE	Write Data to Memory	'1'	'0'	'1'	01	A7-A0	D15-D0	27	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	'1'	11	A7-A0	N x D15-D0	11 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	'1'	00	01XXXXXX	D15-D0	27	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	'1'	00	11XXXXXX		11	
WDS	Write Disable	X	'0'	'1'	00	00XXXXXX		11	
PRREAD	Protect Register Read	X	'1'	'1'	10	XXXXXXXX	Q7-Q0 + Flag		Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	'1'	01	A7-A0		11	Data above specified address A7-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	'1'	11	11111111		11	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	'1'	00	11XXXXXX		11	
PRDS	Protect Register Disable	'1'	'1'	'1'	00	00000000		11	OTP bit is set permanently

Notes: 1. X = don't care bit.

2. Address bit A7 is not decoded by the M93S56.

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The M93Sx6 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed. The Write Disable instruction (WDS) disables the execution of the following Write instructions and the internal programming cycle cannot run.

When power is first applied, the M93Sx6 is in Write Disable mode and all Write instructions are inhibited. When the WEN instruction is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or V_{CC} falls below the Power-On Reset threshold Voltage.

To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle. The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is composed of the Start bit plus the Op-Code followed by the address and the 16 data bits to be written. The Write Enable signal (W) must be held high during the Write instruction. Data input (D) is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. This is really important as, if S is brought low before or after this specific frame window, the addressed location will not be programmed, providing that the address is NOT in the protected area.

If the M93Sx6 is still performing the write cycle, the Busy signal ($Q = 0$) will be returned if the Chip Select input (S) is driven high after the t_{SLSH} delay, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal ($Q = 1$) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle).

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the PAWRITE instruction. Input address and data are sampled on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits (Ax-A2) remaining unchanged. Users must take care by software to ensure that the last word address has the same upper order address bits as the initial address transmitted to avoid address roll-over. After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C) in order to start the self-timed programming cycle. This is really important as, if S is brought low before or after this specific frame window, the addressed locations will not be programmed. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the M93Sx6 is still performing the programming cycle, the Busy signal ($Q = 0$) will be returned if the Chip Select input (S) is driven high, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal ($Q = 1$) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write All instruction. Input address and data are sampled on the Low to High transition of the clock. If the M93Sx6 is still performing the write cycle, the Busy signal ($Q = 0$) will be returned if the Chip Select input (S) is driven high after the t_{SLSH} delay, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal ($Q = 1$) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, WRALL or PAWRITE instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the M93Sx6 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The M93Sx6 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the memory protection through the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS. this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable) and W (Write Enable).

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction.

As in the Read instruction a dummy '0' bit is output first. Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN instruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable

(W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

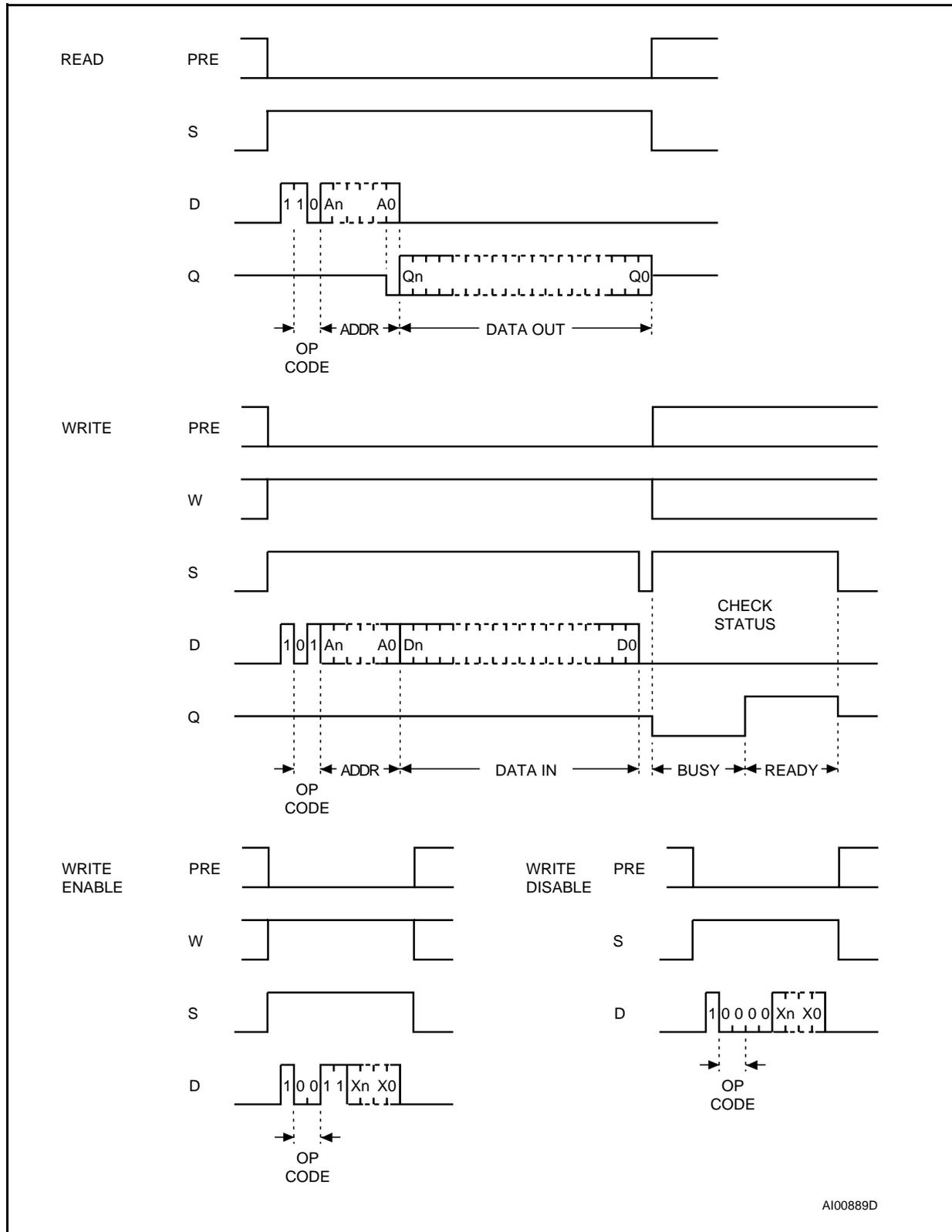
Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q). When the OTP bit is not set, the Busy status appear on the Data output (Q).

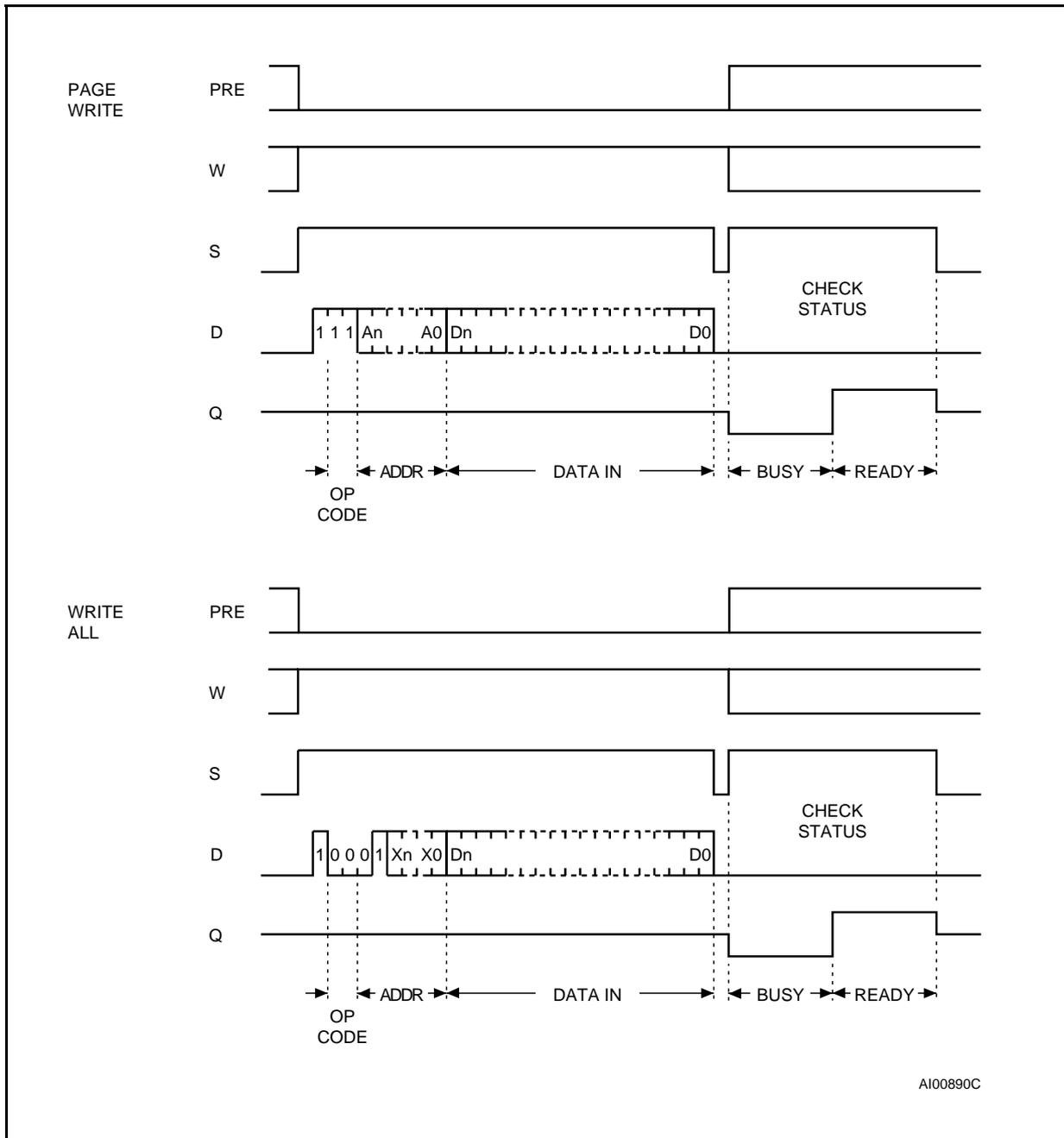
Note: A PREN instruction must immediately precede the PRDS instruction.

Figure 6. READ, WRITE, WEN, WDS Sequences



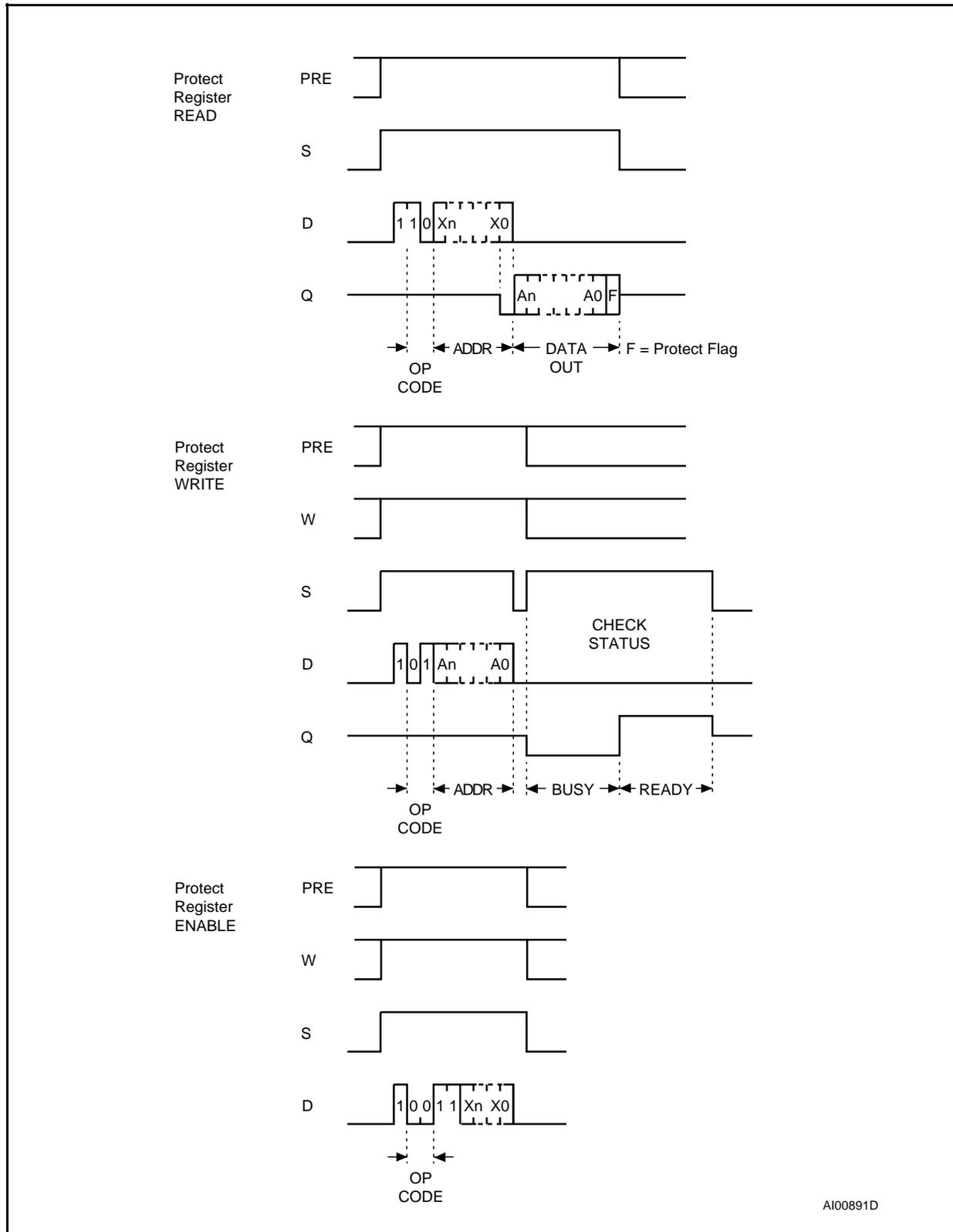
Notes: 1. An - Xn - Qn - Dn: Refer to Table 7a for the M93S46.
 2. An - Xn - Qn - Dn: Refer to Table 7b for the M93S56 and M93S66.

Figure 7. PAWRITE, WRALL Sequences



Notes: 1. An - Xn - Dn: Refer to Table 7a for the M93S46.
 2. An - Xn - Dn: Refer to Table 7b for the M93S56 and M93S66.

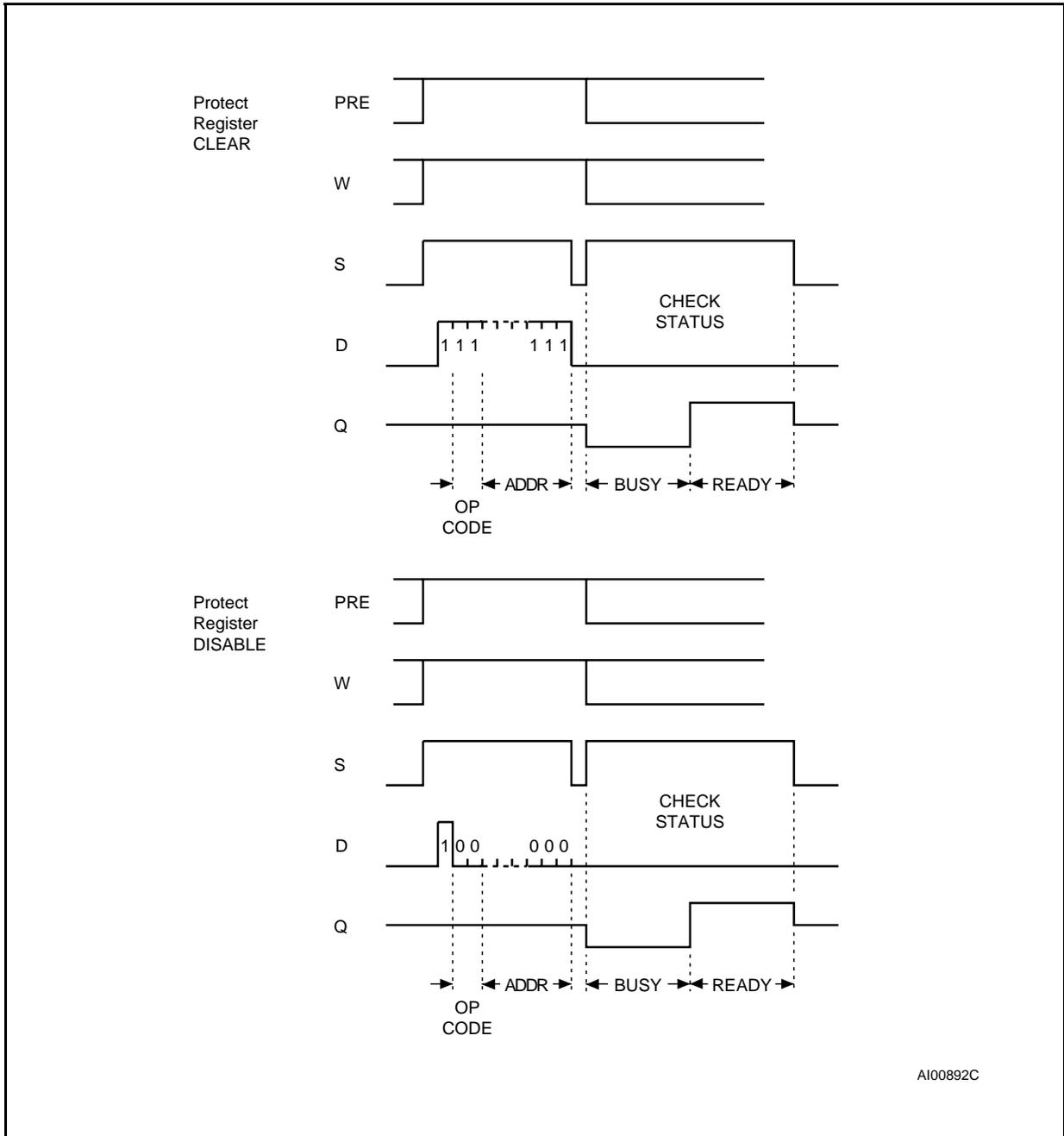
Figure 8. PRRREAD, PRWRITE, PREN Sequences



AI00891D

Notes: 1. A_n - X_n - D_n: Refer to Table 7a for the M93S46.
 2. A_n - X_n - D_n: Refer to Table 7b for the M93S56 and M93S66.

Figure 9. PRCLEAR, PRDS Sequences



AI00892C

Notes: 1. An - Xn - Dn: Refer to Table 7a for the M93S46.
 2. An - Xn - Dn: Refer to Table 7b for the M93S56 and M93S66.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the STMicroelectronics application note AN394 "MICROWIRE EEPROM Common I/O Operation".

CLOCK PULSE COUNTER

The M93Sx6 offers a functional security filtering glitches on the clock input (C), the clock pulse counter.

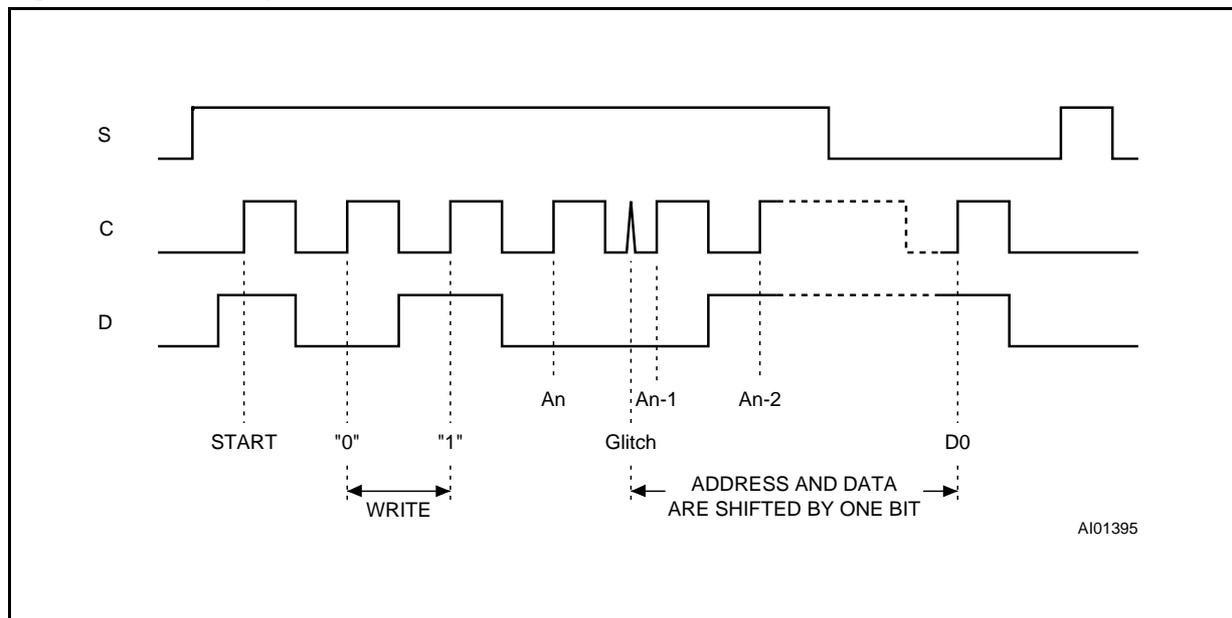
In a normal environment, the M93Sx6 expects to receive the exact amount of data on the D input (start bit, Op-Code, Address, Data), that is the exact amount of clock pulses on the C input. In a noisy environment, the number of pulses received (on the clock input C) may be greater than the clock

pulses delivered by the Master (Microcontroller) driving the M93Sx6. In such a case, a part of the instruction is delayed by one bit (see Figure 10), and it may induce an erroneous write of data at a wrong address. The M93Sx6 has an on-chip counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal.

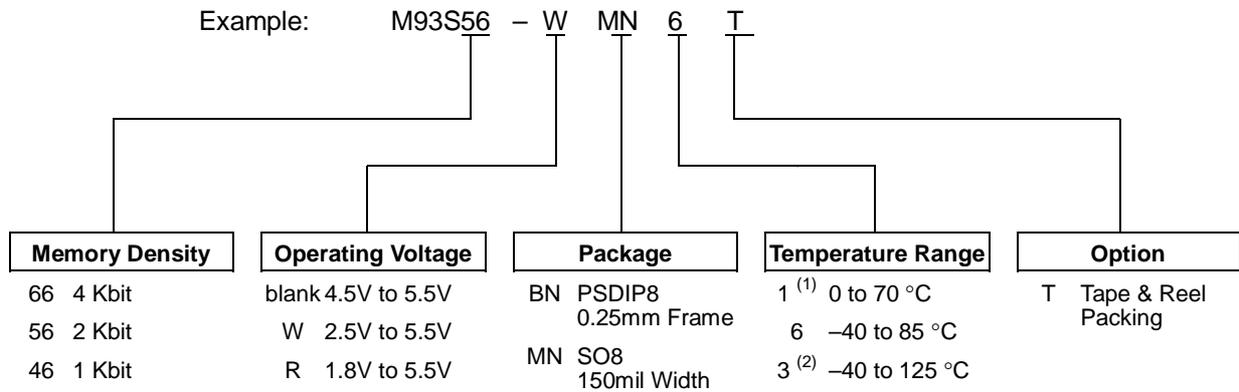
For the WRITE instructions with a M93S56 (or M93S66), the number of clock pulses incoming to the counter must be exactly 27 from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 Op-code bit + 8 Address bit + 16 Data bit = 27): if so, the M93S56 (or M93S66) executes the WRITE instruction. If the number of clock pulses is not equal to 27, the instruction will not be executed (and data will not be corrupted).

The clock pulse counter is active on WRITE, PAWRITE, WRALL, PRWRITE and PRCLEAR instructions. In order to determine the exact number of clock pulses needed for all the M93Sx6 on WRITE instructions, refer to Tables 7a and 7b, in the column: Requested Clock Cycles.

Figure 10. Write Sequence with One Clock Glitch



ORDERING INFORMATION SCHEME

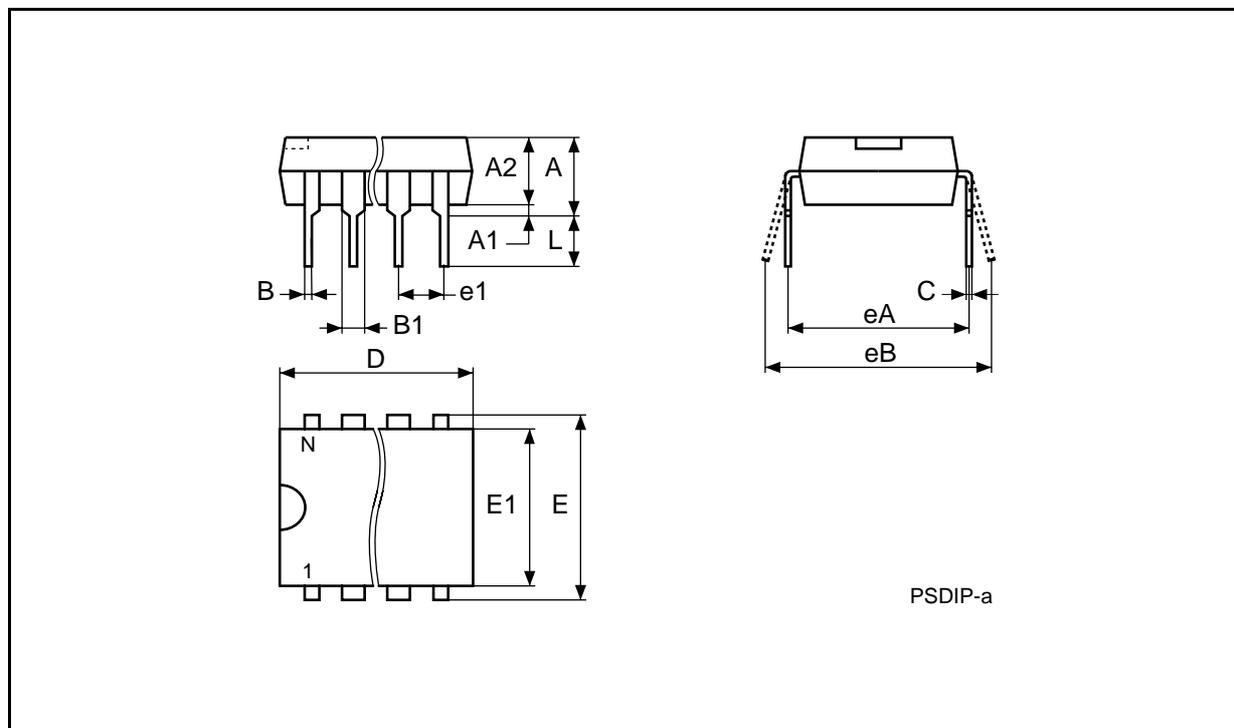


Notes: 1. Temperature range on request only.
 2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 1MHz only.

Devices are shipped from the factory with the memory content set at all "1's" (FFFFh).
 For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

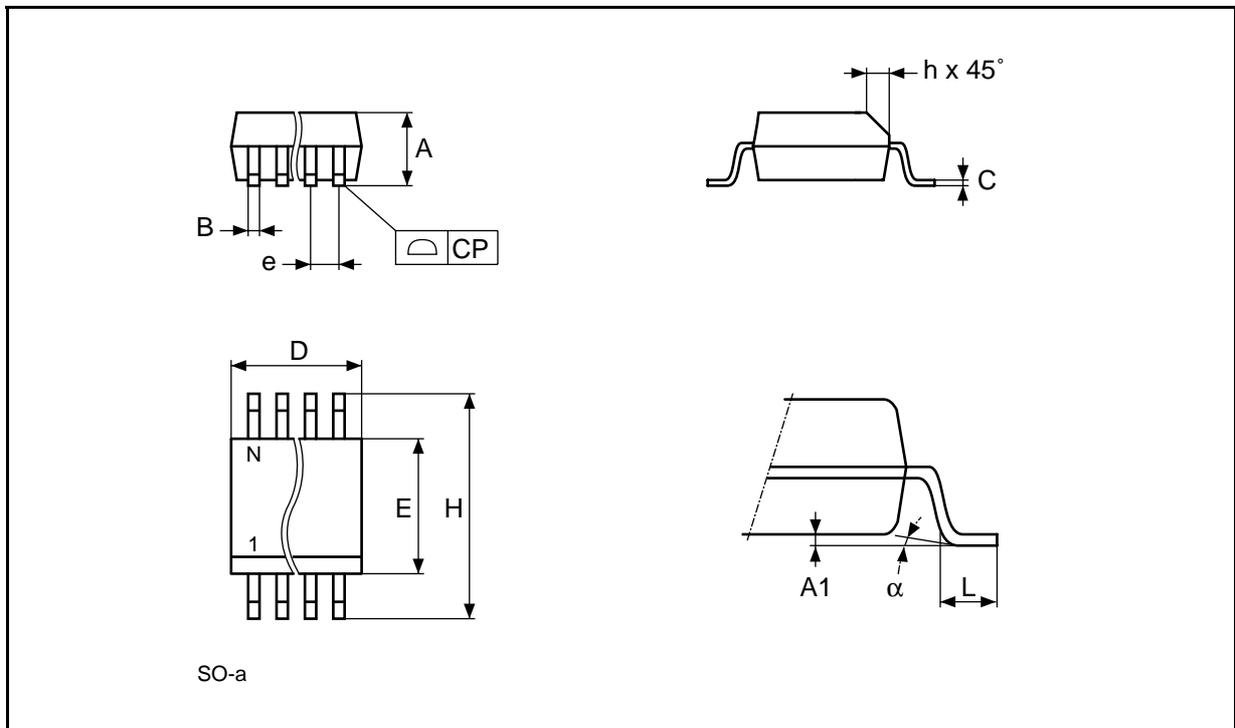
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	



Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



Drawing is not to scale

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