MA28139

OBDH Bus Terminal

Replaces January 2000 version, DS3592-6.0

DS3592-6.1 July 2002

The OBT ASIC will interface any user to the ESA On Board Data Handling bus. Developed under ESA Contract, it conforms to ESA OBDH, Digital Bus Interface and Internal User Bus Standards.

The OBT has 2 separate functions. The first is a 5 channel modem which, on the bus side, provides the digital waveforms necessary to operate the Litton Bus drivers, and receives the outputs of the Litton bus detectors. On the user side, it provides an input / output at Digital Bus Interface level. The second function, internally coupled to the first, provides a multiplexing / demultiplexing function of the DBI signals down to Internal User Bus levels and vectored 16 bit serial register read and write commands (see section 7.2 of ESA standard TTC-B-01). In effect, the second function of the OBT provides the core of an RTU.

The Interrogation and Response bus data streams of the two functions may be either coupled together (in RT mode) or isolated (in CT mode). The device may hence be used as a modem only, an RTU kernel only or as a combined modem and RTU kernel. In RT mode, the Interrogation bus data stream can be observed and the Response bus data from associated devices, such as an MA28138 Remote Bus Interface, can be combined with that from the RTU kernel before being used by the modem circuits to modulate the Response bus. Bi-directional access to the Block Transfer bus is provided in either mode.

When used to interface a central terminal to the OBDH bus, the OBT should be continuously clocked in order to output timing to all users on the I-bus as dummy interrogations from the CT. Commands and telemetry are normally sent on the I and BT busses whilst responses and telemetry normally return on the R and BT busses.

FEATURES

- Radiation Hard
- Low Power Consumption
- Single CMOS-SOS ASIC Implementation
- Latch-up Free
- High SEU Immunity
- Fully Compliant with ESA OBDH, IUB, DBI and RBI Specification
- Contains OBDH Bus Modem and RTU Kernel
- Supports Bi-directional Data Transfer on Response and Block Transfer Bus

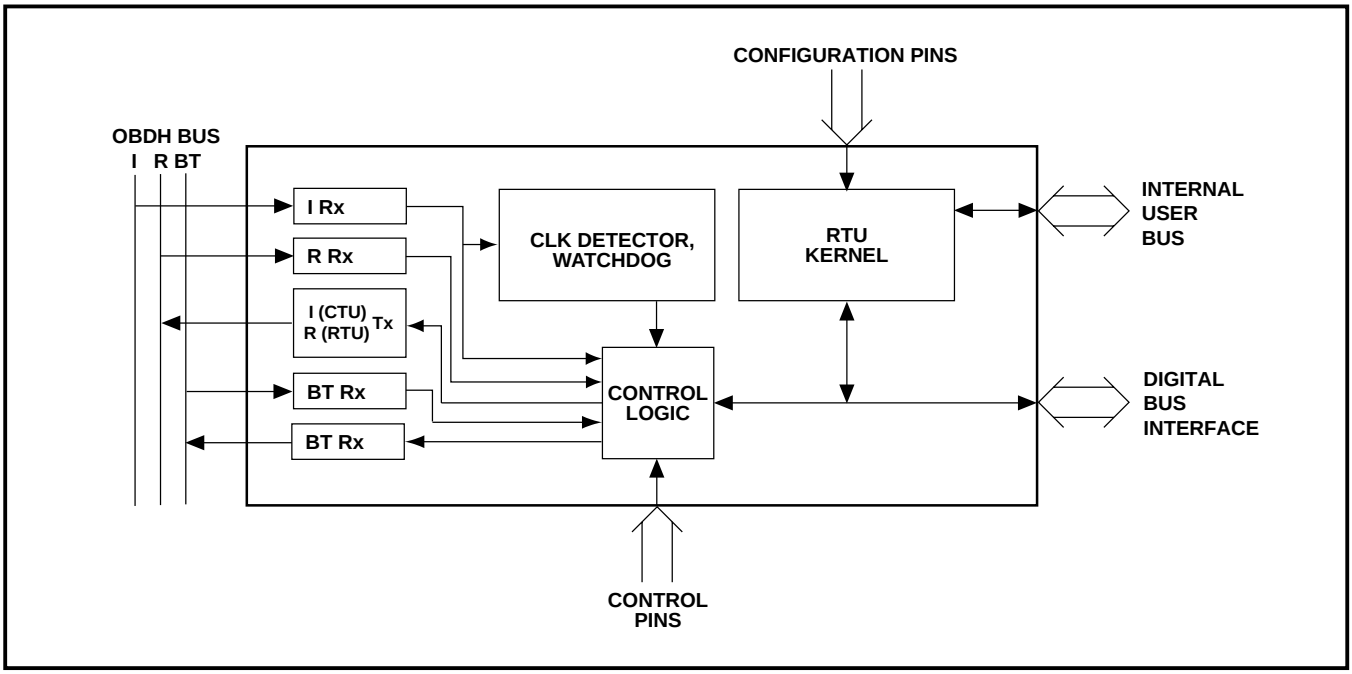


Figure 1: Block Diagram

APPLICATION

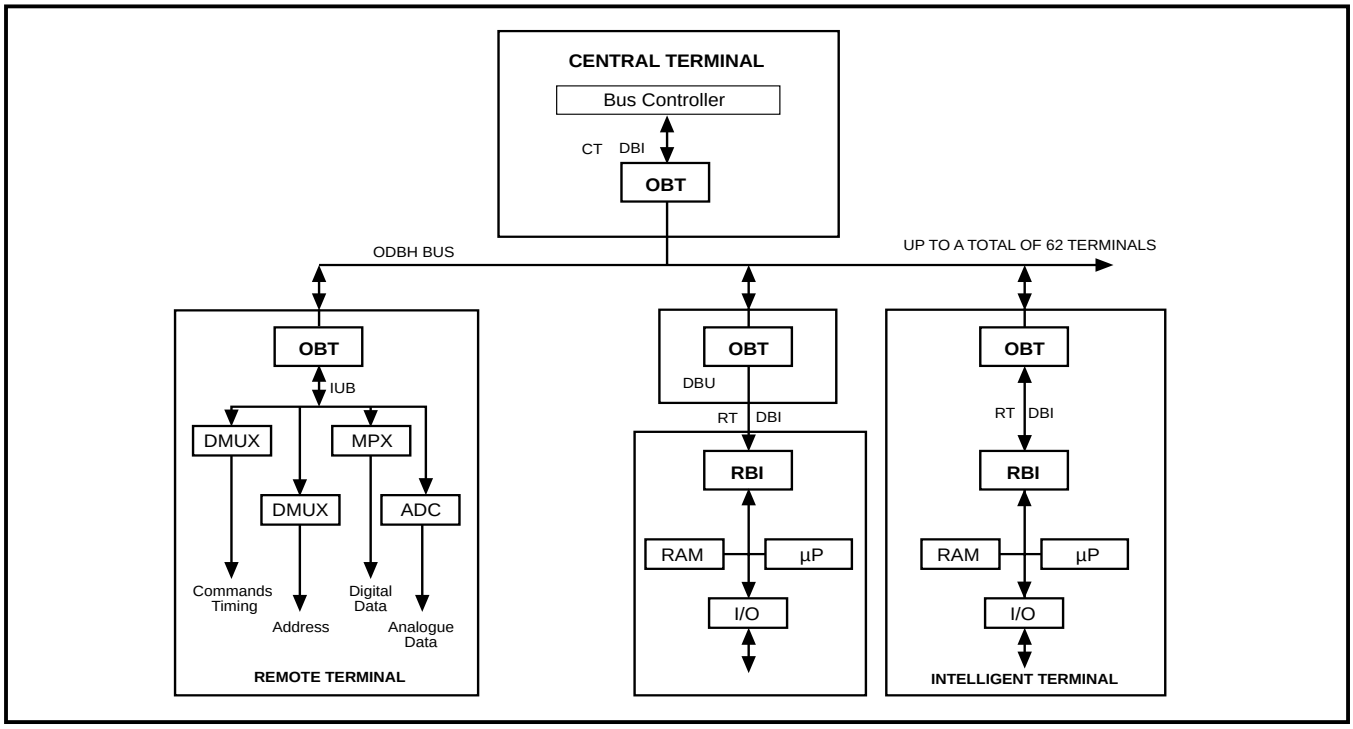


Figure 2: Application

PAYLOAD INTERFACES

The OBT converts the OBDH bus to an Internal User Bus, and a Digital Bus Interface. The OBT can connect OBDH to existing ESA standard payload interfaces such as the MSS PIU (payload interface unit), ICU (intelligent control unit), SBC (single board MIL-STD-1750 computer) or FTC (fault tolerant computer).

The OBT and analogue components/transformers can be integrated in the PIU, ICU, SBC, etc.

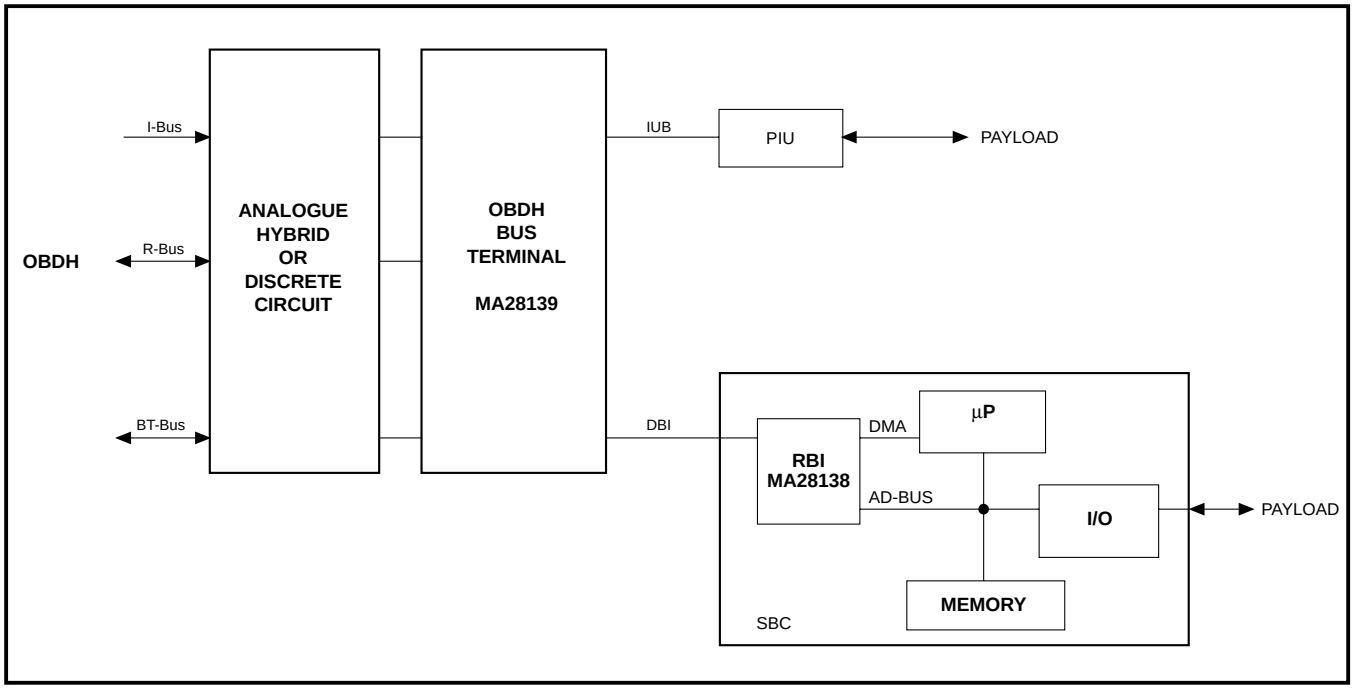


Figure 3: Payload Interface

FUNCTIONAL DESCRIPTION

In RT mode, power up resets the OBT and causes it to deselect both busses. Two watchdog counters monitor the Nominal l-bus and the Redundant l-bus. If either bus becomes active, that bus will be selected. If the selected bus stops, the OBT watchdog times out and resets both the OBT and the user. If both busses become active, the Nominal bus will be selected in preference to the Redundant one. A change in bus selection will always result in the OBT and the user being reset. Responses from the user are always returned on the selected bus. Setting 'SIMUL' high causes both BATs to drive both the Nominal and the Redundant busses irrespective of the current bus selection. The time-out period may be set to any desired number of bits by varying the 'LOSC' frequency. The OBT derives all timing from, and is synchronous with, the selected l-bus. The OBT demodulates the l-bus to the DBI and decodes commands to the IUB.

The CTpRTn mode pin causes the modem circuits and the RTU Kernel to be either cascade or isolated. If CTpRTn is low (RT mode), the RIRSYNC, CLK, DATA and VAL signals are routed to the RTU Kernel and the associated pins act as outputs; responses from the RTU Kernel are ORed with those from the external RRTDATA and RRTEN inputs and can be independently monitored on the DATARRT and ENRRT pins. In this mode any reset caused by the Clock Detector watchdogs is also combined with the power up reset input.

If CTpRTn is high (CT mode), the modem and RTU Kernel functions are isolated to permit the device to be used as either a modem within the CTU or an RTU Kernel interfacing to an external modem where the RIRSYNC, CLK, DATA and VAL pins act as inputs. The right-hand multiplexer bank is switched to the upper position so that the CT drives the OBDH via the CIT and CBT (if used) pins and receives responses/telemetry via the CRR and CBR (if used) pins. Note: in CT mode, BAT1 must be connected to the l-busses.

In RT mode, the CITSEL, MOD, CLK, SYNC and INV pins are disabled and the clocks are supplied by the l-bus BAR in response to the selected bus. In CT mode, the Clock Detector is functional and drives the TIMEOUTn pin but is unable to cause internal reset on time-out; in this mode the CT must supply all clocks and select the operational bus.

The changes depending upon selection of RT mode or CT mode with the CTpRTn pin are defined in the table below:

Functional Signal	**CT Mode Source (CTpRTn = '1')**	**RT Mode Source (CTpRTn = '0')**
BAT1, 2 modulation clock	CITMOD input pin	Recovered R2F
BAT1, 2 data clock	CITCLK input pin	Recovered RIRCLK
BAT1 data input	RRTDATA input pin	RRTDATA OR DATARRT (RTU Kernel)
BAT1 tx enable	'1'	RRTEN OR DATAEN (RTU Kernel)
BAT1 sync code tx enable	CITSYNC input pin	'0'
BAT1 bit invalidate tx enable	CITINV input Pin	'0'
BAT1, 2 bus selection	CITSEL and SIMUL input pins	Detected active bus and SIMUL input pin
BAT2 data input	RBTDATA input Pin	RBTDATA input pin
BAT2 tx enable	RBTEN input pin	RBTEN input pin
BAT1, 2, BAR1, 2, 3 reset	MRSTn input pin	TIMEOUTn AND MRSTn input pin
RIRSYNC, CLK, DATA, VAL pin direction	outputs	inputs
BAT/BAR and RTU Kernel coupling	separated	coupled

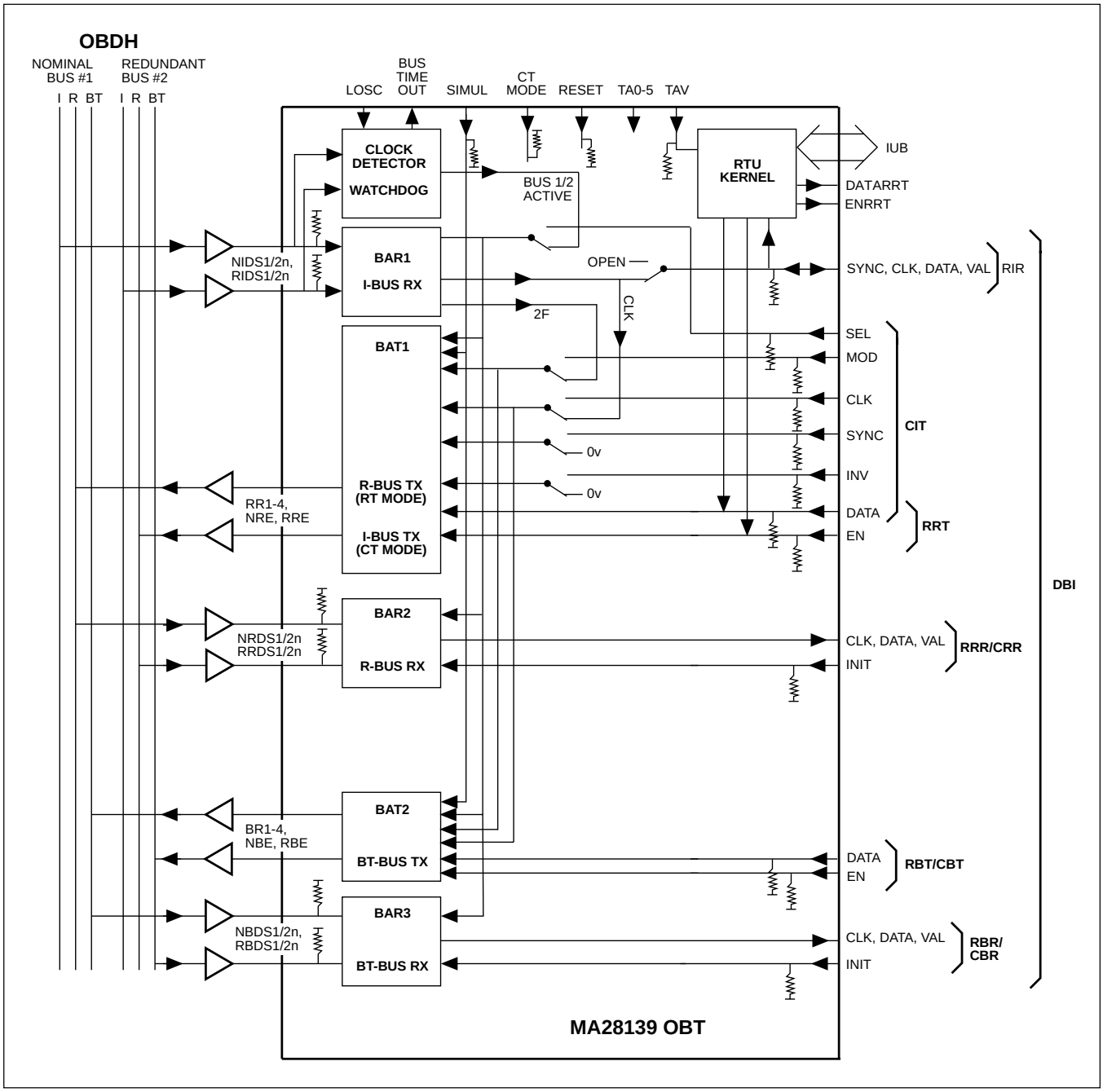
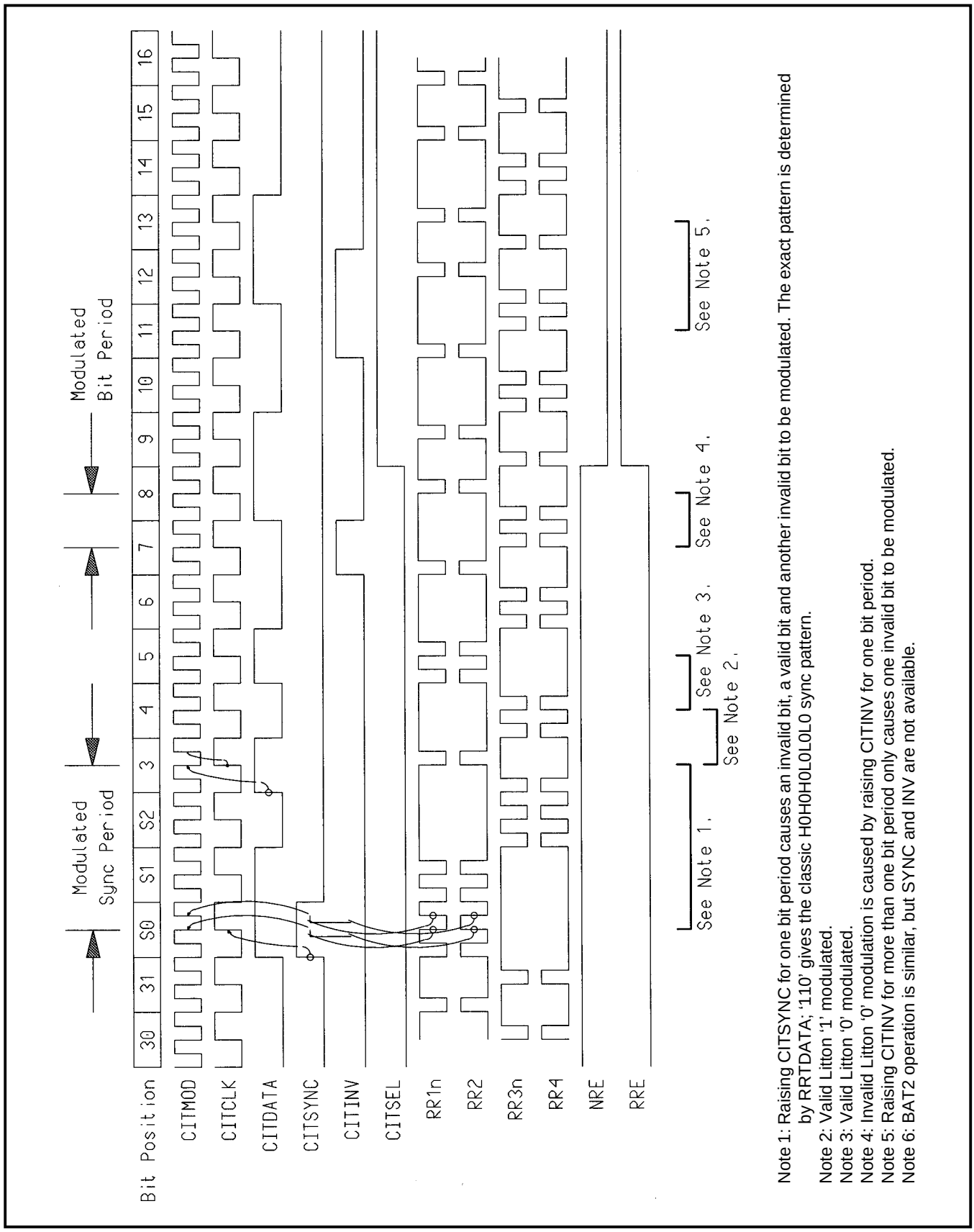


Figure 4: Architecture

Note: Switches in lower position - RT mode
Switches in upper position - CT mode

MODEM Modulation Waveforms are compliant with ESA document THB/Apo/KZ/1386/av. Waveforms indicating the operation of BAT1, 2 and BAR1, 2, 3 in both the CT and RT modes are shown in Figures 5 to 8.



Note 1: Raising CITSYNC for one bit period causes an invalid bit, a valid bit and another invalid bit to be modulated. The exact pattern is determined by RRTDATA; '110' gives the classic H0H0H0L0L0L0 sync pattern.
Note 2: Valid Litton '1' modulated.
Note 3: Valid Litton '0' modulated.
Note 4: Invalid Litton '0' modulation is caused by raising CITINV for one bit period.
Note 5: Raising CITINV for more than one bit period only causes one invalid bit to be modulated.
Note 6: BAT2 operation is similar, but SYNC and INV are not available.

Figure 5: CT Mode Bus Adaptor Transmitter Waveforms

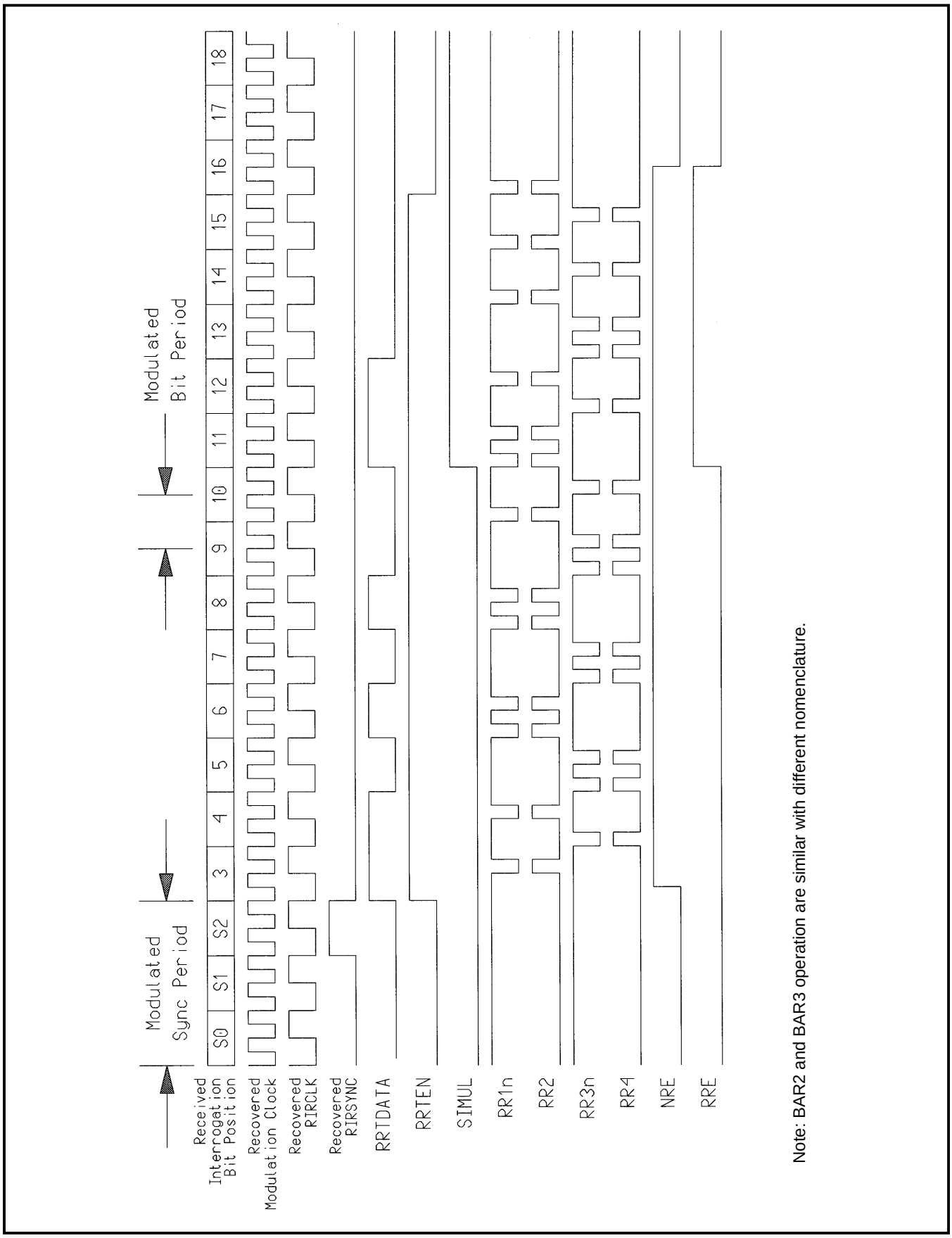


Figure 6: RT Mode Bus Adaptor Transmitter Waveforms

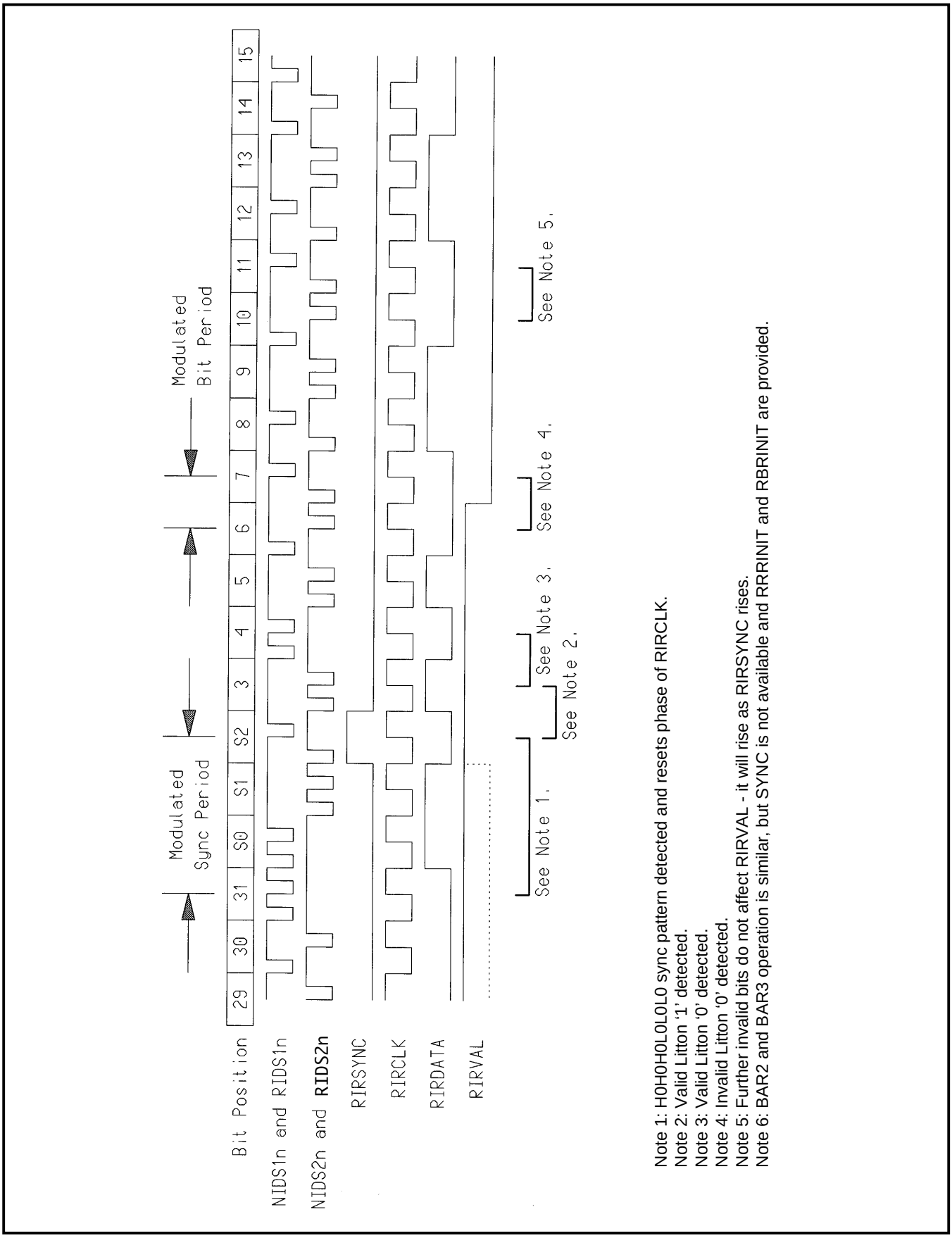


Figure 7: RT Mode Bus Adaptor Receiver Waveforms

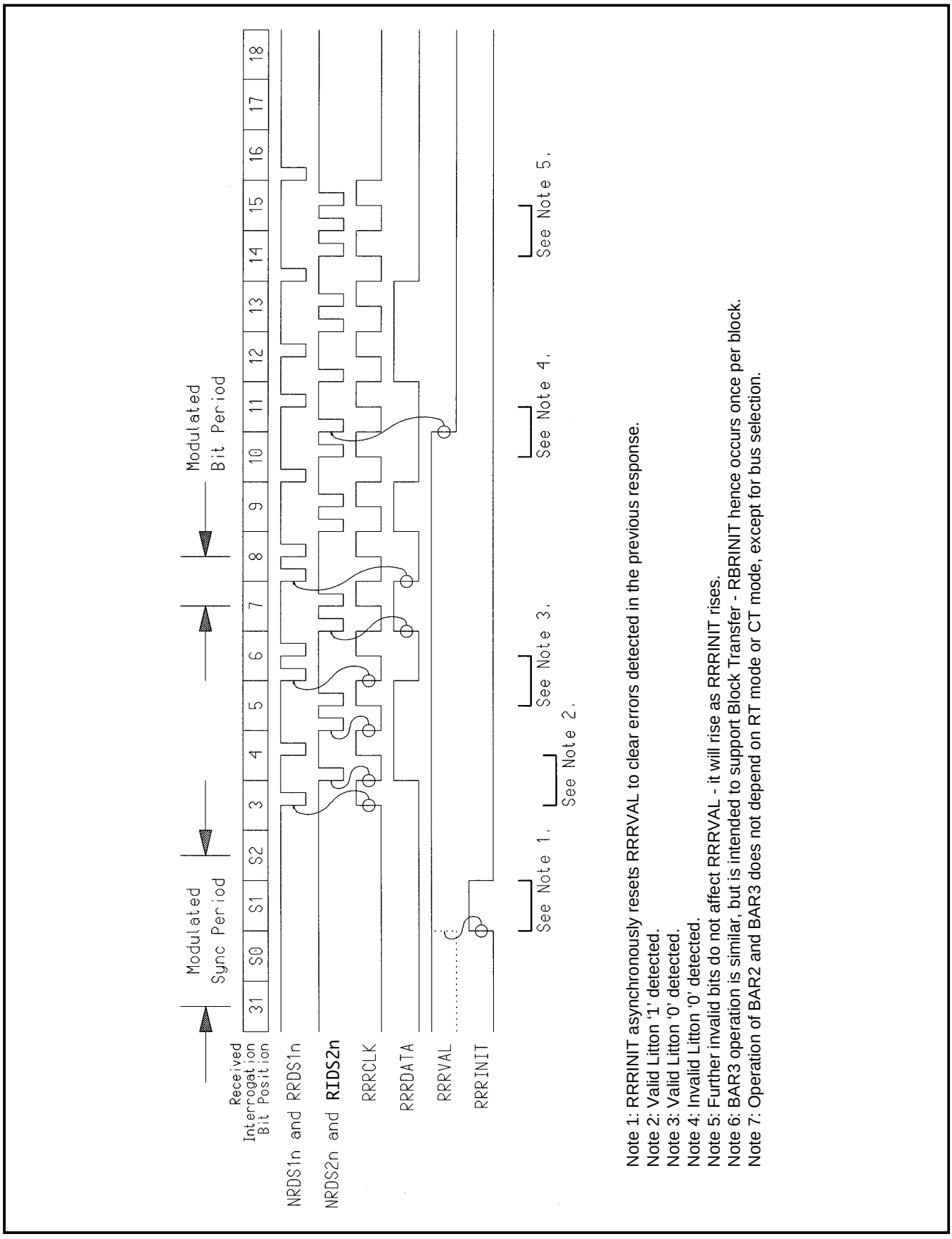


Figure 8: BAR2 Bus Adaptor Receiver Waveforms

CLOCK DETECTOR OPERATION

The Clock Detector architecture is shown in Figure 9; a separate channel is essentially provided for each of the Nominal and Redundant Interrogation busses. Associated waveforms are shown in Figure 10.

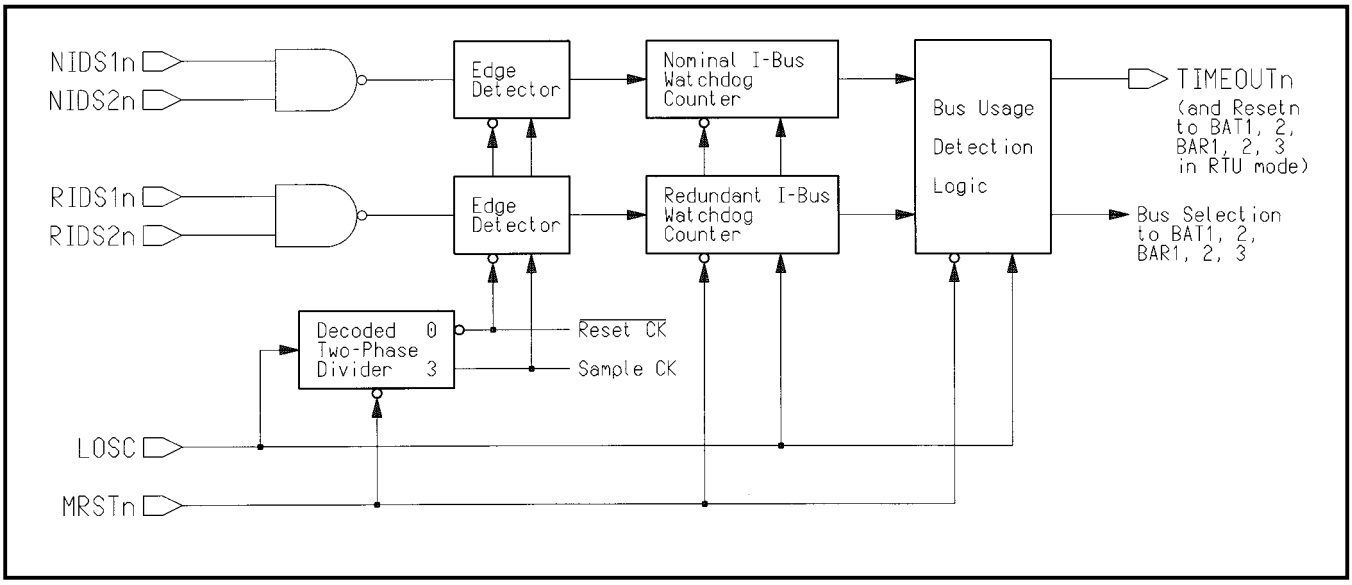


Figure 9: Clock Detector Architecture

Each channel contains an Edge Detector and a 5-bit Watchdog Counter which respond only to high-to-low transitions on their respective Interrogation bus DS1n inputs. A common Bus Usage Detection circuit is used to generate time-out pulses (used for internal and external reset) and bus selection signals from the results of the watchdogs.

The local oscillator input, LOSC, is divided and decoded to generate an active low reset and an active high sample clock. When applied to both input Edge Detectors, these signals permit input high-to-low transitions to be detected for one LOSC cycle in every two (between the reset ↓ and sample clock ↑). Once such transitions have been detected by a sample clock, the associated watchdog counter is reset. The MSB of each watchdog counter is used as an indication of its bus's status - active or inactive. Should the watchdog counter overflow (i.e. its MSB be set to 1), the associated bus will be considered inactive.

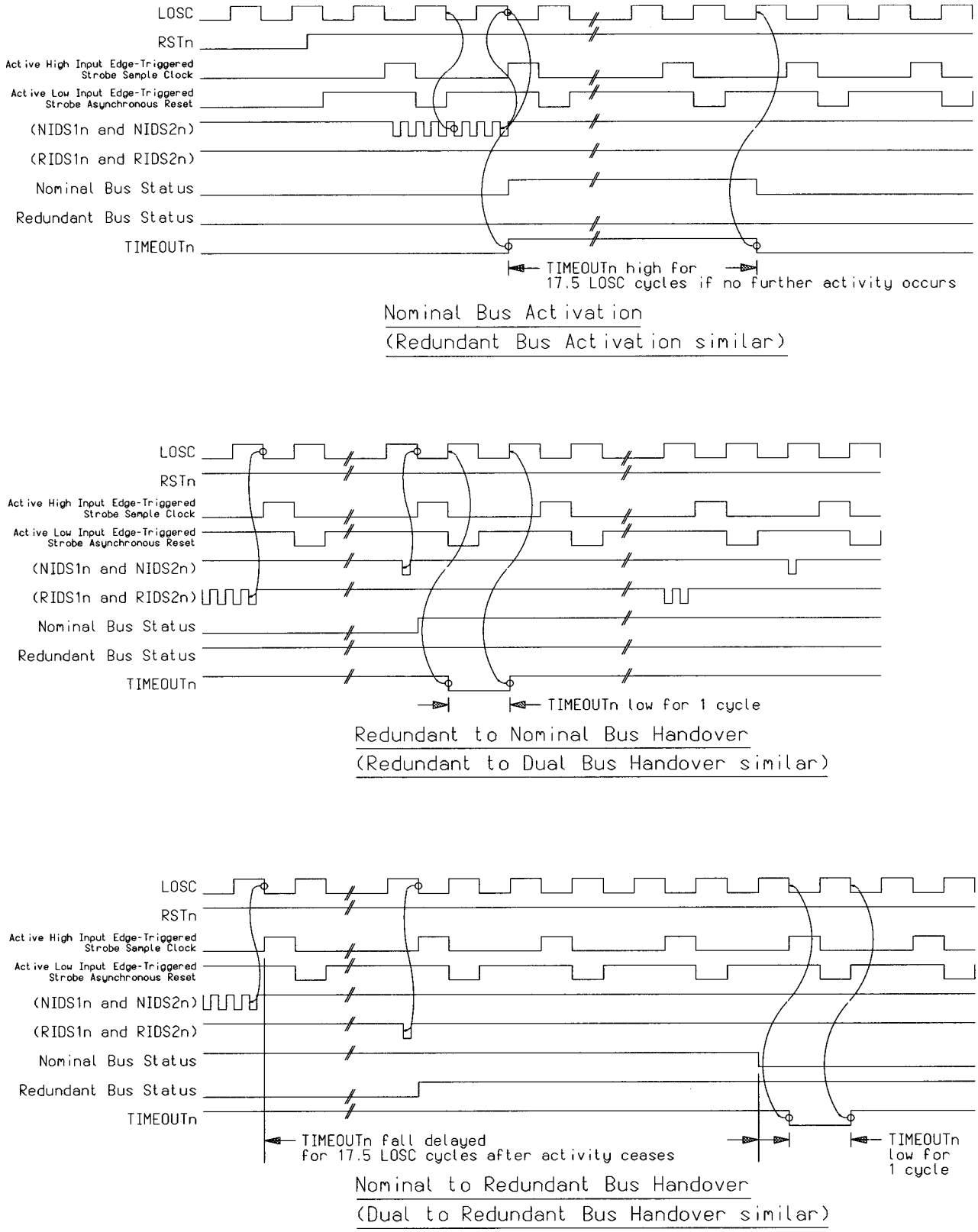
The status of the Nominal and Redundant Interrogation busses is used to determine internal bus selection for the modulation of Response and Block Transfer data in the device's RT mode. If neither bus is considered active, the TIMEOUTn pin will be held low and RT mode reception of all 3 busses will be inhibited. If one bus is considered active, RT mode reception will occur on the same set of bus circuits (redundancy) as the active Interrogation bus. If both busses are considered active, RT mode reception from the Nominal set of bus circuits will be performed. RT mode transmission will always occur on the same set of bus circuits (redundancy) as selected for reception unless the SIMUL pin is held high, in which case transmission will occur simultaneously on both the Nominal and Redundant busses.

Both watchdog counters are fully set at power up to mark both busses as inactive - in this way, a missing LOSC input will not cause inactive busses to be deemed active.

For a single detected input transition, 17.5 to 18.5 LOSC cycles will elapse before the relevant bus is considered inactive. If near-instantaneous Nominal-to-Redundant or Dual-to-Redundant bus handover occurs, the change-over will be delayed by 18 to 19 LOSC cycles, in order to preserve the priority of the Nominal bus. If near-instantaneous Redundant-to-Nominal or Redundant-to-Dual bus handover occurs, the change-over will occur after 1.5 to 2.5 LOSC cycles since the Nominal bus takes priority. In either of these cases, a 1 LOSC cycle TIMEOUTn pulse is always generated to ensure that internal reset occurs.

The frequency of the local oscillator may be varied to make the nominal time-out period of 17.5 LOSC cycles correspond to any desired number of (missing) bits on the Interrogation bus. Variation of the duty cycle does not vary the time-out period. After 16 LOSC cycles without detected input transitions, the associated watchdog times-out and is detected on the next LOSC ↑ edge; the generation of a TIMEOUTn pulse and reset are then inevitable.

For proper Clock Detector operation, (at least) one high-to-low input transition must be detected within a period of 16 LOSC cycles of the last such detection, but transitions made during alternate LOSC cycles (the phase is difficult to predict) will not be detected. Local oscillator clock signals which are harmonically-related to the modulation clock by an integer ratio are thus a cause for concern, although this problem is perhaps only likely to occur in experimental set-ups.



Note: If both busses are determined by their watchdogs to be active (as indicated above by their status), the Nominal Bus will always be used by the Bus Adaptor Transmitter and Receiver circuits instead of the Redundant Bus.

Figure 10: MA28139 Clock Detector Operation

The requirement to respect set-up and hold times for the capture of the Edge Detector outputs by the LOSC high-to-low transition means that LOSC signals which are harmonically-related to the Litton modulation clock but whose phase can not be controlled can never be guaranteed to provide reliable operation.

For asynchronous local oscillator signals, there will be no concern if we are simply able to place two or more Litton DSn high-to-low edges into each LOSC cycle, so that:

$$\tau_{MOD} \leq \tau_{LOSC} - t_{SU} - t_{HOLD}$$

and the time-out period of 16 τ_{LOSC} is hence approximately 8 bit periods or more.

However, suppose that the periods of the modulation clock and the local oscillator clock are such that the relationship between them is:

$$\tau_{MOD} = m \ \tau_{LOSC}$$

where m is a positive integer.

In order to respect the setup and hold times, t_{SU} + t_{HOLD} respectively, between the DSn ↓, and LOSC ↓ edges, it is necessary to avoid such harmonic relationships; it can be shown that around these spot frequencies it is necessary to ensure that either:

$$w \ \tau_{MOD} \geq x \ \tau_{LOSC} + t_{SU} + t_{HOLD}$$

or

$$y \ \tau_{MOD} \leq z \ \tau_{LOSC} - t_{SU} - t_{HOLD}$$

where the integer constants w, x, y and z are given in the table below.

Since two modulation clock cycles occur per bit, the time-out period at these harmonics will then be:

$$16 \ \tau_{LOSC} \approx 16 \ \tau_{MOD} / m \approx 8 / m \text{ bit periods.}$$

m	w	x	y	z	Approx. time-out period (bit periods)
1	15	15	17	17	8
2	7	15	8	15	4
3	5	15	5	15	2.67
4	3	13	4	15	2
5	3	15	3	15	1.6
6	2	13	2	11	1.33
7	1	7	1	7	1.14
8	1	9	2	15	1
9	1	9	1	9	0.88
10	1	11	1	9	0.8
11	1	11	1	11	0.73
12	1	13	1	11	0 67
13	1	13	1	13	0.62
14	1	15	1	13	0.57
15	1	15	1	15	0.53

In summary, slow local oscillator clocks which cause relatively long timeout periods ≥ 8 bit periods are not considered a problem; very long time-outs can be reliably implemented. For shorter time-out periods, however, it is necessary to avoid harmonic relationships between the Litton modulation clock and the local oscillator. The simplest practical method for avoiding such relationships would be to arrange for the ratio

$$n = \tau_{MOD} / \tau_{LOSC}$$

to have a half-integer value such that n = 0.5, 1.5, 2.5, ...using an independent crystal oscillator if necessary.

OBDH / IUB INTERFACE

The Central Terminal Unit controls timing, commands and telemetry to all subsystems on the OBDH bus. ESA TTC-B-01 specifies the OBDH to be 2 redundant sets (Nominal and Redundant) of 2 twisted pairs (Interrogation and Response bus) plus an optional redundant 3rd twisted pair (Block Transfer bus), Litton modulated (self clocking with parity on each bit), balanced transformer coupled for less than 1 error in 100 million bits on a 25 metre bus. The data rate is nominally 500K Bits/sec although the chip itself supports up to 5MBits/sec. The OBT is transformer coupled with adjustable reference and threshold levels as shown below. Litton more positive than V_{th+} makes discriminator signal NIDS1n low. Litton more negative than V_{th-} makes NIDS2n low. OBT RR1n, RR2, RR3n, RR4 control 4 switches which drive the bus with bipolar Litton code when enabled. For clarity redundancy is not shown below:

TTC-B-01 also specifies the IUB. The OBT supplies specified clocks, memory load address for ML data (or channel address for mode command) and responds on the R bus with a 13 zeroes response as acknowledgement. If the command requires data aquisition, the OBT responds with a 13 or 21 bit response containing 8 or 16 bits (respectively) of user data, controlling external ADC as required.

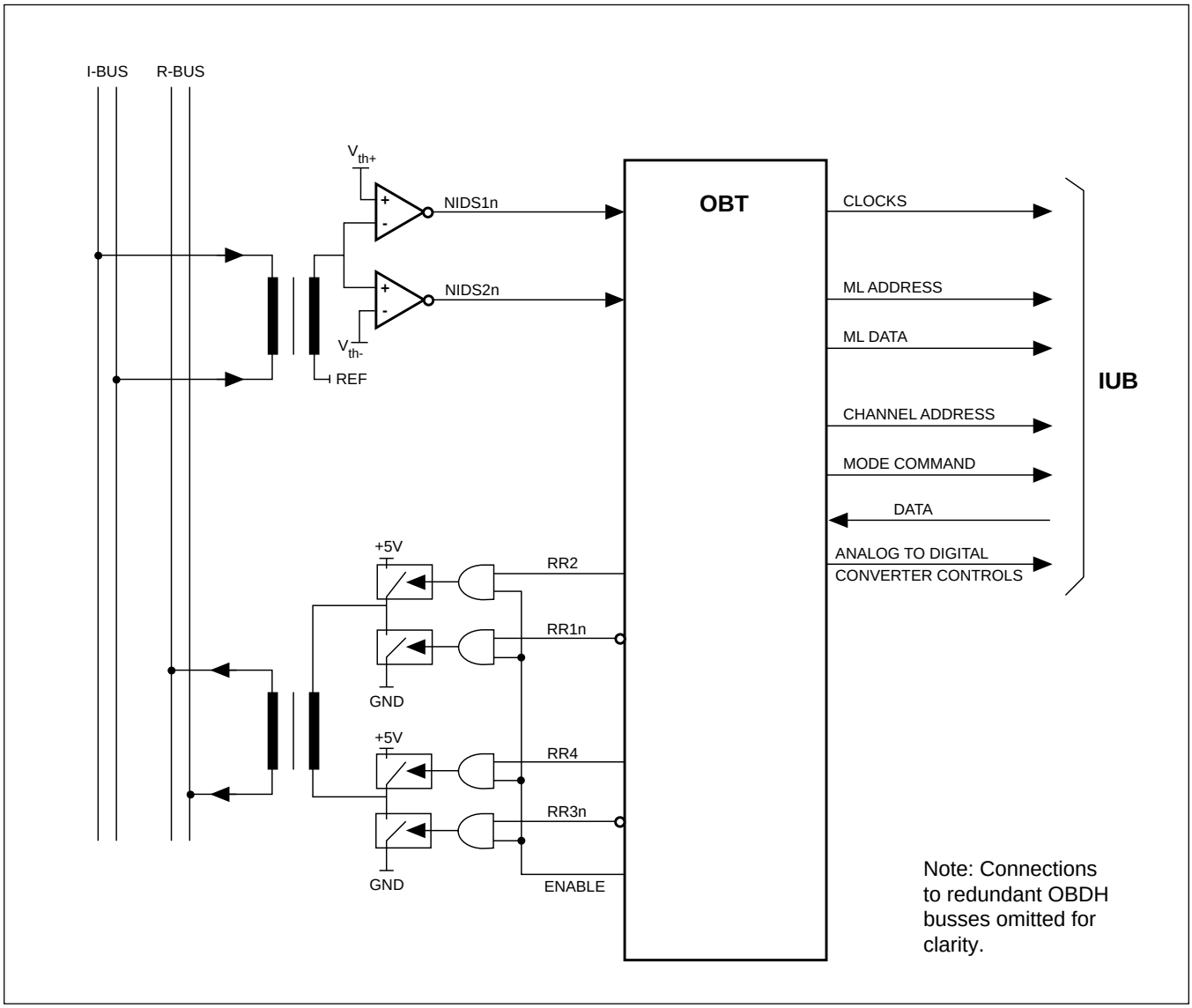


Figure 11: OBDH to IUB interface

RTU KERNEL PROTOCOL VIOLATIONS

Some commands to the RTU Kernel cannot be completed within one Interrogation period (or “slot”) because of the need to provide a slow external interface as defined in ESA standard TTC-B-01. These are commands for 16-bit Digital Serial Acquisition (S16) and 16-bit Memory Load (ML). In addition, it is also possible to inhibit On/Off commands by pin configuration.

Consequently:

- a Memory Load command cannot be followed by another Memory Load command in the next Interrogation; the second command of such a sequence will be ignored,
- a 16-bit Digital Serial Acquisition (S16) cannot be followed by another acquisition or command in the next Interrogation; the second command of such a sequence will be ignored,
- a Long On/Off command will be ignored if the On/Off command Inhibit input pin, OOINH, is high.

Note that in all MODE Dependent Command and Acquisition Interrogations, bits 23 to 30 of the Interrogation are output as an 8 bit channel address on CHADD(0:7). ESA standard TTC-B-01, p.110 specifies a 7 bit channel address in bits 27 to 29, leaving bit 30 as Reserved. For complete compliance with this standard, CHADD(7) should be disregarded and CHADD(0:6) only should be used.

The signals generated by the RTU Kernel during 8-bit Single-Ended and 8-bit Double-Ended Analog Data Acquisitions are intended for connection to an 8-bit serial ADC module. The outputs PC, ANCLK, SOC and SH are intended to provide ADC power control, conversion clock, start of conversion pulse and sample/hold control respectively.

RTU Kernel BroadCast Pulse and BCP Validity Waveforms are shown in Figure 12.

RTU Kernel Memory Load Command Waveforms are shown in Figure 13.

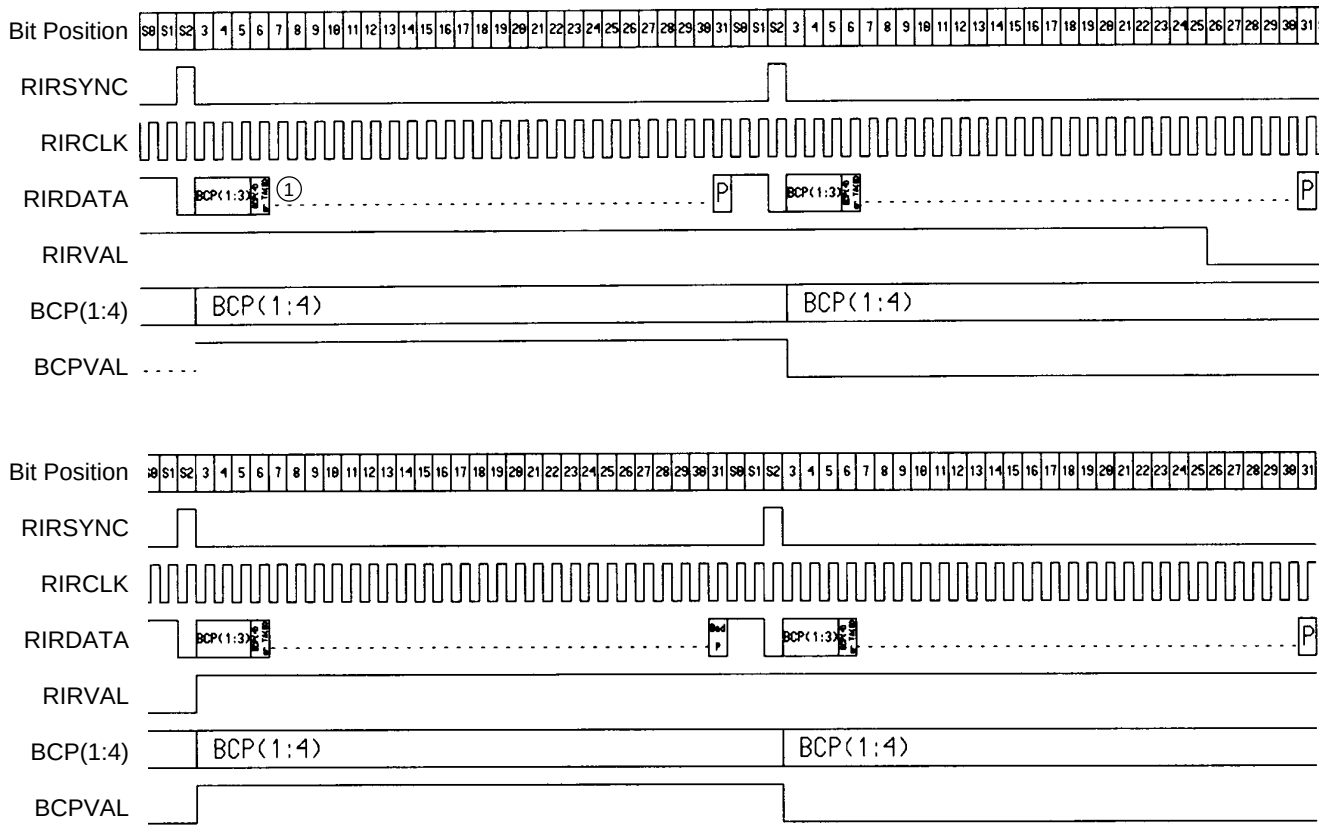
RTU Kernel MODE Dependent Command and Acquisition Waveforms are shown in Figures 14 - 17.

RTU KERNEL MODE DEFINITIONS

The mode field contained in bits 19 to 22 of the Interrogation is decoded during acquisition commands to drive one of the MOSC, MOLC, MOHL, MOBT, MODBL, MODS8, MODS16, MOANS or MOAND outputs. Mode decoding is an extension of that defined in ESA standard TTC-B-01 Table 7.1 and is shown in Table 1 below:

Mode Code					Associated
Bit 19	Bit 20	Bit 21	Bit 22	Function	Output Pin
0	0	0	0	Unused	-
0	0	0	1	Short Switch Closure On/Off Command	MOSC
0	0	1	0	Long Switch Closure On/Off Command	MOLC
0	0	1	1	High Power Switch Closure On/Off Cmd	MOHL
0	1	0	0	Unused	-
0	1	0	1	Unused	-
0	1	1	0	Unused	-
0	1	1	1	Block Transfer Command	MOBT
1	0	0	0	8-bit Digital Bi-Level Data Acquisition	MODBL
1	0	0	1	Unused	-
1	0	1	0	16-bit Serial Digital Data Acquisition	MODS16
1	0	1	1	8-bit Serial Digital Data Acquisition	MODS8
1	1	0	0	8-bit Single-Ended Analog Data Acquisition	MOANS
1	1	0	1	Unused	-
1	1	1	0	8-bit Double-Ended Analog Data Acquisition	MOAND
1	1	1	1	Unused	-

Table 1: RTU Kernel Mode Definitions

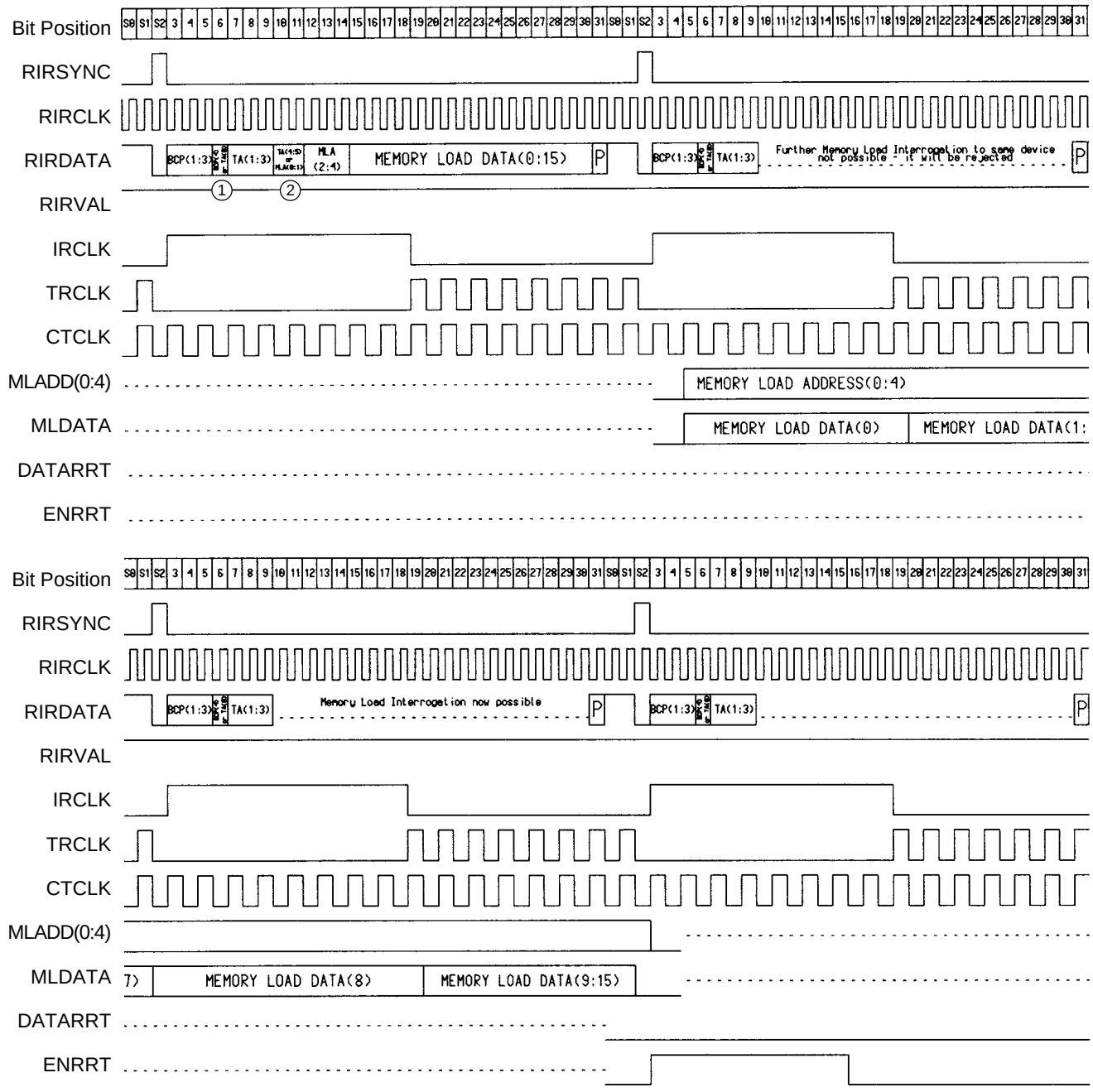


① = BCP(4) or TA(0)

Note 1: Bit 6 of the Interrogation will be interpreted as BCP(4) if (EXTFMT = 0);
if (EXTFMT = 1), the BCP (4) output will be 0 and bit 6 will be interpreted as TA(0).

Note 2: (RIRVAL = 0) (presumably because of bad Interrogation length or received Litton coding errors detected by the modem), bad received parity in bit 31 of the Interrogation or wrong Interrogation length will both cause the Interrogation to be rejected and will set BCPVAL = 0.

Figure 12: BroadCast Pulse and BCP Validity Waveforms



① = BCP(4) or TA(0)

② = TA(4:5) or MLA(0:1)

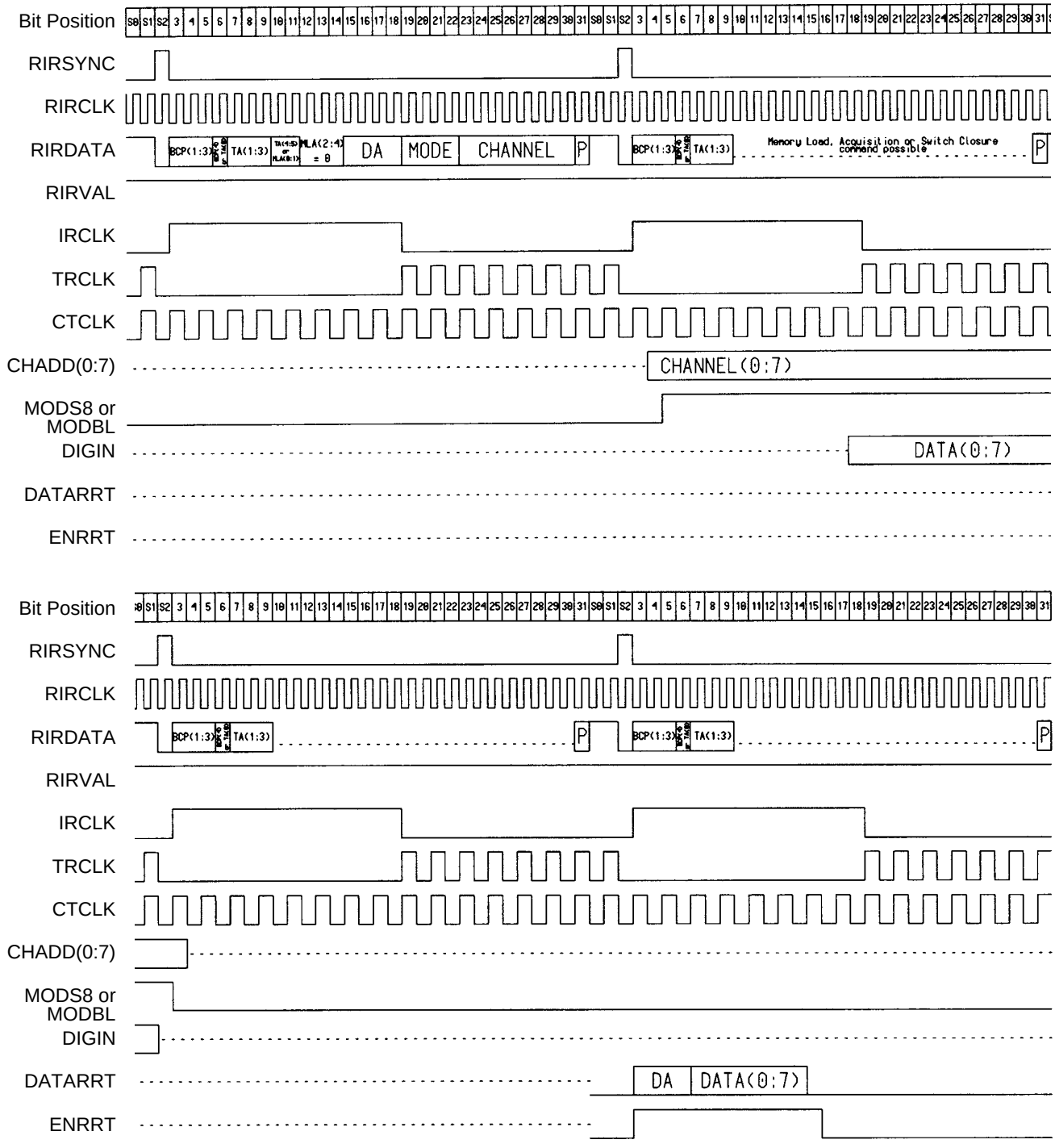
Note 1: One Memory Load command takes 2 Interrogations to complete. Consecutive Memory Load commands are hence not possible and form a protocol violation. The second Memory Load command of such a sequence will be rejected.

Note 2: For a Memory Load command to be decoded, the evaluated Memory Load Address must be non-zero. An evaluated Memory Load Address of zero implies data aquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The Memory Load command response is always 13-zeros.

Figure 13: Memory Load Command Waveforms

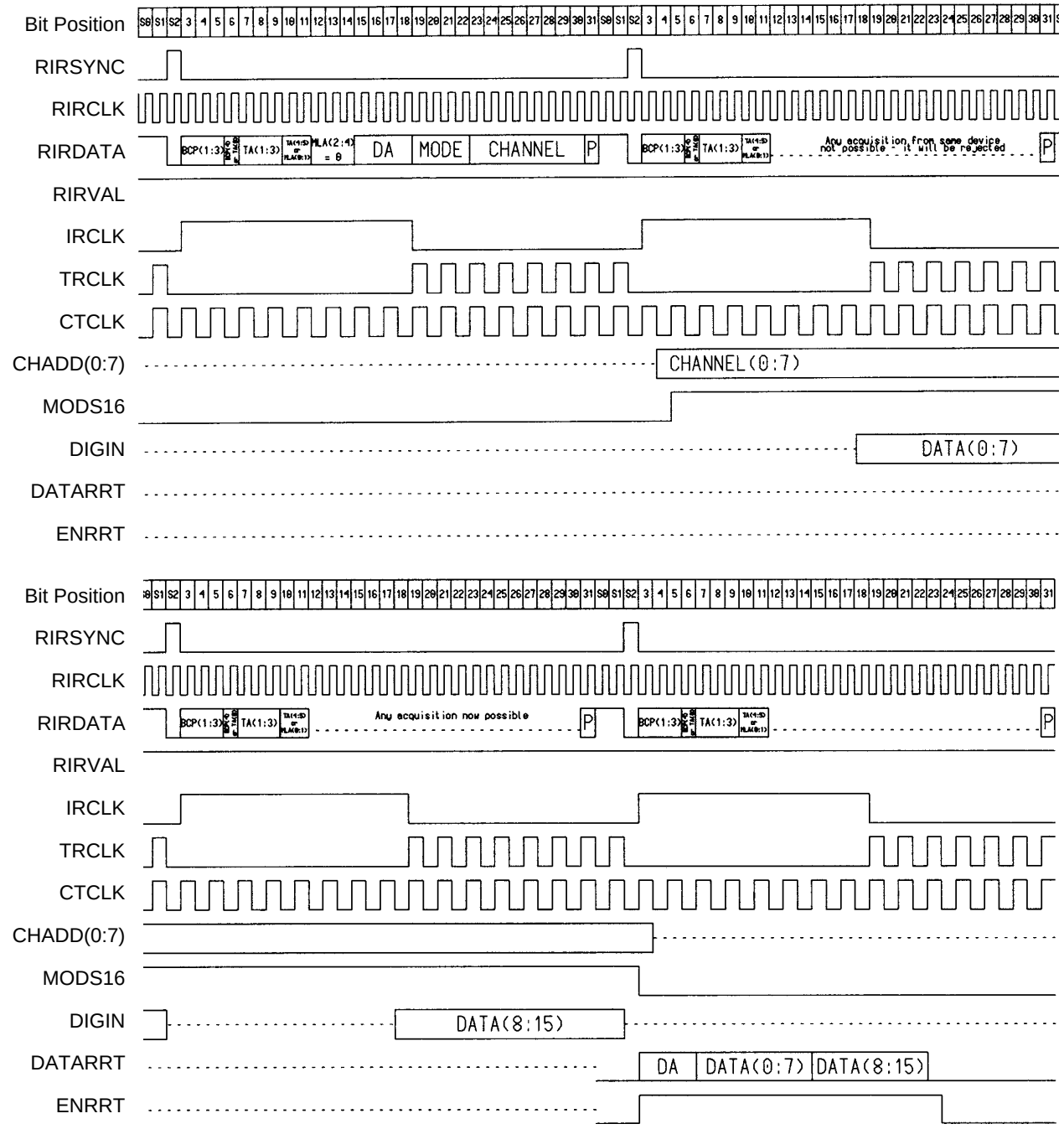


Note 1: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 2: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 3: The 8-bit Digital Serial and 8-bit Digital Bi-Level Acquisition command responses are always 13 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 14: 8-Bit Digital Serial and 8-Bit Digital Bi-Level Acquisition Waveforms



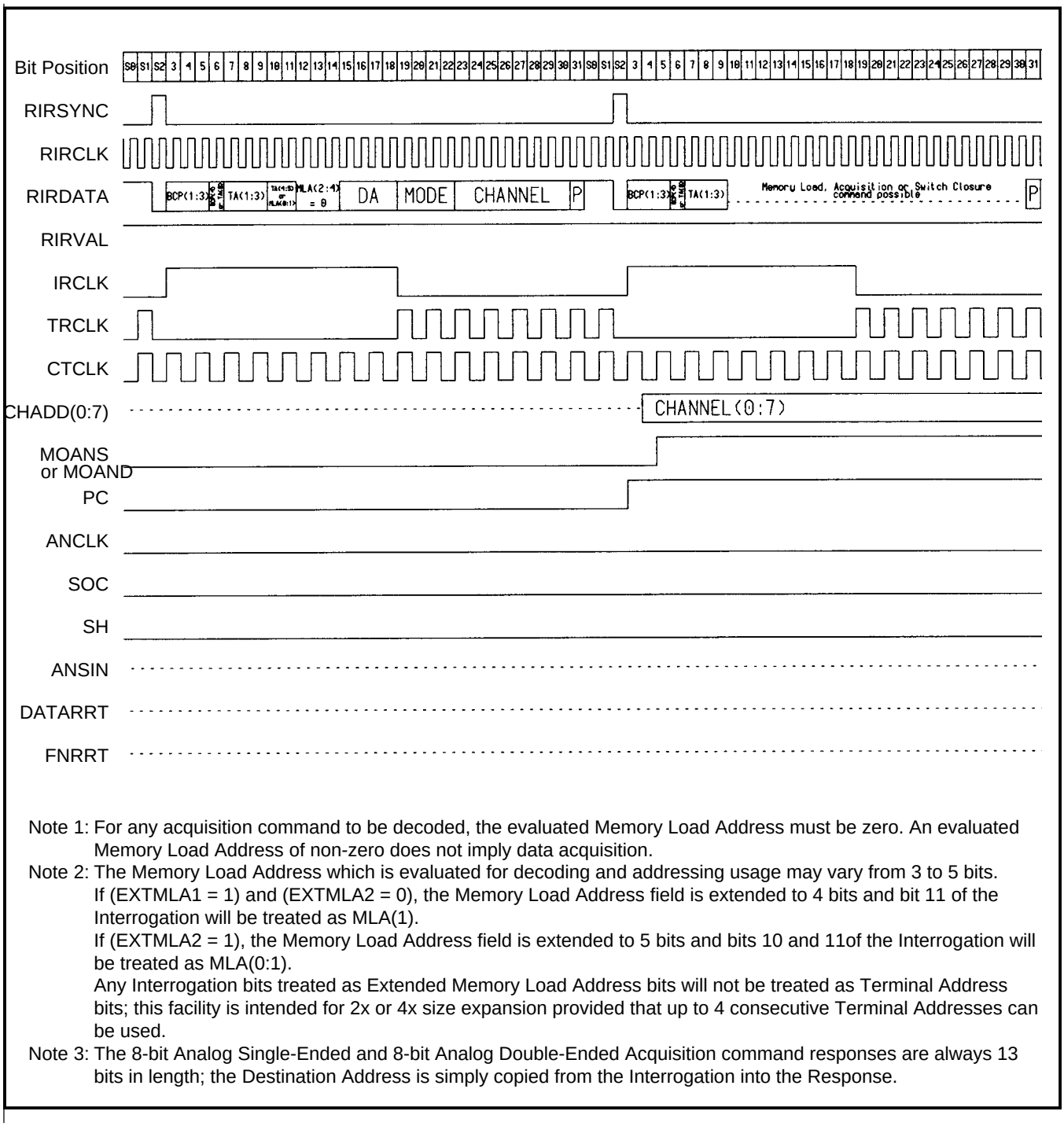
Note 1: One 16-bit Digital Serial Acquisition command takes 2 Interrogations to complete. A succeeding Acquisition or Switch Closure command of any type is hence not possible and forms a protocol violation. The second command of such a sequence will be rejected.

Note 2: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11 of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The 16-bit Digital Serial Acquisition command response is always 21 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 15: 16-Bit Digital Serial Acquisition Waveforms



Note 1: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 2: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 3: The 8-bit Analog Single-Ended and 8-bit Analog Double-Ended Acquisition command responses are always 13 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 16: 8-Bit Analog Single-Ended and 8-Bit Analog Double-Ended (Serial) Acquisition Waveforms

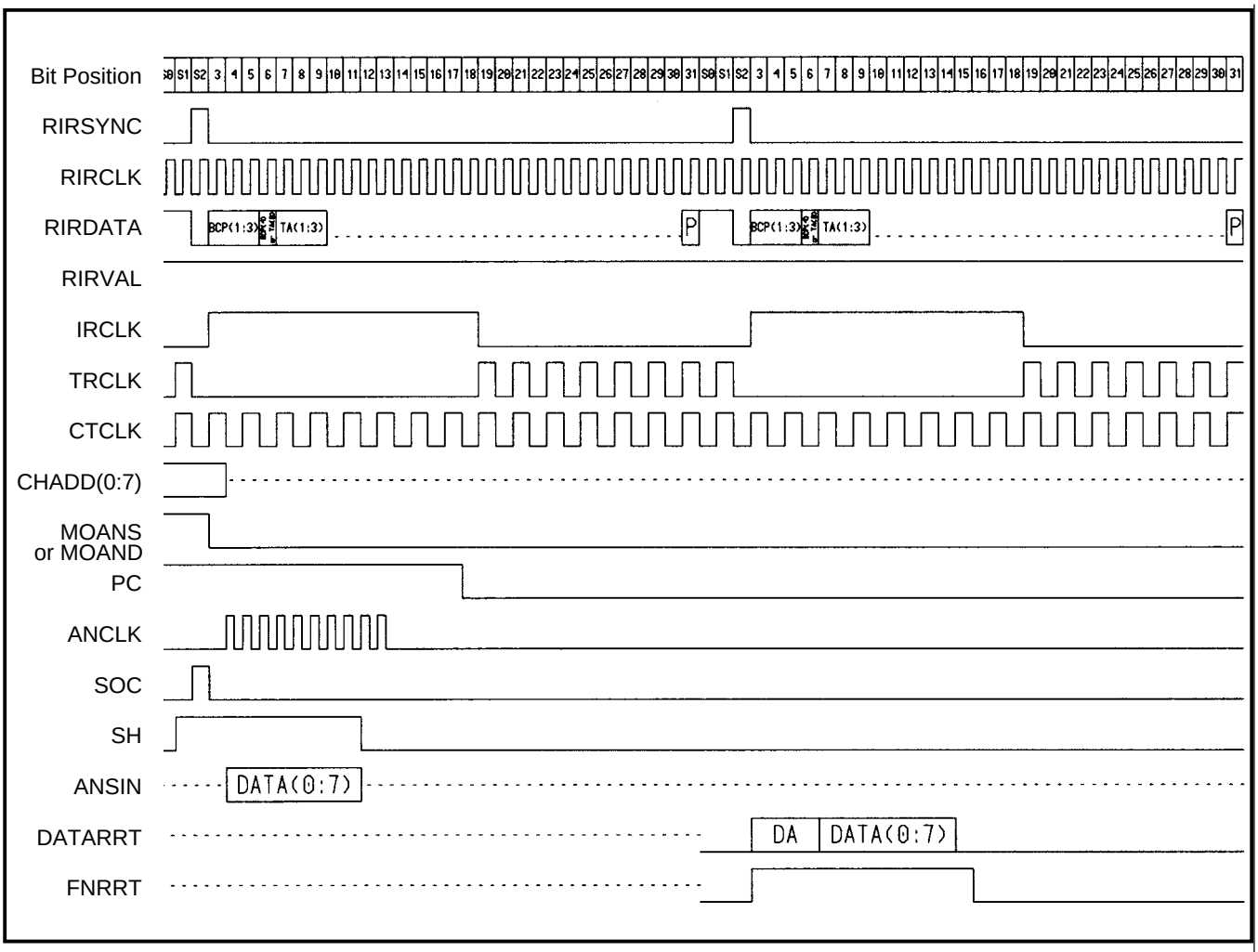
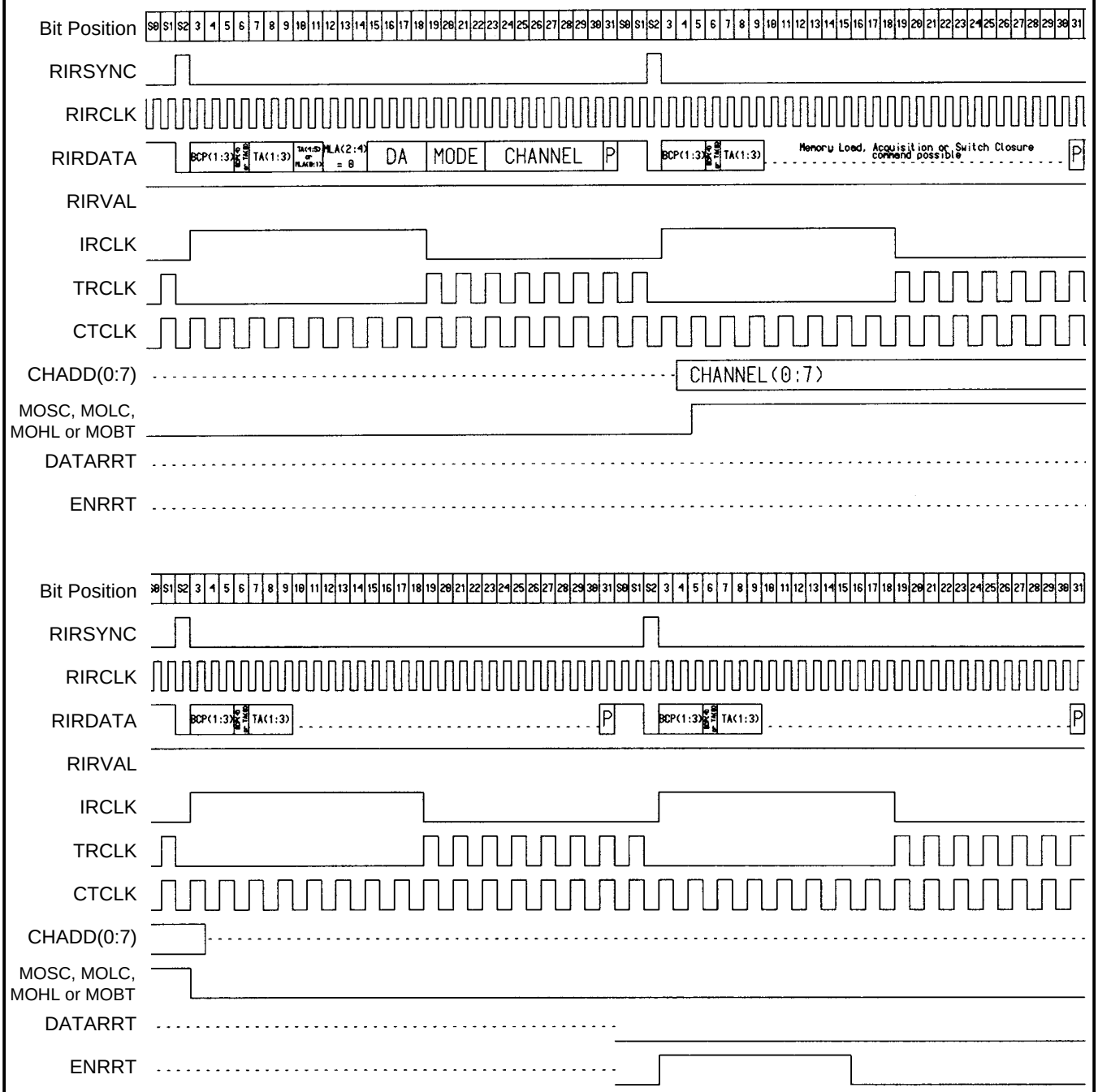


Figure 16 continued



Note 1: The Block Transfer command does not require a Channel Address; CHADD(0:7) is set therefore to zero.

Note 2: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The Short-Command, Long-Command, High-Level Switch Closure and Block Transfer command responses are always 13-zeroes.

Figure 17: Short-Command, Long-Command and High-Level Switch Closure and Block Transfer Command Waveforms

THE ESA ON-BOARD DATA HANDLING (OBDH) BUS

The dual redundant OBDH bus is connected to the OBT bus interface via an input descriminator and an output bridge driver circuit. These convert between the bipolar LITTON code and the standard CMOS inputs and outputs of the IC.

The OBDH bus is divided into three parts:

A. INTERROGATION BUS (I BUS)

This bus is used to transfer data from the CT to the RTs, as commands of 32 bit words, each bit being modulated according to the Litton scheme shown in Figure 18. Each Interrogation (or command) “slot” comprises 3 Sync bits, 3 or 4 BroadCast Pulses, 5 or 6 Terminal Address bits, 4 Destination Address bits, 16 Data bits and a Parity bit.

B. RESPONSE BUS (R BUS)

This bus is used to send data from the RTs to the CT, (can be used by RTs to receive data). Each response word comprises the 4 Destination Address bits sent in the corresponding Interrogation, either 8 or 16 Data bits from the user (8 bits unless a 16 bit acquisition was requested and 8 zeros if no response data is required) and a single Stop bit (used to ensure data is fully clocked through bus modems and 0 by convention).

C. BLOCK TRANSFER BUS (BT BUS)

Used to transfer blocks of data between the CT and RTs, in either direction, as a contiguous block or stream of data bits.

FASTER OBDH/DBI COMPATIBLE NETWORKS

With analog components the OBT can interface any equipment to the specified ESA OBDH bus at the nominal data rate of 0.5 Mbps. Contract 5352 proved that analog components limit OBDH data rate to 2 Mbps maximum. But OBTs work to over 5 Mbps (10MHz with 2 clocks/bit Litton coded). OBTs may be directly networked via digital bus drivers/receivers, (eliminating analog components) using Litton coded 4 wire (R2/DS1 and R4/DS2) busses (see OBDH application note 1). MSS made a 3 metre optical OBDH network for the Pegasus ion source.

DBIs may be directly connected but will not be Litton coded with Parity on every bit, or exhibit modulation and demodulation delays.

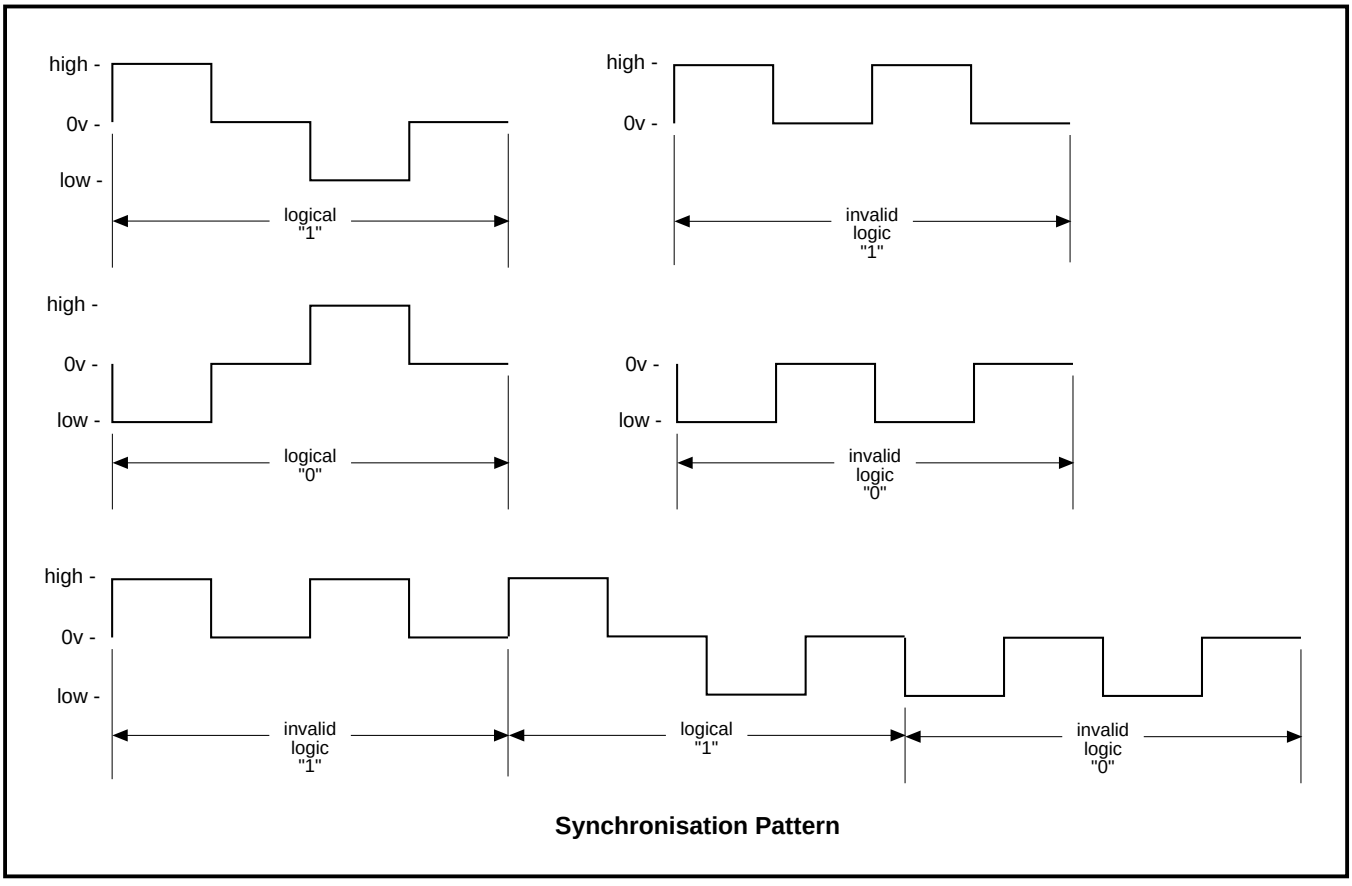
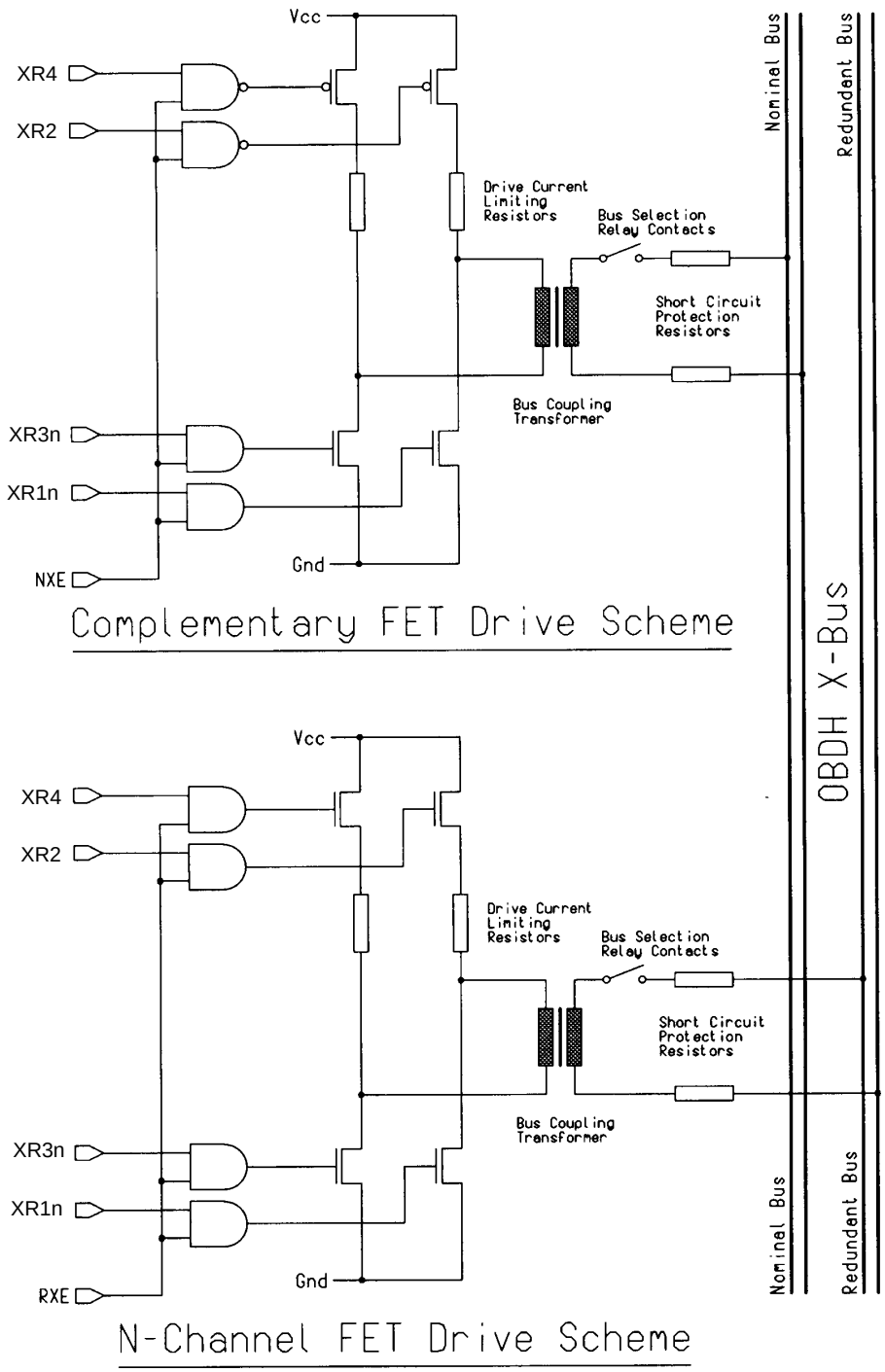


Figure 18: Litton Coded Data

CONNECTIONS TO THE OBDH I, R AND BT BUSSES (SUGGESTED SCHEMES ONLY)

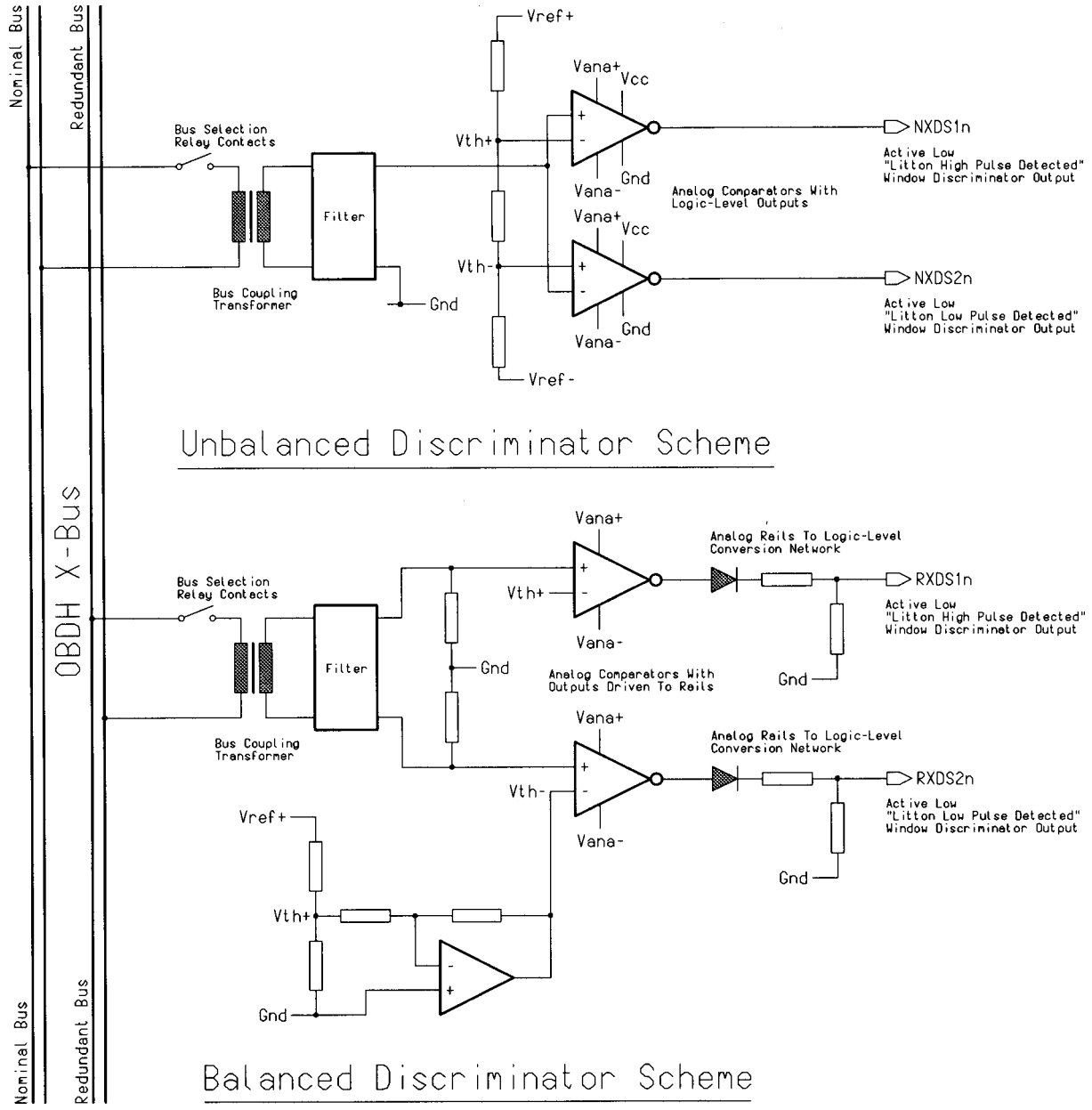
TRANSMITTER



Two OBDH bus driver schemes based on complementary and N-channel enhancement-mode FETs are shown.
Current-limiting and protection resistors may be employed to prevent damage under short-circuit.
Latching and/or non-latching relays may be used to provide isolation from the bus when a redundant circuit is unused or unpowered.
NPN and/or PNP bipolar junction transistors may also be employed in place of FETs.
Redundancy can be handled in channels (as shown) or by applying cross-strapping between the transformers and the drivers.
This implementation generates 'active ground' pulses where the transformer is shorted out (by conduction of the two lower FETs) while the bus driver is enabled to reduce ringing, bus echoes, etc.
Using XR2 in place of XR3n and XR4 in place of XR1n will not cause 'active zeros' to be driven.

Figure 19: Conceptual OBDH Bus Driver Scheme

RECEIVER



Two OBDH bus window discriminator schemes, based on balanced and unbalanced techniques are shown.
Current-limiting and protection resistors may be employed to prevent damage under short-circuit.
Latching and/or non-latching relays may be used to provide isolation from the bus when a redundant circuit is unused or unpowered.
Noise filtering and the effects of bus loading should be considered.
Redundancy can be handled in channels (as shown) or by applying cross-strapping between the transformers and the receivers.

Figure 20: Conceptual OBDH Bus Window Discriminator Scheme

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	CMOS input high voltage	-	$0.8V_{DD}$	-	V_{DD}	V
V_{IL}	CMOS input low voltage	-	V_{SS}	-	$0.2\ V_{DD}$	V
V_{OH}	Output high voltage	I_{OH} = -1.0mA	V_{DD} - 0.5	-	-	V
V_{OL}	Output high voltage	I_{OL} = 4.0mA	-	-	0.4	V
I_{PDL}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-25	-	25	µA
I_{PDH}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{DD}	25	-	400	µA
I_{PUL}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-400	-	-25	µA
I_{PUH}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-25	-	25	µA
I_L	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-10	-	10	µA
I_{OZL}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{SS}	-30	-	30	µA
I_{OZH}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{DD}	25	-	400	µA
I_{DD1}	Static Power supply Current	V_{DD} = 5.5V	-	0.02	8	mA
I_{DD2}	Dynamic Power supply Current	f = 1MHz, V_{DD} = 5.5V	-	6	20	mA

Notes: 1. V_{DD} = 5V ±10% over full temperature range.
2. Total dose radiation not exceeding 10^5 Rads(Si).
3. Mil-Std-883, method 5005, subgroups 1, 2, 3.
4. All outputs are suitable for TTL/CMOS drive.
5. Electro-Static Discharge protection is provided for all pins.
6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.
7. Input and output leakage measurements are guaranteed but not tested at -55°C.

Table 3: DC Characteristics

AC CHARACTERISICS

No.	Parameter	Condition	Min.	Max.	Units
T1	CITMOD to RR1n, RR2, RR3n, RR4, BR1n, BR2, BR3n, BR4	CTU mode	-	45	ns
T2	CITMOD to NRE, RRE, NBE, RBE	CTU mode	-	55	ns
T3/ T3a	CITSYNC, CITINV to CITCLK ↑ (setup/hold)	CTU mode	10	-	ns
T4/4a	RRTDATA to CITMOD ↓ (setup/hold)	CTU mode	10	-	ns
T5/5a	RBTDATA to CITMOD ↓ (setup/hold)	CTU mode	10	-	ns
T6/6a	RBTEN to CITMOD ↑ (setup/hold)	CTU mode	10	-	ns
T7/7a	CITCLK to CITMOD ↑ (setup/hold)	CTU mode	10	-	ns
T8	NIDS1n, NIDS2n, RIDS1n, RIDS2n to RR1n RR2, RR3n, RR4, BR1n, BR2, BR3n, BR4	RTU mode	-	55	ns
T9	NIDS1n, NIDS2n, RIDS1n, RIDS2n to NRE RRE, NBE, RBE	RTU mode	-	75	ns
T10/ T10a	RRTDATA to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup/hold)	RTU mode	10	-	ns
T11/ T11a	RBTDATA to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup/hold)	RTU mode	10	-	ns
T12	RRTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ setup	RTU mode	0	-	ns
T12a	RRTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ hold	RTU mode	35	-	ns
T13	RBTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ setup	RTU mode	0	-	ns
T13a	RBTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ hold	RTU mode	35	-	ns

Table 4: Bus Adaptor Transmitter Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T14	NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ to RIRSYNC, RIRCLK, RIRDATA, RIRVAL valid	RTU mode	-	80	ns
T15	NRDS1n, NRDS2n, RRDS1n, RRDS2n ↓ to RRRCLK, RRRDATA valid	RTU mode	-	55	ns
T16	NBDS1n, NBDS2n, RBDS1n, RBDS2n to RBRCLK, RBRDATA valid	RTU mode	-	55	ns
T17	NRDS1n, NRDS2n, RRDS1n, RRDS2n ↓ to RRRVAL ↓	RTU mode	-	55	ns
T18	NBDS1n, NBDS2n, RBDS1n, RBDS2n to RBRVAL ↓	RTU mode	-	55	ns
T19	RRRINIT to RRRVAL ↑	RTU mode	-	30	ns
T20	RBRINIT to RBRVAL ↑	RTU mode	-	30	ns
T21	NIDS1n, NIDS2n, RIDS1n, RIDS2n pulse width low (min.)	RTU mode	12	-	ns
T22	NRDS1n, NRDS2n, RRDS1n, RRDS2n pulse width low (min.)	RTU mode	12	-	ns
T23	NBDS1n, NBDS2n, RBDS1n, RBDS2n pulse width low (min.)	RTU mode	12	-	ns

Table 5: Bus Adaptor Receiver Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T24	LOSC ↓ to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (hold max.)	CTU mode or RTU mode	10	-	ns
T25	LOSC ↓ to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup max.)	CTU mode or RTU mode	15	-	ns
T26	LOSC ↑↓ to TIMEOUTn valid	CTU mode or RTU mode	-	55	ns
	Timeout period = $16\tau_{LOSC}$	CTU mode or RTU mode	Guaranteed, not measured		
	Redundant to Dual or Redundant to Nominal bus changeover TIMEOUTn low reset period = τ_{LOSC}	CTU mode or RTU mode	Guaranteed, not measured		

Table 6: Clock Detector Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T27	RIRCLK ↓ to BCP(1:4), BCPVAL valid	CTU mode	-	70	ns
T28	RIRCLK ↓ to MLADD(0:4)	CTU mode	-	80	ns
T29	RIRCLK ↓ to MLDATA	CTU mode	-	80	ns
T30	RIRCLK ↓ to CHADD	CTU mode	-	75	ns
T31	RIRCLK ↓ to MOSC, MOLC, MOHL, MOBT, MODBL, MODS16, MODS8, MOANS, MOAND valid	CTU mode	-	70	ns
T32	RIRCLK ↓ to IRCLK, CTCLK, TRCLK valid	CTU mode	-	70	ns
T33	RIRCLK ↓ to PC, ANCLK, SOC, SH valid	CTU mode	-	70	ns
T34	RIRCLK ↓ to DATARRT, ENRRT valid	CTU mode	-	55	ns
T35	ANSIN to RIRCLK ↑ setup	RTU mode	0	-	ms
T35a	ANSIN to RIRCLK ↑ hold	RTU mode	30	-	ns
T36	NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ to DATARRT, ENRRT	RTU mode	-	75	ns

Note 1: RTU mode timing parameters not explicitly stated will be lower than the sum of the appropriate parameters for the RTU Kernel, BAR1 and BAT2. Parameters T34 and T36 above may be used to estimate the difference in timing between CTU mode (i.e. where the RTU Kernel, BAR1 and BAT2 are not coupled together) and RTU mode usage (i.e. where those components are coupled together).

Note 2: Configuration pins such as TA(0:5), EXTFMT, EXTMLA1 and EXTMLA2 and MRSTn are not considered here because they do not need to be dynamically changed.

Note 3: V_{DD} = 5V ±10% over full temperature range. $V_{OH} = V_{OL} = V_{DD}/2$, $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, C_L = 50pF.

Note 4: Total dose radiation not exceeding 10^5 Rads (Si).

Note 5: Tables 4, 5, 6 & 7 contain Mil-Std-883, method 5005, subgroups 9, 10, 11.

Table 7: RTU Kernel Characterisation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note 1: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Table 8: Capacitance

Symbol	Parameter	Conditions
F_T	Functionality	V_{DD} = 4.5 - 5.5V, FREQ = 1 MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} = V_{OH} = V_{DD}/2$ TEMP = -55˚C to +125˚C, GPS Pattern Set Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Table 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 3 at +25˚C
2	Static characteristics specified in Table 3 at +125˚C
3	Static characteristics specified in Table 3 at -55˚C
7	Functional characteristics specified in Table 9 at +25˚C
8A	Functional characteristics specified in Table 9 at +125˚C
8B	Functional characteristics specified in Table 9 at -55˚C
9	Switching characteristics specified in Tables 4 to 7 at +25˚C
10	Switching characteristics specified in Tables 4 to 7 at +125˚C
11	Switching characteristics specified in Tables 4 to 7 at -55˚C

Table 10: Definition of Subgroups

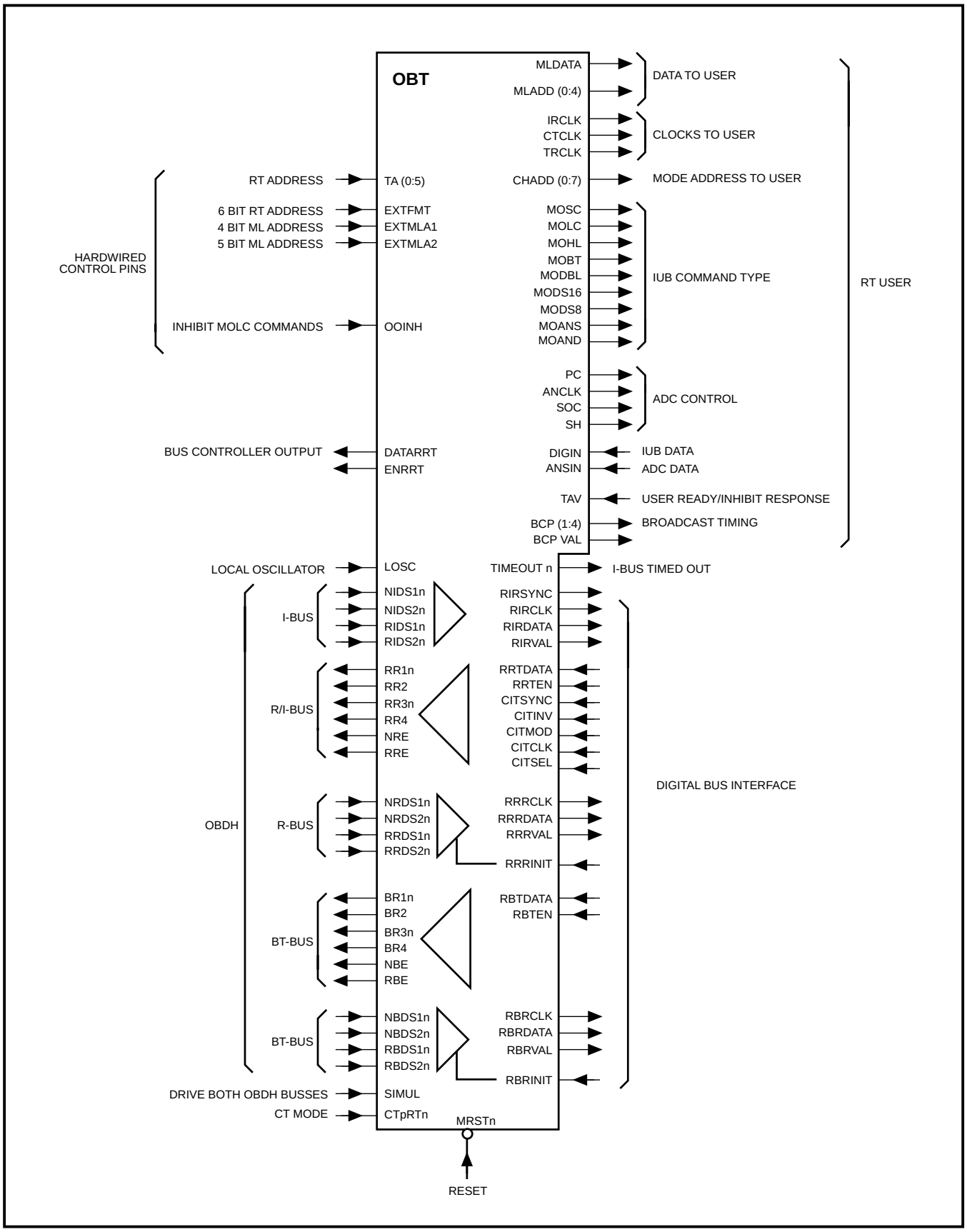


Figure 21: OBT Schematic

PIN ASSIGNMENT

OBT/IUB PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
45	IRCLK	O	Interrogation rate clock
46	CTCLK	O	Continuous clock
56	TRCLK	O	Transfer clock
79	MLDATA	O	Memory load data to user
78	MLADD0	O	Memory load address MSB (Interrogation bit 10)
77	MLADD1	O	Memory load address
76	MLADD2	O	Memory load address
75	MLADD3	O	Memory load address
74	MLADD4	O	Memory load address LSB (Interrogation bit 14)
73	CHADD0	O	Channel address 0 (Interrogation bit 23)
72	CHADD1	O	Channel address 1
71	CHADD2	O	Channel address 2
70	CHADD3	O	Channel address 3
69	CHADD4	O	Channel address 4
68	CHADD5	O	Channel address 5
67	CHADD6	O	Channel address 6
66	CHADD7	O	Channel address 7 (Interrogation bit 30)
65	MOSC	O	Mode short command (Interrogation mode bits 19/22 = 1 hex)
64	MOLC	O	Switch closure on/off command (mode 2)
63	MOHL	O	High power on/off command (mode 3)
62	MOBT	O	Mode block transfer (mode 7)
61	MODBL	O	Digital bi-level data acquisition (mode 8)
60	MODS16	O	16-bit serial digital data acquisition (mode A)
59	MODS8	O	8-bit serial digital data acquisition (mode B)
58	MOANS	O	Single ended analog data acquisition (mode C)
57	MOAND	O	Double ended analog acquisition (mode E)
131	PC	O	Power on to analog-to-digital converter
132	ANCLK	O	ADC shift clock
1	SOC	O	Start of conversion
2	SH	O	Sample/hold
42	DIGIN	I (PULL-DOWN)	Digital serial data input
43	ANSIN	I (PULL-DOWN)	Analog serial data input
3	BCP1	O	Broadcast pulse 1 (Interrogation bit 3)
4	BCP2	O	Broadcast pulse 2 (Interrogation bit 4)
5	BCP3	O	Broadcast pulse 3 (Interrogation bit 5)
6	BCP4	O	Broadcast pulse 4 (Interrogation bit 6 when extfmt = 0)
7	BCPVAL	O	Broadcast pulses valid
37	DATARRT	O	Data to RRT when used as RTU kernel
38	ENRRT	O	Enable RRT when used as RTU kernel

OBT/DBI PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
8	RIRSYNC	O/I (PULL-DOWN)	Sync from I-bus or (CT mode) input to RTU kernel
9	RIRCLK	O/I (PULL-DOWN)	Clock from I-bus or (CT mode) input to RTU kernel
10	RIRDATA	O/I (PULL-DOWN)	Data from I-bus or (CT mode) input to RTU kernel
11	RIRVAL	O/I (PULL-DOWN)	Validity from I-bus or (CT mode) input to RTU kernel
12	RRRCLK	O	Clock from R-bus
13	RRRDATA	O	Data from R-bus
21	RRRVAL	O	Validity from R-bus
22	RRRINIT	I (PULL-DOWN)	Initialise R-bus receiver
23	RRTDATA	I (PULL-DOWN)	Data to R-bus or (CT mode) to I-bus
24	RRTEN	I (PULL-DOWN)	Enable R-bus transmitter
25	CITSYNC	I (PULL-DOWN)	(CT mode) sync to I-bus
26	CITINV	I (PULL-DOWN)	(CT mode) invalid to I-bus
27	CITMOD	I (PULL-DOWN)	(CT mode) modulation to I-bus
28	CITCLK	I (PULL-DOWN)	(CT mode) clock to I-bus
29	CITSEL	I (PULL-DOWN)	(CT mode) select nominal or redundant I-bus
34	RBTDATA	I (PULL-DOWN)	Data to BT-bus
35	RBTEN	I (PULL-DOWN)	Enable BT-bus transmitter
30	RBRCLK	O	Clock from BT-bus
31	RBRDATA	O	Data from BT-bus
32	RBRVAL	O	Validity from BT-bus
33	RBRINIT	I (PULL-DOWN)	Initialise BT-bus receiver

OBT/OBDH PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
111	NIDS1n	I (PULL-UP) (CSCHMITT)	Nominal I-bus Discriminator Signal 1
110	NIDS2n	I (PULL-UP) (CSCHMITT)	Nominal I-bus Discriminator Signal 2
109	RIDS1n	I (PULL-UP) (CSCHMITT)	Redundant I-bus Discriminator Signal 1
108	RIDS2n	I (PULL-UP) (CSCHMITT)	Redundant I-bus Discriminator Signal 2
107	NRDS1n	I (PULL-UP) (CSCHMITT)	Nominal R-bus Discriminator Signal 1
106	NRDS2n	I (PULL-UP) (CSCHMITT)	Nominal R-bus Discriminator Signal 2
105	RRDS1n	I (PULL-UP) (CSCHMITT)	Redundant R-bus Discriminator Signal 1
104	RRDS2n	I (PULL-UP) (CSCHMITT)	Redundant R-bus Discriminator Signal 2
103	RR1n	O	R-bus driver 1
102	RR2	O	R-bus driver 2
101	RR3n	O	R-bus driver 3
100	RR4	O	R-bus driver 4
99	NRE	O	Nominal R-bus Enable
98	RRE	O	Redundant R-bus Enable
97	NBDS1n	I (PULL-UP) (CSCHMITT)	Nominal BT-bus Discriminator Signal 1
96	NBDS2n	I (PULL-UP) (CSCHMITT)	Nominal BT-bus Discriminator Signal 2
95	RBDS1n	I (PULL-UP) (CSCHMITT)	Redundant BT-bus Discriminator Signal 1
94	RBDS2n	I (PULL-UP) (CSCHMITT)	Redundant BT-bus Discriminator Signal 2
93	BR1n	O	BT-bus driver 1
92	BR2	O	BT-bus driver 2
91	BR3n	O	BT-bus driver 3
90	BR4	O	BT-bus driver 4
89	NBE	O	Nominal BT-bus enable
88	RBE	O	Redundant BT-bus enable

OBT CONTROL PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
121	TA0	I	Terminal Address bit 0 (MSB = I-bus bit 6)
122	TA1	I	Terminal Address bit 1
123	TA2	I	Terminal Address bit 2
124	TA3	I	Terminal Address bit 3
125	TA4	I	Terminal Address bit 4
126	TA5	I	Terminal Address bit 5
127	EXTFMT	I	Extended format Enable
128	EXTMLA1	I	Extended Memory Load Address 1 Enable
129	EXTMLA2	I	Extended Memory Load Address 2 Enable
130	OOINH	I	On/Off INHibit of MOLC commands
40	TEST	I	Tie to Ground (this input for test purposes only)
87	SIMUL	I (PULL-DOWN)	Simultaneously drive both busses
41	CTpRTn	I (PULL-UP)	CT mode when high, RT mode when low
36	MRSTn	I (PULL-DOWN) (CSCHMITT)	Master reset when low
112	LOSC	I (CSCHMITT)	Oscillator from user to drive OBT timeout
39	TIMEOUTn	O	Low when I-bus timeout
44	TAV	I (PULL-DOWN)	Terminal available (take low to disable responses from RTU kernal)

OBT POWER SUPPLY DISTRIBUTION PINS

No.	Name	Type	Description
55, 113	V_{DD}	P	Positive supply nominally +5 volts. Connect both pins.
14, 47, 80	V_{SS}	P	Power and signal ground. Connect all pins.

Notes: 1. CSCHMITT means CMOS Schmitt-trigger inputs.
2. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.59	-	-	0.102
A1	1.37	-	1.88	0.054	-	0.074
b	0.23	-	0.33	0.009	-	0.013
c	0.10	-	0.18	0.004	-	0.007
D1, D2	-	-	24.38	-	-	0.960
E	-	-	18.11	-	-	0.713
E2	-	20.32	-	-	0.800	-
e	-	0.63	-	-	0.025	-
L	6.35	-	7.11	0.250	-	0.280

XG533

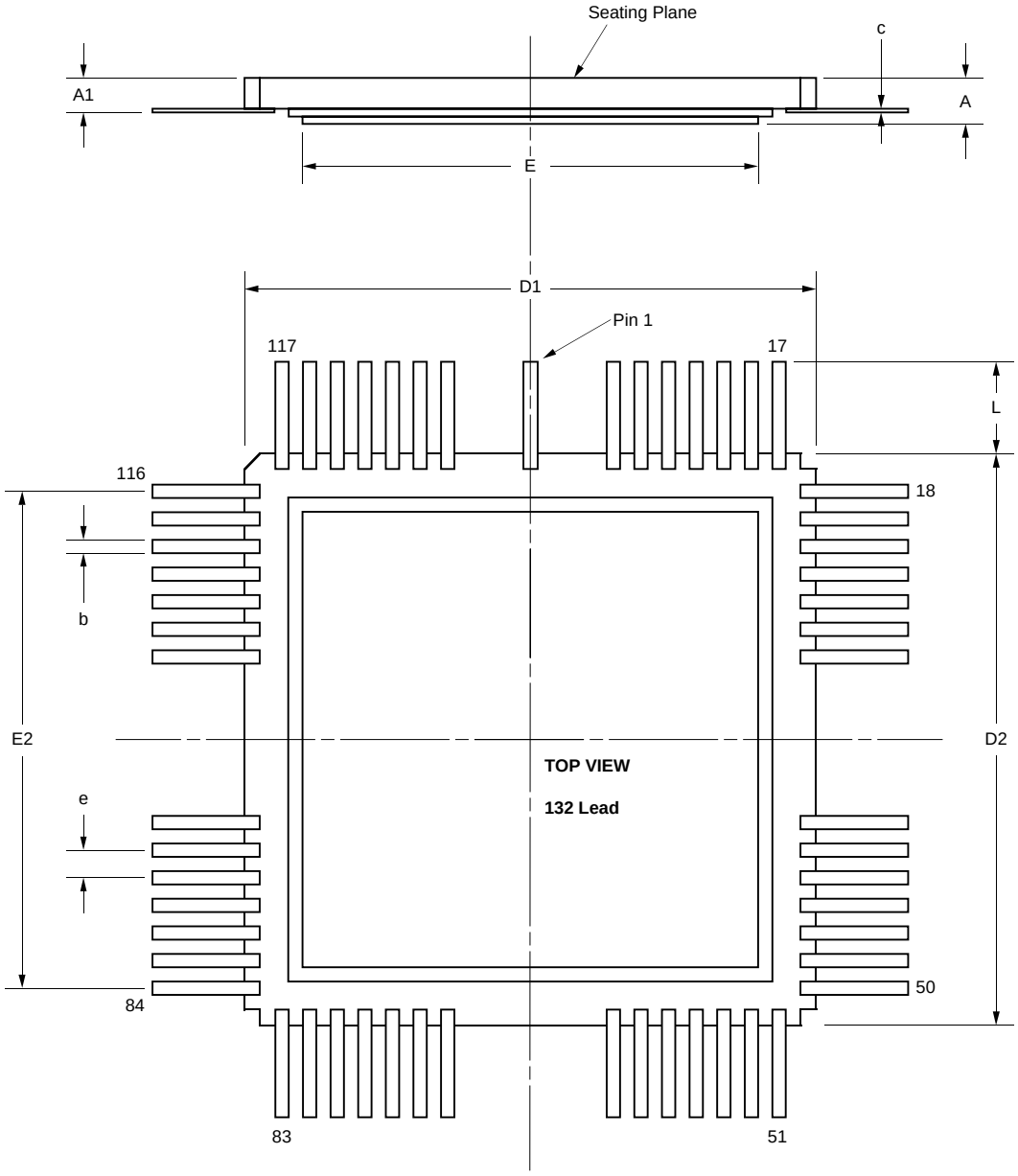


Figure 22: Package Dimensions

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019 Ionizing Radiation (total dose).

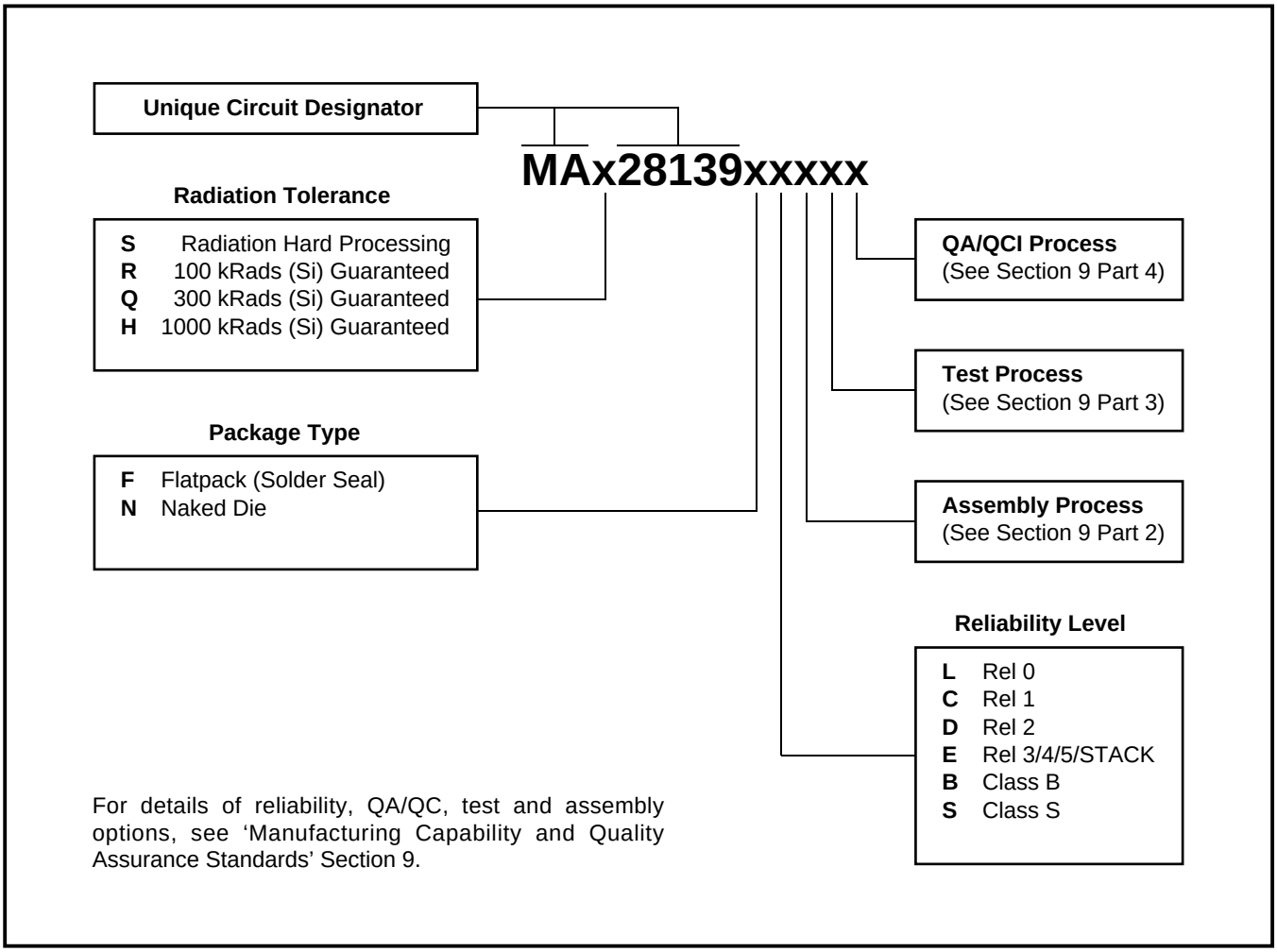
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 11: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

SYNONYMS

ASIC	Application Specific Integrated Circuit
BT-bus	Block Transfer Bus
CBR	CTU mode, block transfer bus, receive
CBT	CTU mode, block transfer bus, transmit
CIT	CTU mode, interrogation unit, transmit
CRR	CTU mode, response bus, receive
CT	Central terminal
DBI	Digital bus interface
DBU	Digital bus unit
ESA	European Space Agency
FET	Field effect transistor
FTC	Fault tolerant computer
GPS	GEC Plessey Semiconductors
I-bus	Interrogation bus
ICU	Intelligent control unit
IUB	Internal user bus
MA28138	Remote bus interface (RBI) ASIC
MA28139	OBDH bus terminal (OBT) ASIC
µP	Microprocessor
MSS	Marconi Space Systems - now Matra Marconi Space (MMS)
OBDH	On board data handling
OBT	OBDH bus terminal (MA28139)
PIU	Payload interface unit
R-bus	Response bus
RBI	Remote bus interface (MA28138)
RBR	RTU mode, block transfer bus, receive
RBT	RTU mode, block transfer bus, transmit
RIR	RTU mode, interrogation bus, receive
RRR	RTU mode, response bus, receive
RRT	RTU mode, response bus, transmit
RT	Remote terminal
SBC	Single board computer
VLSI	Very large scale integration

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

DYNEX SEMICONDUCTOR

http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: +44-(0)1522-500500
Fax: +44-(0)1522-500550

CUSTOMER SERVICE
Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020

SALES OFFICES
Benelux, Italy & Switzerland: Tel: +33 (0)1 64 66 42 17. Fax: +33 (0)1 64 66 42 19.
France: Tel: +33 (0)2 47 55 75 52. Fax: +33 (0)2 47 55 75 59.
Germany, Northern Europe, Spain & Rest Of World: Tel: +44 (0)1522 502753 / 502901.
Fax: +44 (0)1522 500020
North America: Tel: (613) 723-7035. Fax: (613) 723-1518. Toll Free: 1.888.33.DYNEX (39639) /
Tel: (949) 733-3005. Fax: (949) 733-2986.

These offices are supported by Representatives and Distributors in many countries world-wide.

Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hard corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.