

MAC12HCDG, MAC12HCMG, MAC12HCNG

Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave ac control applications, such as motor controls, heating controls or dimmers; or wherever full-wave, silicon gate-controlled devices are needed.

Features

- Uniform Gate Trigger Currents in Three Quadrants, Q1, Q2, and Q3
- High Commutating di/dt and High Immunity to dv/dt @ 125°C
- Minimizes Snubber Networks for Protection
- Blocking Voltage to 800 Volts
- On-State Current Rating of 12 Amperes RMS at 80°C
- High Surge Current Capability – 100 Amperes
- Industry Standard TO-220AB Package for Ease of Design
- Glass Passivated Junctions for Reliability and Uniformity
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T _J = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM} , V _{RRM}	400 600 800	V
On-State RMS Current (All Conduction Angles; T _C = 80°C)	I _{T(RMS)}	12	A
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T _J = 125°C)	I _{TSM}	100	A
Circuit Fusing Consideration (t = 8.33 ms)	I ² t	41	A ² sec
Peak Gate Power (Pulse Width ≤ 1.0 μs, T _C = 80°C)	P _{GM}	16	W
Average Gate Power (t = 8.3 ms, T _C = 80°C)	P _{G(AV)}	0.35	W
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

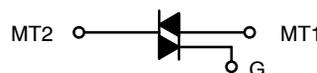
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



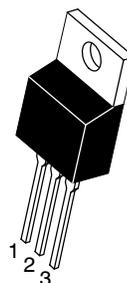
ON Semiconductor®

<http://onsemi.com>

TRIACS
12 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO-220AB
CASE 221A-09
STYLE 4

- x = D, M, or N
- A = Assembly Location (Optional)*
- Y = Year
- WW = Work Week
- G = Pb-Free Package

* The Assembly Location code (A) is optional. In cases where the Assembly Location is stamped on the package the assembly code may be blank.

PIN ASSIGNMENT

Pin	Assignment
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC12HCDG	TO-220AB (Pb-Free)	50 Units / Rail
MAC12HCMG	TO-220AB (Pb-Free)	50 Units / Rail
MAC12HCNG	TO-220AB (Pb-Free)	50 Units / Rail

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}, V_{RRM}, \text{ Gate Open}$)	I_{DRM}, I_{RRM}	-	-	0.01	mA
	$T_J = 25^{\circ}\text{C}$	-	-	2.0	
	$T_J = 125^{\circ}\text{C}$	-	-		

ON CHARACTERISTICS

Peak On-State Voltage (Note 2) ($I_{TM} = \pm 17 \text{ A}$)	V_{TM}	-	-	1.85	V
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	I_{GT}	10	-	50	mA
MT2(+), G(+)		10	-	50	
MT2(+), G(-)		10	-	50	
MT2(-), G(-)		10	-	50	
Holding Current ($V_D = 12 \text{ V}, \text{ Gate Open}, \text{ Initiating Current} = \pm 150 \text{ mA}$)	I_H	-	-	60	mA
Latch Current ($V_D = 12 \text{ V}, I_G = 50 \text{ mA}$)	I_L	-	-	60	mA
MT2(+), G(+)		-	-	80	
MT2(+), G(-)		-	-	60	
MT2(-), G(-)		-	-	60	
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	V_{GT}	0.5	-	1.5	V
MT2(+), G(+)		0.5	-	1.5	
MT2(+), G(-)		0.5	-	1.5	
MT2(-), G(-)		0.5	-	1.5	

DYNAMIC CHARACTERISTICS

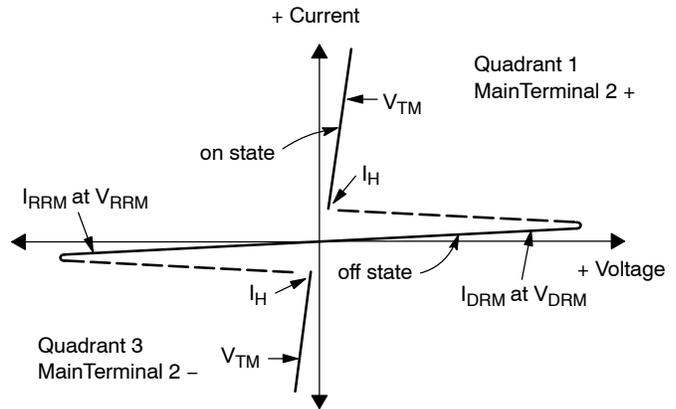
Rate of Change of Commutating Current ($V_D = 400 \text{ V}, I_{TM} = 4.4 \text{ A}, \text{ Commutating } dv/dt = 18 \text{ V}/\mu\text{s}, \text{ Gate Open},$ $T_J = 125^{\circ}\text{C}, f = 250 \text{ Hz}, C_L = 10 \mu\text{F}, L_L = 40 \text{ mH}, \text{ with Snubber}$)	$(di/dt)_c$	15	-	-	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}, \text{ Exponential Waveform},$ $\text{ Gate Open}, T_J = 125^{\circ}\text{C}$)	dv/dt	600	-	-	V/ μs
Repetitive Critical Rate of Rise of On-State Current $\text{ IPK} = 50 \text{ A}; \text{ PW} = 40 \mu\text{sec}; di_G/dt = 200 \text{ mA}/\mu\text{sec}; f = 60 \text{ Hz}$	di/dt	-	-	10	A/ μs

2. Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.

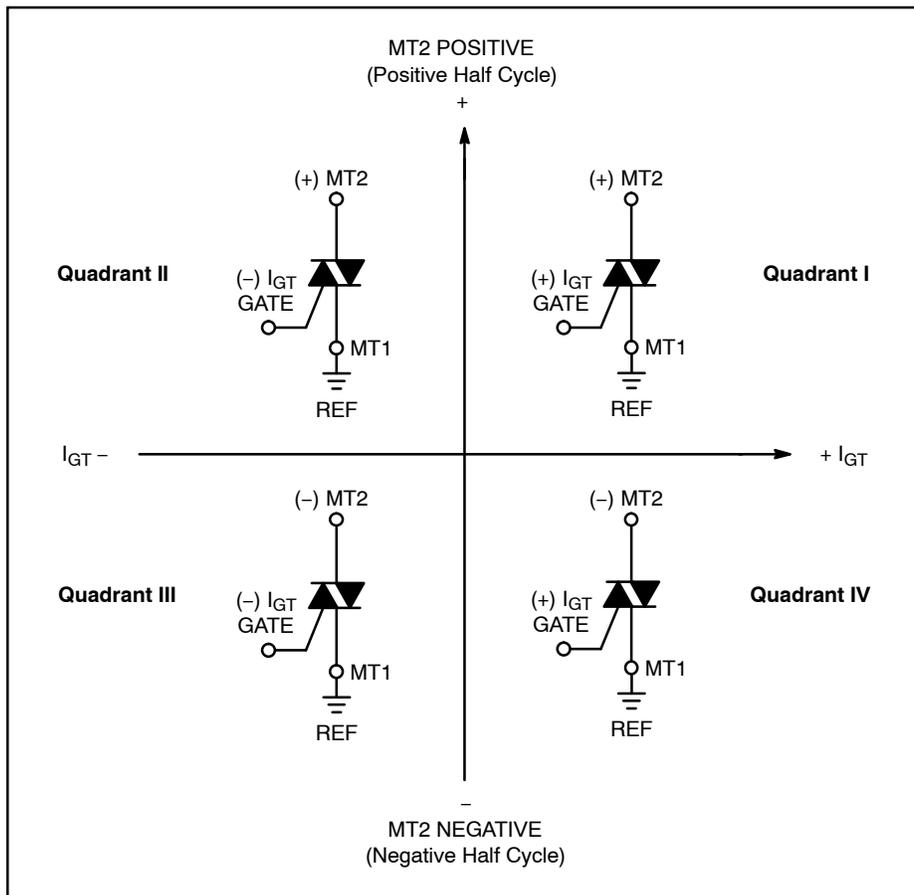
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Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.

With in-phase signals (using standard AC lines) quadrants I and III are used.

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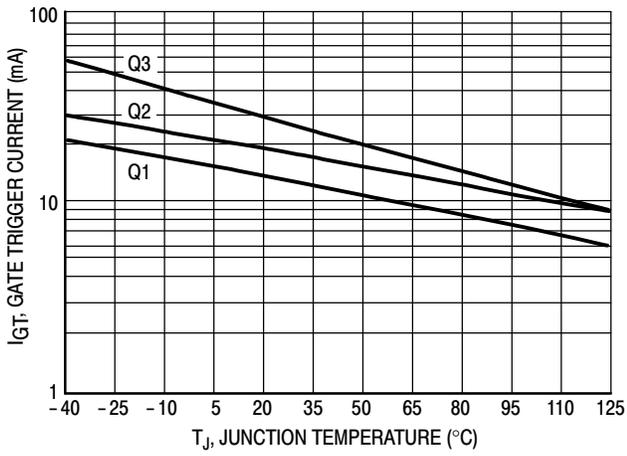


Figure 1. Typical Gate Trigger Current versus Junction Temperature

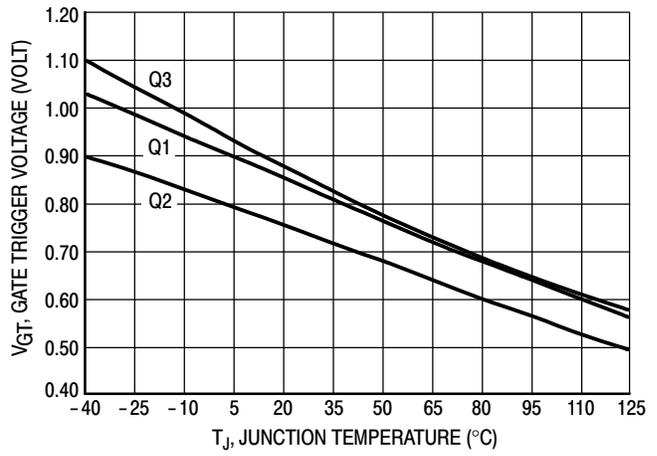


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

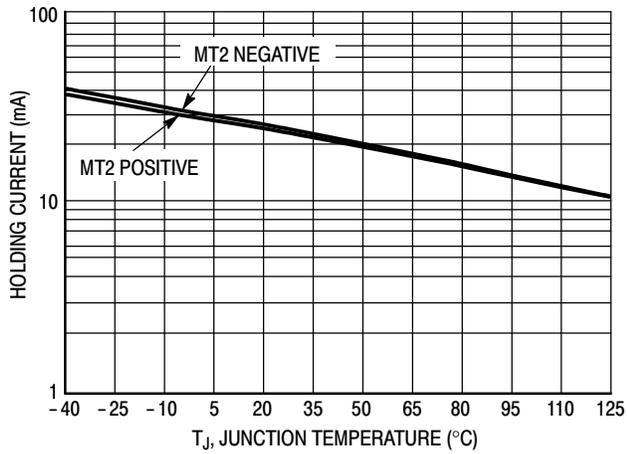


Figure 3. Typical Holding Current versus Junction Temperature

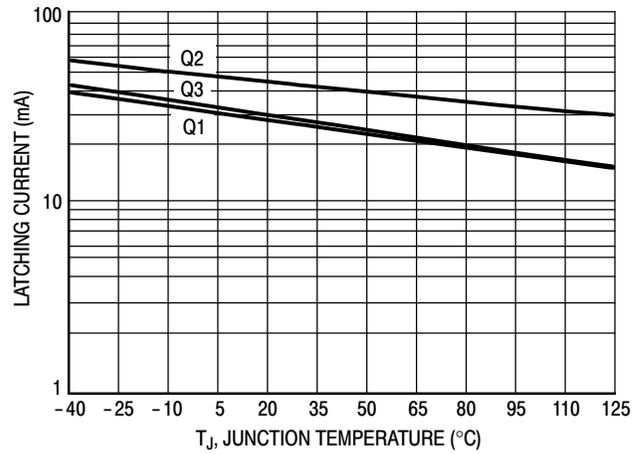


Figure 4. Typical Latching Current versus Junction Temperature

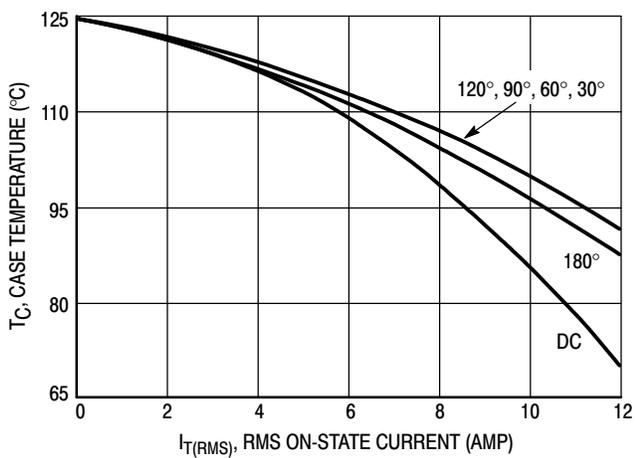


Figure 5. Typical RMS Current Derating

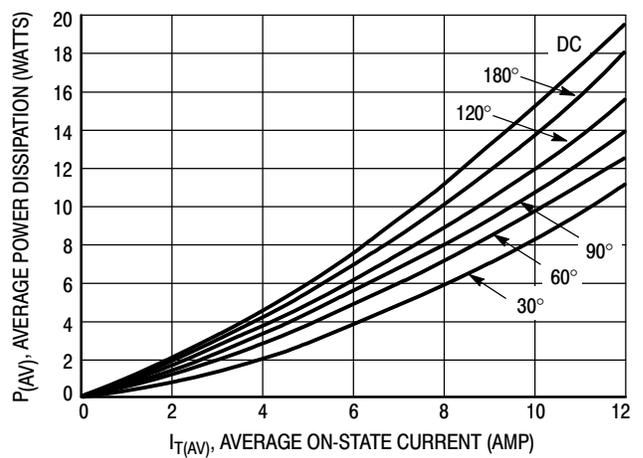


Figure 6. On-State Power Dissipation

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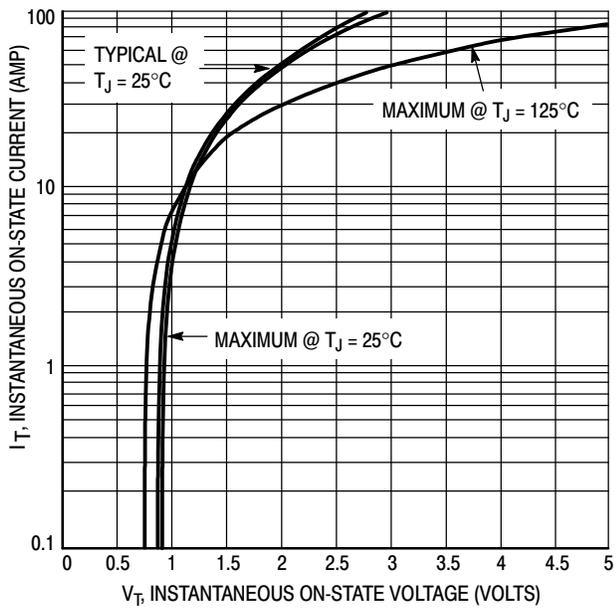


Figure 7. Typical On-State Characteristics

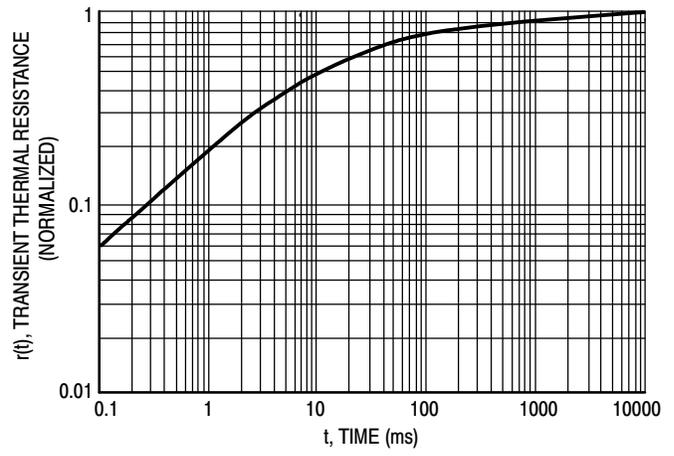
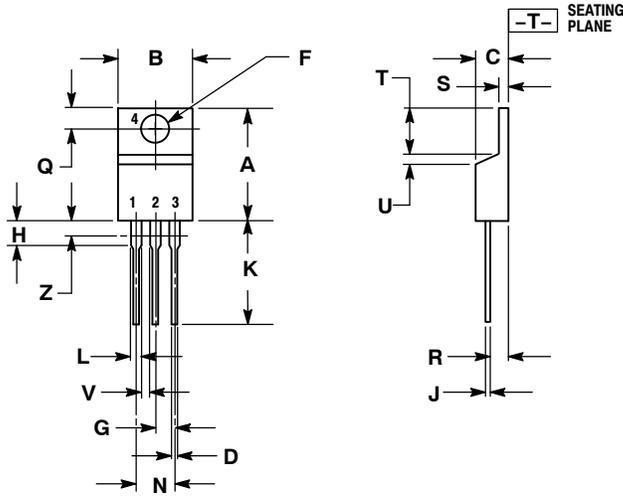


Figure 8. Typical Thermal Response

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PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AG



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

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