EVALUATION KIT AVAILABLE

MAX14983E

Enhanced 1:2 VGA Mux with Monitor Detection and Priority Port Logic

General Description

The MAX14983E integrates high-bandwidth analog switches, level-translating buffers, and 5V power switches to implement a complete 1:2 multiplexer for VGA monitors. The device switches graphics signals between a controller and two outputs. Integrated pullup resistors (2.2kΩ typ) are provided on the monitor-side display data channel (DDC) signal lines.

The device features a simple power interface that operates with a single +5V supply input. Two integrated power switches with current limiting and reverse-current protection pass the +5V supply to external loads with minimal voltage drop.

The horizontal and vertical synchronization (HSYNC/VSYNC) buffers shift logic levels to support +2.5V to +5.0V CMOS or TTL-compatible graphics controllers while meeting the VESA drive capability requirement of ±8mA. An internal 2.5V regulator translates the DDC voltage levels to be compatible with low-voltage graphics controllers.

The device also features monitor-detect outputs and enable inputs that allow monitor switching to operate either automatically or with inputs from the graphics controller.

The MAX14983E is available in a 32-pin (5mm x 5mm) TQFN package, and is specified over the -40°C to +85°C extended temperature range.

Applications

Servers

KVM Switches

Computing

Graphics Cards

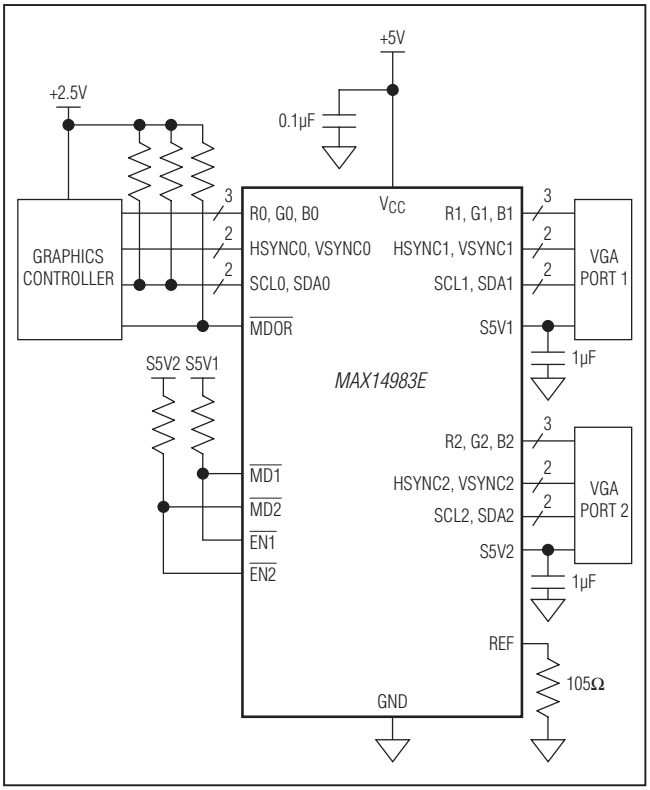
***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX14983E.related**.

Benefits and Features

- **Design Flexibility**
  - **Graphics Controller Port is Protected when V_{CC} = 0V**
  - **DDC Switches Limit Voltage to Low-Voltage Supply**
  - **Internal +2.5V Regulator**
- **High Level of Integration for Enhanced Performance**
  - **Low 5.5pF (typ) RGB Capacitance**
  - **2.0ns (typ) t_R/t_F with 10pF, 2.2kΩ Load on Monitor-Side SYNC Signals**
  - **Source and Sink 8mA While Meeting Speed Requirements**
  - **±11kV Human Body Model (HBM)**
- **Saves Space on Board**
  - **Internal Power Switches**
    Pass +5V with 300mV (max) IR Drop
    Short-Circuit/Thermal/Reverse-Current Protection
  - **5mm x 5mm, 32-Pin TQFN Package**

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5935; Rev 0; 6/11

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V_{CC}, S5V1, S5V2, SDA_, SCL_, REF, $\overline{MD\_}$, $\overline{EN\_}$, $\overline{MDOR}$ ..... -0.3V to +6V

HSYNC_, VSYNC_, R_, G_, B_..... -0.3V to (V_{CC} + 0.3V)

Continuous Current Through R_, G_, B_ Switches..... ±50mA

Continuous Current Through SDA_, SCL_ Switches ..... ±50mA

Continuous Current Through S5V_ ..... ±750mA

Peak Current Through R_, G_, B_, SDA_, SCL_ (10% duty cycle) ..... ±100mA

Continuous Power Dissipation (T_A = +70°C)

TQFN (derate 34.5mW/°C above +70°C).....2758.6mW

Operating Temperature Range ..... -40°C to +85°C

Junction Temperature .....+150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) .....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Quiescent Current	I_Q	V_{CC} = 5.25V, $V_{\overline{EN1}}$ = $V_{\overline{EN2}}$ = V_{CC}, REF unconnected		50	150	µA
Operating Current	I_{CC}	HSYNC0 = 50kHz, VSYNC0 = 60Hz 10% duty cycle, R_L on SYNC outputs = 2kΩ, REF unconnected		1.5	2.7	mA
5V SWITCH (S5V1, S5V2 OUTPUTS)						
S5V_ Voltage Drop	V_{S5V}	I_{OUT} = 55mA			0.3	V
Reverse Leakage Current	I_L	V_{CC} = 0V, $V_{\overline{EN1}}$ = $V_{\overline{EN2}}$ = 0V, V_{S5V1} = V_{S5V2} = 5.25V, no load on S5V1 or S5V2			10	µA
Pulldown Resistor	R_{S5V1}, R_{S5V2}	V_{S5V1} = V_{S5V2} = 1V, $V_{\overline{EN1}}$ = $V_{\overline{EN2}}$ = V_{CC}		250		Ω
Output Current Limit	I_{LIM}		55	300	500	mA
Thermal-Shutdown Threshold	T_{SHDN}			+150		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			25		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DDC SWITCHES (SDA_, SCL_ INPUTS/OUTPUTS)						
Input Leakage Current	I_L	$V_{\overline{EN1}}$ = V_{CC}, $V_{\overline{EN2}}$ = V_{CC}, V_{IN} = 0V or 5.25V	-1		+1	µA
Off-Leakage Current	I_{LOFF}	V_{IN} = +5.25V, V_{CC} = 0V			10	µA
On-Resistance	R_{ON}	V_{IN} = 0.8V, $I_{SDA\_}$ = $I_{SCL\_}$ = ±10V		25		Ω
SDA1, SDA2, SCL1, SCL2 Internal Pullup Resistance	R_{PULLUP}	$V_{SDA\_}$ = $V_{SCL\_}$ = 4V		2.2		kΩ
CONTROL SIGNALS (HSYNC_, VSYNC_, $\overline{EN\_}$ INPUTS/OUTPUTS)						
Input Logic-Low Voltage	V_{IL}	HSYNC0, VSYNC0, $\overline{EN1}$, $\overline{EN2}$			0.8	V
Input Logic-High Voltage	V_{IH}	HSYNC0, VSYNC0, $\overline{EN1}$, $\overline{EN2}$	2			V
Output Logic-Low Voltage	V_{OL}	HSYNC1, HSYNC2, VSYNC1, VSYNC2, I_{SINK} = 8mA			0.5	V
Output Logic-High Voltage	V_{OH}	HSYNC1, HSYNC2, VSYNC1, VSYNC2, I_{SOURCE} = 8mA	2.4			V
Rise Time/Fall Time	t_R, t_F	HSYNC0 input t_R/t_F < 5ns, 10% to 90%		2		ns
MONITOR DETECTION OUTPUTS ($\overline{MD\_}$, $\overline{MDOR}$)						
Output-Voltage Low	V_{OL}	R_{PULLUP} = 3.3kΩ, V_{PU} = 3.3V (Note 3)			0.3	V
Input Leakage Current	I_{LOD}	V_{IN} = 3.3V, $\overline{MD\_}$ and $\overline{MDOR}$ deasserted			1	µA
R_, G_, B_ SWITCH PERFORMANCE						
Bandwidth	f_{MAX}	Figure 1, R_S = R_L = 50Ω		800		MHz
On-Loss	I_{LOSS}	Figure 1, f = 50MHz, R_S = R_L = 50Ω		-0.6		dB
On-Resistance	R_{ON}	I_{IN} = ±10mA, V_{IN} = 0.7V		5	8	Ω
On-Resistance Matching	ΔR_{ON}	I_{IN} = ±10mA, V_{IN} = 0 to 0.7V			1	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	I_{IN} = ±10mA, V_{IN} = 0 to 0.7V		0.5	1	Ω
B1, B2 Internal Pullup Resistance	R_B			2.5		kΩ
Off-Leakage Current	I_{LOFF}	$V_{R\_}$ = $V_{G\_}$ = V_{B0} = 0V or V_{CC}	-1		+1	µA
Off-Capacitance	C_{OFF}	f = 1MHz; R0, G0, B0 to R_, G_, B_		2.5		pF
On-Capacitance	C_{ON}	f = 1MHz; R0, G0, B0 to R_, G_, B_		5.5		pF
ESD PROTECTION						
High-ESD Pins ESD Protection		Human Body Model (Note 4)		±11		kV
All Other Pins ESD Protection		Human Body Model (Note 4)		±2		kV

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: V_{PU} is the pullup voltage.
Note 4: See the *Pin Description* section for the ESD status of each pin.

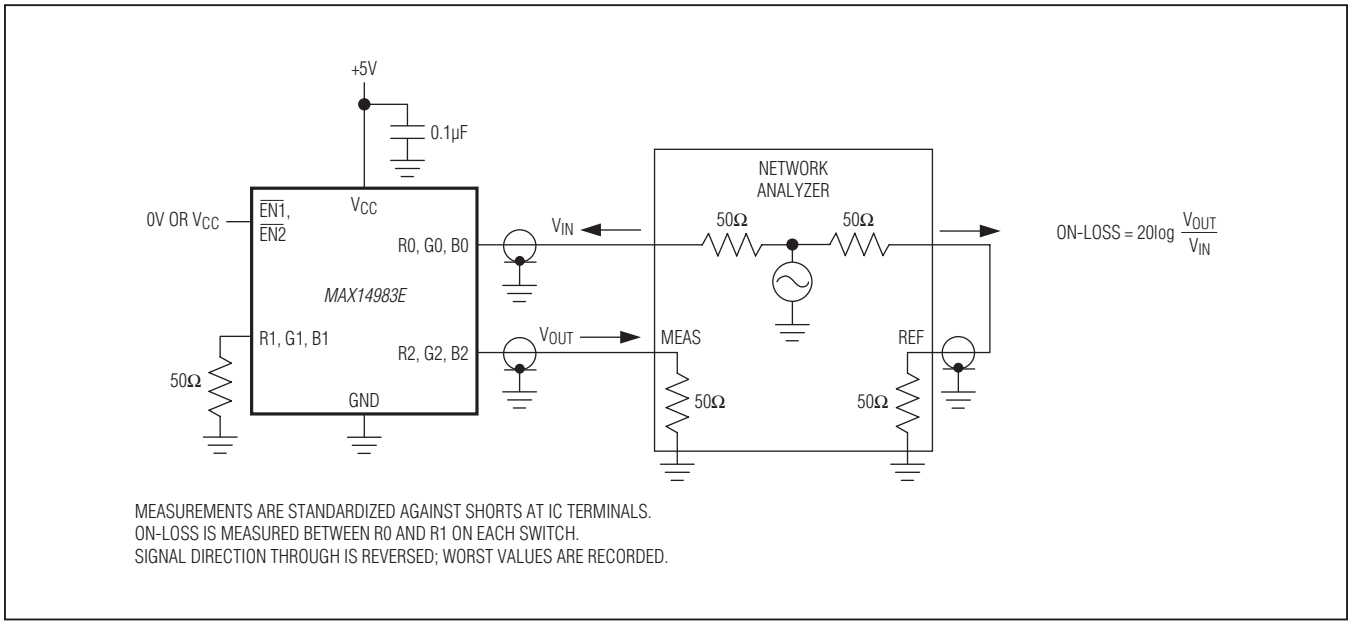
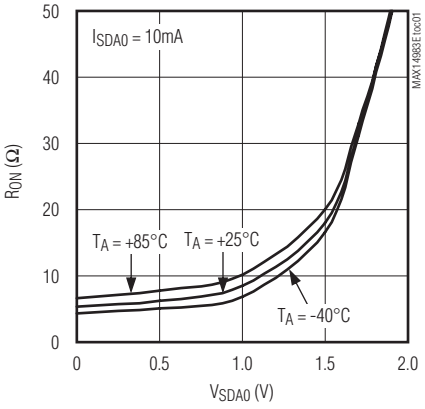


Figure 1. On-Loss

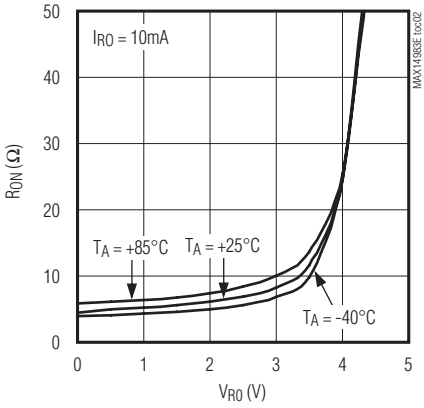
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

DDC ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



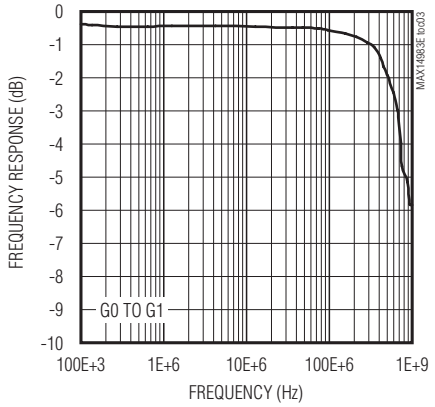
RGB ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



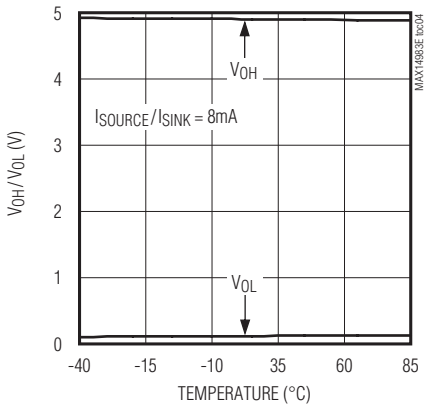
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

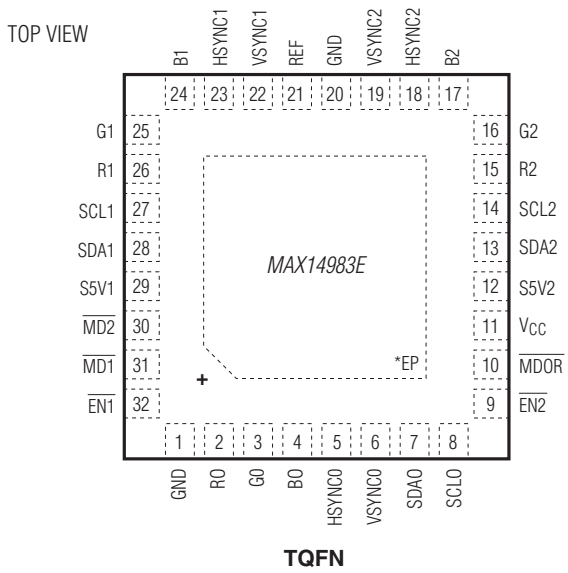
FREQUENCY RESPONSE



HSYNC_/VSYNC_ OUTPUT VOLTAGE vs. TEMPERATURE



Pin Configuration



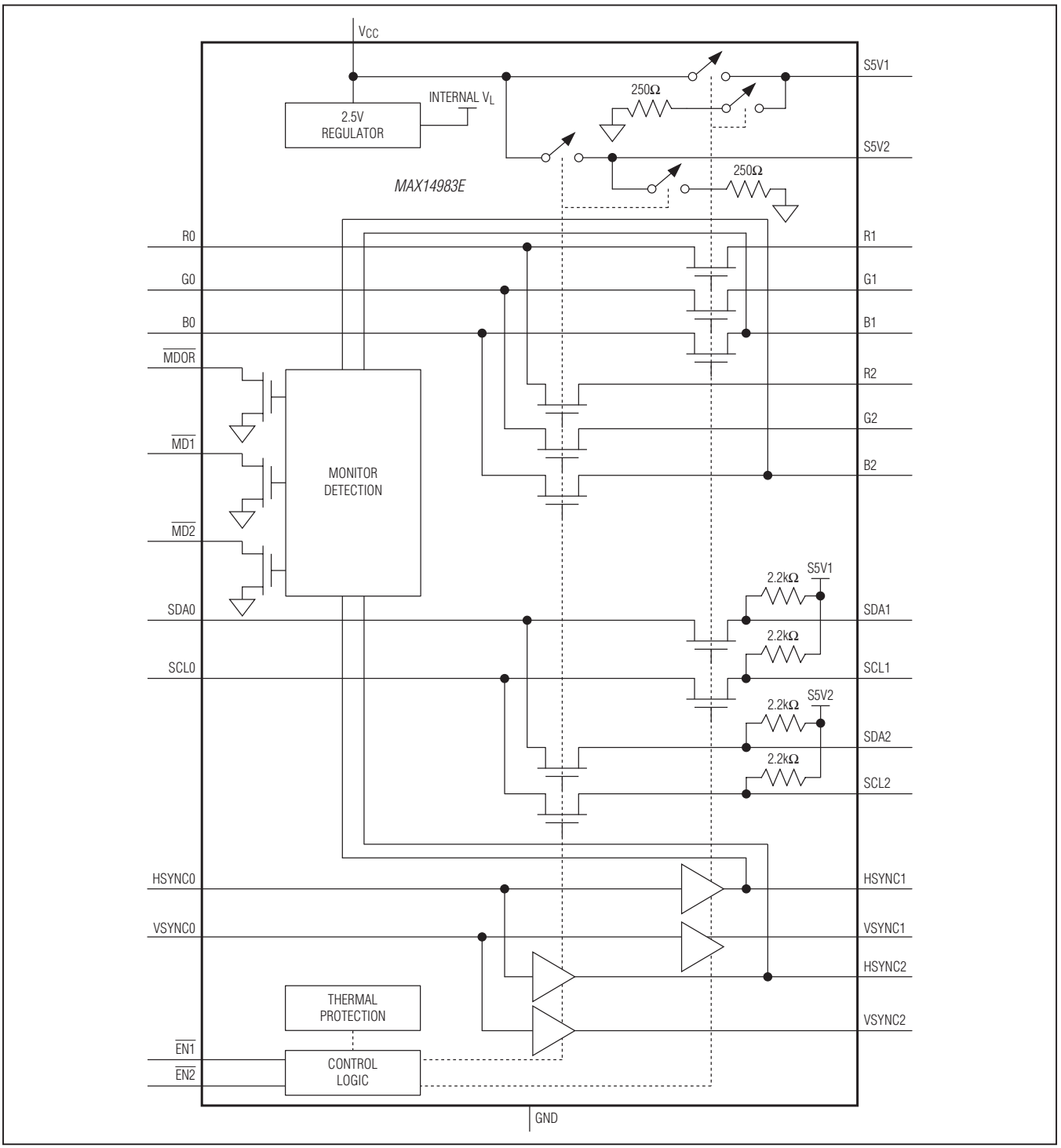
TQFN

*CONNECT EP TO GND.

Pin Description

PIN	NAME	FUNCTION	ESD
1, 20	GND	Ground	—
2	R0	RGB Analog Input	Standard
3	G0	RGB Analog Input	Standard
4	B0	RGB Analog Input	Standard
5	HSYNC0	Horizontal Sync Input	Standard
6	VSYNC0	Vertical Sync Input	Standard
7	SDA0	DDC Input/Output	Standard
8	SCL0	DDC Input/Output	Standard
9	$\overline{EN2}$	Active-Low Enable Input 2. Assert $\overline{EN2}$ to connect the graphics controller to the monitor on port 2 (see Table 1).	Standard
10	$\overline{MDOR}$	Logic NOR Output of $\overline{MD1}$ and $\overline{MD2}$. $\overline{MDOR}$ asserts whenever a monitor is detected on either port. $\overline{MDOR}$ is an active-low, open-drain output.	Standard
11	V_{CC}	Supply Voltage. V_{CC} = +5.0V ±5%. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor as close as possible to V_{CC}.	Standard
12	S5V2	Switched 5V Out 2. S5V2 is internally pulled down when not connected.	High
13	SDA2	DDC Input/Output. SDA2 has a 2.2kΩ (typ) internal pullup resistor to S5V2.	High
14	SCL2	DDC Input/Output. SCL2 has a 2.2kΩ (typ) internal pullup resistor to S5V2.	High
15	R2	RGB Analog Output for Port 2	High
16	G2	RGB Analog Output for Port 2	High
17	B2	RGB Analog Output for Port 2	High
18	HSYNC2	Horizontal Sync Output for Port 2	High
19	VSYNC2	Vertical Sync Output for Port 2	High
21	REF	Monitor-Detection Reference. Connect a 105Ω ±1% resistor from REF to ground.	Standard
22	VSYNC1	Vertical Sync Output for Port 1	High
23	HSYNC1	Horizontal Sync Output for Port 1	High
24	B1	RGB Analog Output for Port 1	High
25	G1	RGB Analog Output for Port 1	High
26	R1	RGB Analog Output for Port 1	High
27	SCL1	DDC Input/Output. SCL1 has a 2.2kΩ (typ) internal pullup resistor to S5V1.	High
28	SDA1	DDC Input/Output. SDA1 has a 2.2kΩ (typ) internal pullup resistor to S5V1.	High
29	S5V1	Switched 5V Out 1. S5V1 is internally pulled down when not connected.	High
30	$\overline{MD2}$	Monitor-Detect Output 2. $\overline{MD2}$ asserts when a monitor is detected on port 2. $\overline{MD2}$ is an active-low, open-drain output.	Standard
31	$\overline{MD1}$	Monitor-Detect Output 1. $\overline{MD1}$ asserts when a monitor is detected on port 1. $\overline{MD1}$ is an active-low, open-drain output.	Standard
32	$\overline{EN1}$	Enable Input 1. Assert $\overline{EN1}$ to connect the graphics controller to the monitor on port 1 (see Table 1).	Standard
—	EP	Exposed Pad. Connect exposed pad to GND.	—

Functional Diagram



Truth Tables

Table 1. Channel Selection

$\overline{EN1}$	$\overline{EN2}$	VGA CONTROLLER CONNECTED TO
0	0	Port 1
0	1	Port 1
1	0	Port 2
1	1	Not Connected

Note: *The B_ switches are unconnected if the HSYNC_ input is idle.*

Table 2. Monitor Detection

MONITOR 1 DETECTED	MONITOR 2 DETECTED	$\overline{MD1}$	$\overline{MD2}$	$\overline{MDOR}$
No	No	1	1	1
No	Yes	1	0	0
Yes	No	0	1	0
Yes	Yes	0	0	0

Note: *$\overline{MD1}$, $\overline{MD2}$, and $\overline{MDOR}$ function regardless of the state of the $\overline{EN\_}$ inputs.*

Detailed Description

The MAX14983E integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 multiplexer for VGA signals. The device provides switching for red-green-blue (RGB) signals, horizontal and vertical synchronization (HSYNC/VSYNC) pulses, display data channel (DDC) signals, and 5V power supplies. The power switches provide +5V power with current limiting and reverse-voltage protection.

The device uses a simplified power-supply interface that operates from a single +5V supply. An internal 2.5V regulator limits the voltage passed by the DDC switches to provide compatibility with low-voltage graphics controllers.

The device features two enable inputs and three monitor-detection outputs. This interface signals to the graphics controller when a monitor is inserted or removed from either of the VGA ports and allows it to switch between them. Alternatively, these signals can be connected together to automatically select the port when a monitor is plugged in. A dedicated output ($\overline{MDOR}$) signals the graphics controller when any monitor is detected.

5V Power Switches (S5V1, S5V2)

The device provides a switched +5V output in addition to the regular VGA signals (S5V1 and S5V2). Each output can supply 55mA with less than 300mV drop from V_{CC}. The S5V_ outputs tolerate +5V while turned off.

The power switches are protected against overcurrent and overtemperature faults. The device limits current supplied to each monitor side to 300mA (typ). Thermal-protection circuitry shuts off the switch when the temperature exceeds +150°C. The device is re-enabled once the temperature has fallen below +125°C.

Each power switch output has a 250Ω (typ) pulldown resistor to discharge filter capacitors when the switch is off.

RGB Switches

The device provides three single-pole/double-throw (SPDT) high-bandwidth switches to route the standard VGA R, G, and B signals (Table 1). The R, G, and B analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals.

Horizontal/Vertical Sync Multiplexer

The HSYNC_/VSYNC_ signals are buffered to provide level shifting and drive capability to meet the VESA specification. HSYNC_/VSYNC_ signals are only routed to the port selected by $\overline{EN2}$ and $\overline{EN1}$ (Table 1). HSYNC_ and VSYNC_ are not interchangeable.

Display Data Channel Multiplexer (SDA_, SCL_)

The device provides two voltage-limited SPDT switches to route DDC signals (SDA_, SCL_). These switches limit the voltage that can be passed through to the graphics controller to less than 2.5V. Internal pullup resistors on the monitor side of the switches translate the graphics controller signals to 5V compatible logic. Connect pullup resistors on SCL0 and SDA0 to define the logic level of the graphics controller.

The SDA_ and SCL_ switches are identical, and either of these two switches can be used to route SDA or SCL I^2C signals.

Applications Information

1:2 Multiplexer for Low-Voltage Graphics Controllers

The device provides the level shifting necessary to drive two standard VGA ports using a single graphics controller. Internal buffers drive the HSYNC_ and VSYNC_ signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by limiting signal levels to less than 2.5V.

Power-Supply Decoupling

Bypass V_{CC} to ground with a 1µF or larger ceramic capacitor as close as possible to the device.

PCB Layout

High-speed switches such as the MAX14983E require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to a solid ground plane.

High-ESD Protection

Electrostatic discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. All outputs are further protected against ESD up to ±11kV (HBM) without damage (see the *Pin Description*).

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the device continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test methodology and results.

Human Body Model

Figure 2 shows the Human Body Model. Figure 3 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

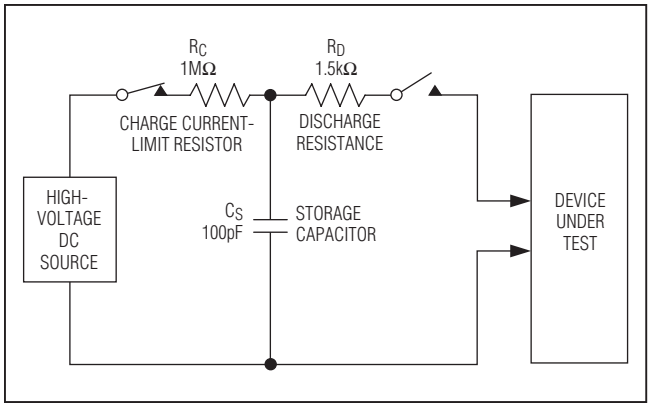


Figure 2. Human Body ESD Test Model

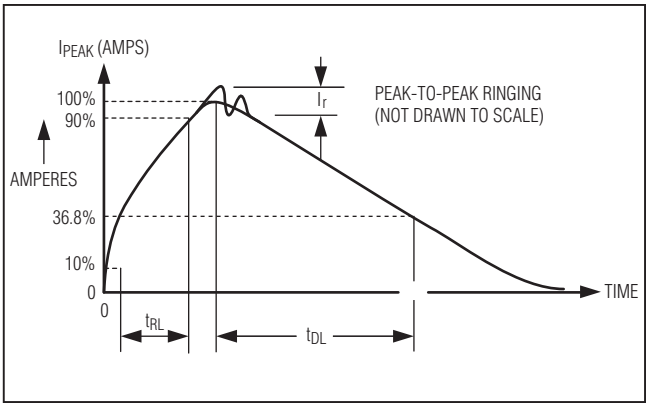


Figure 3. Human Body Current Waveform

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14983EETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—