ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +6V
V_{DD} to V_{SS} ..... -0.3V, +12V
V_{DD} to AGND ..... -0.3V, +6V
Digital Outputs and Inputs to DGND ..... -0.3V, V_{DD} +0.3V
Analog Inputs to V_{SS} ..... -0.3V, V_{DD} +0.3V
REFOUT Current ..... Indefinite Short to V_{DD} or AGND
Power Dissipation (Any Package) to +75°C 1000mW
Derate Above 75°C by ..... 10mW/°C
Max Junction Temperature
MAX151C, MAX151E ..... 150°C
MAX151M ..... 175°C
Operating Temperature Ranges
MAX151C ..... 0°C to +70°C
MAX151E ..... -40°C to +85°C
MAX151M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature Range (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ACCURACY						
Resolution			10			Bits
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Total Unadjusted Error	TUE	MAX151A MAX151B			±1 ±1.5	LSB
Power-Supply Rejection		V_{DD} = ±5% V_{SS} fixed V_{SS} = ±5% V_{DD} fixed			±1/4 ±1/4	LSB
DYNAMIC PERFORMANCE (f_s = 300kHz, V_{IN} = $5V_{P-P}$ at 40kHz)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)		55	58		dB
Total Harmonic Distortion	THD	First 5 harmonics		-70	-60	dB
Peak Harmonic or Spurious Noise				-70	-60	dB
Full-Power Input Bandwidth	FPBW			5		MHz
ANALOG INPUT						
Analog Input Range			VREF-		VREF+	V
Input Resistance	RIN			10		MΩ
Input Capacitance	CAIN	In series with 150Ω		150		pF
Input Current	IAIN	AIN = 0V to V_{DD}			±10	μA
REFERENCE INPUT						
Ladder Resistance		VREF+ to VREF-	0.5	1		kΩ
Negative Reference Voltage			V_{AGND}-0.1		V_{AGND}+0.1	V
Reference Voltage (Note 2)		VREF+ to VREF-	1		V_{DD}	V
INTERNAL REFERENCE						
Output Voltage		T_A = 25°C	3.970	4.000	4.030	V
Temperature Coefficient (Note 3)					60	ppm/°C
External Load Current		Must not change during conversion (In addition to ladder current)			2	mA
Power-Suppy Rejection		V_{DD} = ±5% V_{SS} fixed V_{SS} = ±5% V_{DD} fixed			±3 ±2	mV
Output Impedance				0.4	1.5	Ω

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$	2.4			V
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$			0.8	V
Input Current	IIN	$\overline{CS}$, $\overline{RD}$; V_{IN} = 0V to V_{DD}			±10	µA
Input Capacitance (Note 1)	CIN	$\overline{CS}$, $\overline{RD}$			10	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB9 I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB9 I_{SRC} = 200µA	4.0			V
Floating State Current	ILKG	DB0-DB9 VOUT = 0V to V_{DD}			±10	µA
Floating Capacitance (Note 1)	COUT				15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		4.75		5.25	V
Negative Supply Voltage	V_{SS}		-4.75		-5.25	V
Positive Supply Current	IV_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		30	45	mA
Negative Supply Current	IV_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		25	40	mA
Power Dissipation	PD	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V, Including Ladder; REFOUT connected to VREF+		275	425	mW

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V; Guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0		ns
Data Access Time (Notes 4, 5)	t_{RD}	C_L = 100pF		70	**120**		**180**	ns
Bus Relinquish Time (Notes 4, 5)	t_{DH}				**70**		**100**	ns
Conversion Time (Note 4)	t_{CONV}			1.9	**2.5**		**2.5**	µs
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 4)	t_{BUSY}	C_L = 100pF		70	**140**		**200**	ns
Data Setup Time After $\overline{BUSY}$ (Notes 4, 5)	t_B				**30**		**50**	ns
Delay Between Conversions	t_D	With $R_S < 50\Omega$	500			500		ns
		With $R_S < 1k\Omega$	1.5			1.5		µs
$\overline{RD}$ Pulse Width	t_{RPW}	To minimize digital coupling in ROM Mode			300		300	ns
Aperture Delay	t_{AP}			30				ns
Aperture Jitter				100				ps

Note 1: Guaranteed by design, not 100% tested.
Note 2: Reduce accuracy at low reference voltages. See Typical Operating Characteristics.
Note 3: VREF Tempco = ΔVREF/ΔT, where ΔVREF is the change in the reference voltage from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: 100% production tested.
Note 5: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. t_{RD} and t_B are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. t_{DH} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{SS} = -5V; VREF- = 0V, VREF+ = +5V; Slow Memory Mode; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$	2.4			V
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$			0.8	V
Input Current	IIN	$\overline{CS}$, $\overline{RD}$; V_{IN} = 0V to V_{DD}			±10	µA
Input Capacitance (Note 1)	CIN	$\overline{CS}$, $\overline{RD}$			10	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB9 I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB9 I_{SRC} = 200µA	4.0			V
Floating State Current	ILKG	DB0-DB9 VOUT = 0V to V_{DD}			±10	µA
Floating Capacitance (Note 1)	COUT				15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		4.75		5.25	V
Negative Supply Voltage	V_{SS}		-4.75		-5.25	V
Positive Supply Current	IV_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		30	45	mA
Negative Supply Current	IV_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V REFOUT connected to VREF+		25	40	mA
Power Dissipation	PD	$\overline{CS}$ = $\overline{RD}$ = 0, AIN = 0V, Including Ladder; REFOUT connected to VREF+		275	425	mW

TIMING CHARACTERISTICS

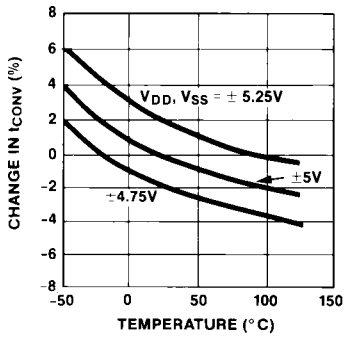
(V_{DD} = +5V, V_{SS} = -5V; Guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0		ns
Data Access Time (Notes 4, 5)	t_{RD}	C_L = 100pF		70	**120**		**180**	ns
Bus Relinquish Time (Notes 4, 5)	t_{DH}				**70**		**100**	ns
Conversion Time (Note 4)	t_{CONV}			1.9	**2.5**		**2.5**	µs
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 4)	t_{BUSY}	C_L = 100pF		70	**140**		**200**	ns
Data Setup Time After $\overline{BUSY}$ (Notes 4, 5)	t_B				**30**		**50**	ns
Delay Between Conversions	t_D	With $R_S < 50\Omega$	500			500		ns
		With $R_S < 1k\Omega$	1.5			1.5		µs
$\overline{RD}$ Pulse Width	t_{RPW}	To minimize digital coupling in ROM Mode			300		300	ns
Aperture Delay	t_{AP}			30				ns
Aperture Jitter				100				ps

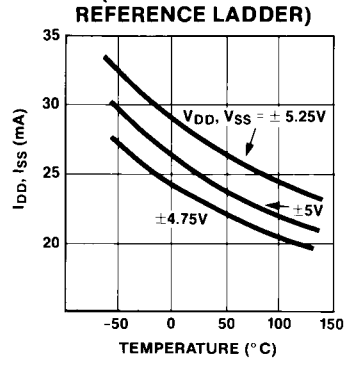
Note 1: Guaranteed by design, not 100% tested.
Note 2: Reduce accuracy at low reference voltages. See Typical Operating Characteristics.
Note 3: VREF Tempco = ΔVREF/ΔT, where ΔVREF is the change in the reference voltage from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: 100% production tested.
Note 5: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. t_{RD} and t_B are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. t_{DH} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Typical Operating Characteristics

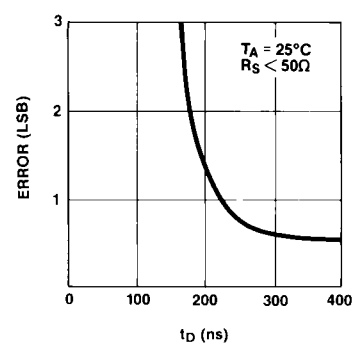
CONVERSION TIME vs. TEMPERATURE



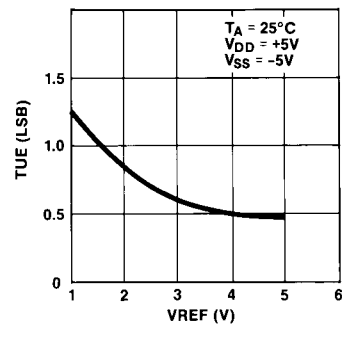
POWER-SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



ACCURACY vs. t_D



ACCURACY vs. VREF (VREF = VREF+ - VREF-)



Pin Description

PIN	NAME	FUNCTION
1	TP	Test Pin, leave open.
2	VREF+	Positive Ladder Input, upper limit of reference span. Set the full-scale input voltage. Range: 1V to V_{DD}.
3	AIN	(Sampling) Analog Input
4	REFOUT	+4V Reference Output, usually connected to VREF+.
5-6	DBX	(Reserved for DB0-1, future 12-bit version, = LOW.)
7-10	DB0-DB3	Three-State Data Output, Bits 0-3
11	$\overline{BUSY}$	$\overline{Busy}$ Status Output, low when conversion is in progress.
12	DGND	Digital Ground.
13	V_{SS}	Negative Supply, -5V.
14	$\overline{CS}$	$\overline{Chip\ Select}$ Input, must be low for the ADC to recognize $\overline{RD}$.
15	$\overline{RD}$	Active Low $\overline{Read}$ Input, starts conversion when $\overline{CS}$ is low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
16-21	DB4-DB9	Three-State Data Output, Bits 4-9
22	V_{DD}	Positive Supply, +5V
23	AGND	Analog Ground
24	VREF-	Negative Voltage Ladder Input, lower limit of reference span. Set the zero-code voltage. Range: AGND ±0.1V.

Detailed Description

ADC Operation

The MAX151 half-flash A/D converter contains 31 comparators. The analog input is sampled by each comparator and compared to a resistive ladder DAC. A 5-bit coarse conversion result is then generated from the ladder DAC, subtracted from the analog input, and compared to a 2nd resistive ladder. 5 coarse and 5 fine bits are output in 10-bit wide parallel output format.

The voltage at the top and the bottom of the reference ladder determines the MAX151's zero-scale and full-scale input voltage. The analog input can range from 0V to +5V. An internal reference provides a 4.000V nominal output and is used by connecting REFOUT to VREF+ and VREF- to AGND. The reference provides up to 2mA of external load current in addition to the current it supplies to the internal ladder. Figure 3 shows the MAX151 in a typical application.

Analog Input - T/H

The MAX151 input can be modeled as a 150pF load in series with 150Ω (Figure 4). The comparator's input capacitance acts as a "hold" capacitor and must be completely charged by the input signal with every A/D conversion.

The input signal sees AIN as a capacitor which is switched between itself and AGND. Between conversions, the signal is tracked by connecting the capacitor to AIN. When a conversion begins, the capacitor disconnects from the analog input, and the A/D performs its conversion. At the end of the conversion, it reconnects to the input and charges to the input signal.

The MAX151 can digitize a variety of high-speed input signals without an external sample-and-hold. Although the conversion time for the MAX151 is 1.9μs, the time the input must be stable is much less.

The time needed for the T/H to acquire an input signal is a function of how quickly the input capacitance can be charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + 150\Omega)150pF$$
(but never less than 500ns)

Where R_S = source impedance of the input signal.

The MAX151 samples the analog input approximately 30ns after $\overline{RD}$ and $\overline{CS}$ (which are internally NANDed) are pulled low. This aperture delay is caused by the propagation delay of the internal logic. The variation in this delay from one conversion to the next is called aperture jitter, and it is typically less than 100ps.

The architecture of the MAX151 allows signals with high slew rates to be converted without error (Figure 4). The errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without sample-and-hold: a 1μs SAR converter would be unable to measure a 1kHz, 5V sine wave without using an external sample-and-hold. With no external sample-and-hold, the MAX151 can typically measure $5V_{p-p}$, 100kHz waveforms.

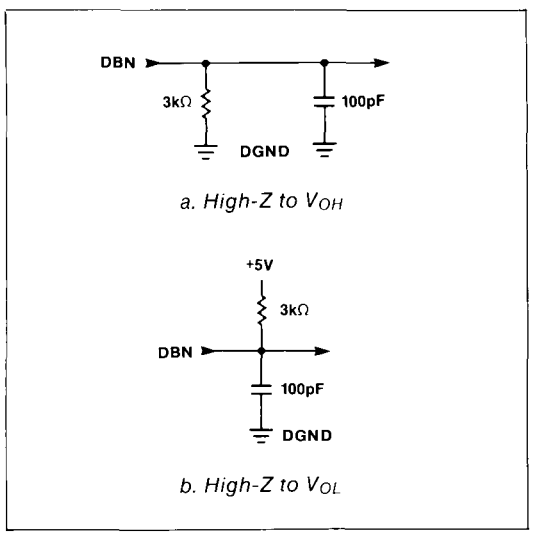


Figure 1. Load Circuits for Data Access Time Test

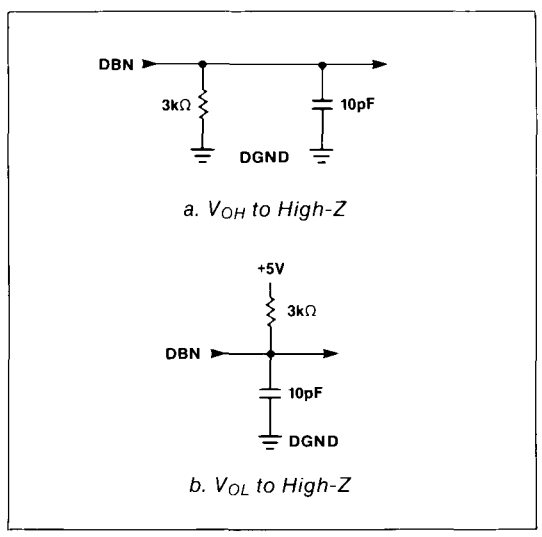


Figure 2. Load Circuits for Bus Relinquish Time Test

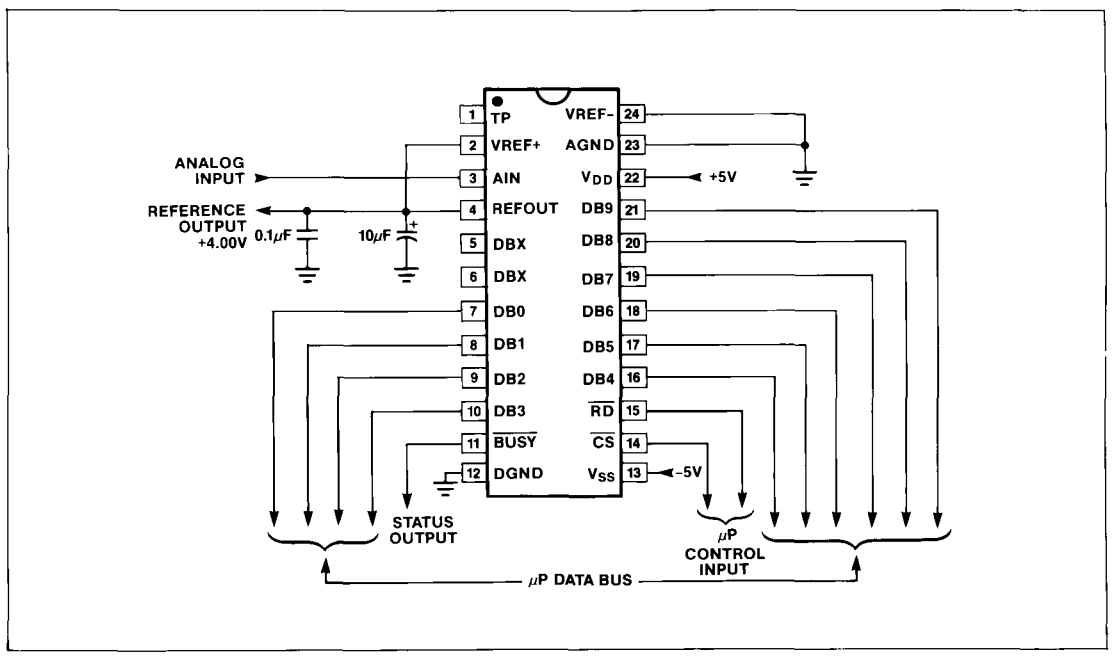


Figure 3. MAX151 Operational Diagram

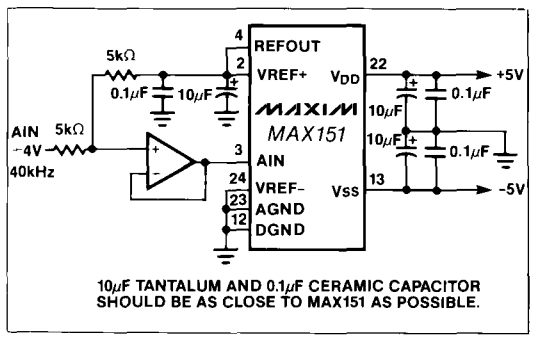


Figure 4. ±4V Bipolar Input with Driving Amplifier

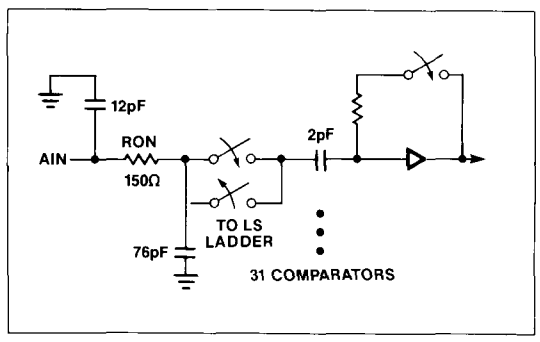


Figure 5. Equivalent Input Circuit

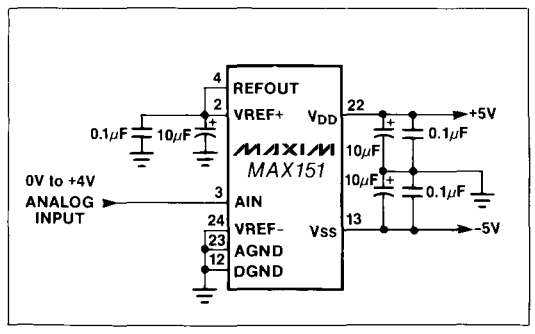


Figure 6. Internal Reference

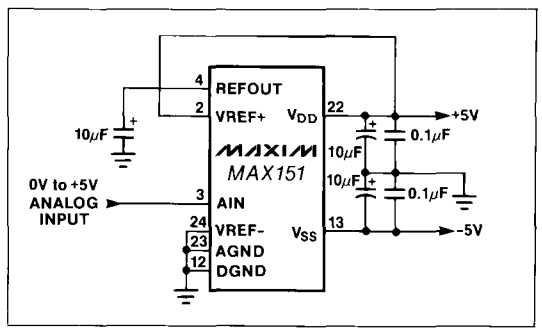


Figure 7. Power Supply as Reference

Input Drive Requirements

To fully utilize the speed advantages of the MAX151, the input should be driven by a fast settling op amp. The OP-42 and AD711 are 10-bit accurate op amps which can drive the MAX151. Both settle to 0.01% in less than 1μs.

On the other hand, since the acquisition time can be user controlled by adding delay between conversions, a slow amplifier or no amplifier can be used. For example, with a 1kΩ driving impedance, waiting 1.5μs between conversions ensures 10-bit accuracy. The MAX400 amplifier works well as an input buffer at these reduced conversion rates.

The analog input can be easily offset by the driving amplifier to obtain a ±4V bipolar input range for DSP applications (Figure 4).

Input Current

The MAX151 input behaves somewhat differently from conventional ADCs. Data-sampling comparators take varying amounts of current from the input. Figure 5 shows the equivalent input circuit. When the conversion starts, AIN is disconnected from the analog input signal. When $\overline{BUSY}$ goes high at the end of a conversion, AIN is connected to 31 2pF capacitors. During this tracking phase ($\overline{BUSY}$ = High), the input capacitors must be charged to the input voltage through the resistance of the internal analog switches (typically 150Ω). In addition, about 90pF of stray capacitance must be charged.

Internal Reference

The MAX151 has a +4.00V buried zener reference. The reference output is available at REFOUT and must be bypassed to AGND with a 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor. The capacitors minimize noise by providing a low impedance path to ground for high-frequency signals. These capacitors should be connected even if the internal reference is not used. A resistor must NOT be connected between the bypass capacitors and REFOUT. In addition to the current it supplies to the ladder, the internal reference output buffer can source up to 2mA for external circuitry.

To use the on-chip reference, connect REFOUT to VREF+ and VREF- to ground. The 4.00V output is referenced to AGND. For the majority of 10-bit measurement applications, use the internal reference. If desired, an external reference can be used as an alternative (Figures 6-8).

300kHz 10-Bit A/D Converter with Reference and T/H

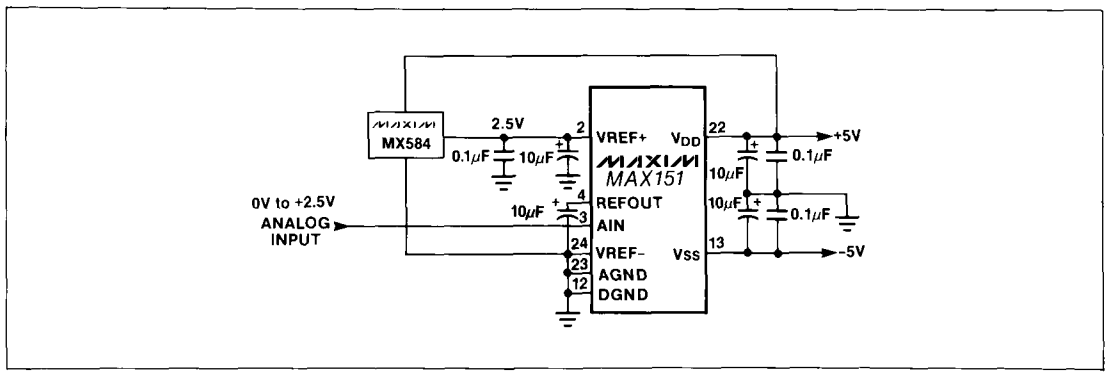


Figure 8. External Reference 2.5V Full-Scale

The VREF+ and VREF- inputs set the full-scale and zero-input voltages of the A/D. More precisely, the voltage at VREF- defines the input which produces an output code of all 0s, and the voltage at VREF+ defines the input which produces an output code of all 1s (Figure 9).

Gain and Offset Adjustment

Figure 9 shows the nominal unipolar transfer function of the MAX151. Code transitions occur at successive integer Least Significant Bit (LSB) values. Output coding is natural binary with 1LSB = 3.91mV (4V/1024) for a 4V reference.

End-point errors are very low. But, if the end points (offset and full scale) need to be adjusted to compensate for errors from other components in the system, use the following techniques. In applications where full-scale adjustment is required, the connection in Figure 10 provides ±0.5%, or ±5 LSBs of adjustment range. If both offset and full-scale range need adjustment, the circuit in Figure 11 is recommended. Offset should be adjusted before full-scale. For the MAX151 (0V to +4V input range), apply 1/2 LSB (2mV) to the analog input and adjust R12 so the digital output code changes between 00000 00000 and 00000 00001. To adjust full-scale, apply FS-3/2LSB (3.994mV) and adjust R8 until the output code changes between 11111 11110 and 11111 11111. There may be slight interaction between adjustments. If an input gain of 2 is acceptable, the connection in Figure 11 can be simplified by removing R5 and R6.

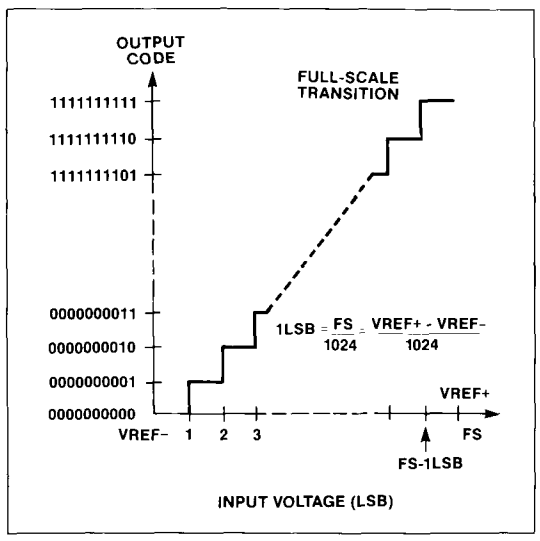


Figure 9. Ideal Transfer Function

Starting a Conversion

The ADC is controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. The T/H holds the value of the input signal, and a conversion is triggered by the falling edge of $\overline{CS}$ and $\overline{RD}$. The $\overline{BUSY}$ output goes low as soon as the conversion starts. $\overline{BUSY}$ goes high at the end of the conversion, and the result is latched into three-state output buffers.

Digital Interface

The MAX151 has two basic interface modes: The Slow Memory Mode requires handshaking, but the ROM Mode does not. The length of the $\overline{RD}$ pulse tells the chip which mode is anticipated. In both modes, conversions are initiated by a falling $\overline{RD}$ and $\overline{CS}$ signal.

In the Slow Memory Mode, the μP actively holds $\overline{RD}$ low until a complete conversion has been performed. During the conversion, the data outputs are active with the data from the previous conversion. After the conversion ends (t_{CONV}), the μP can read the result of the conversion. The $\overline{BUSY}$ signal is used as a handshake to tell the μP when a conversion ends.

In the ROM Mode, a short $\overline{RD}$ pulse starts a conversion and reads the result of the previous conversion. Note, the width of this pulse should not exceed 300ns.

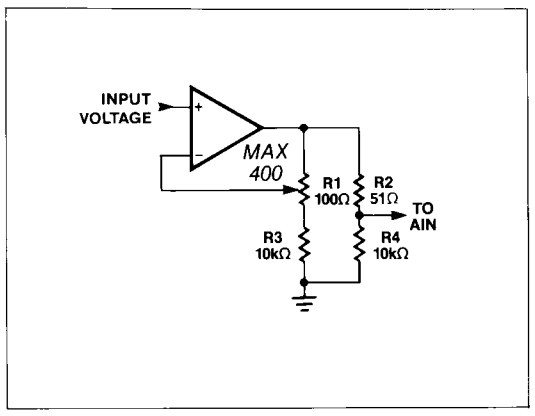


Figure 10. Trim Circuit for Full-Scale Only (±0.5%)

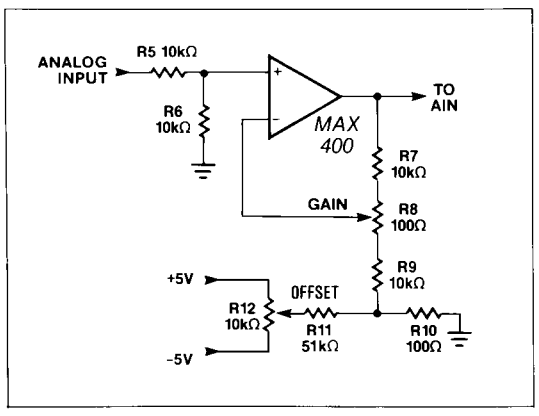


Figure 11. Offset (±20mV) and Gain (±0.5%) Trim Circuit

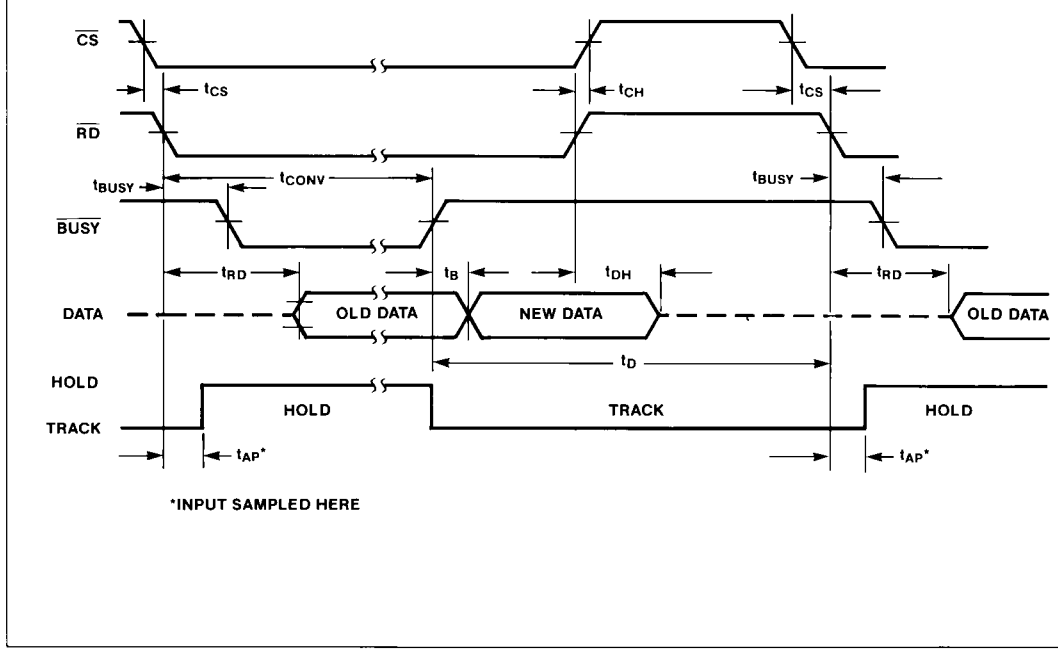


Figure 12. Timing Diagram—Slow Memory Mode

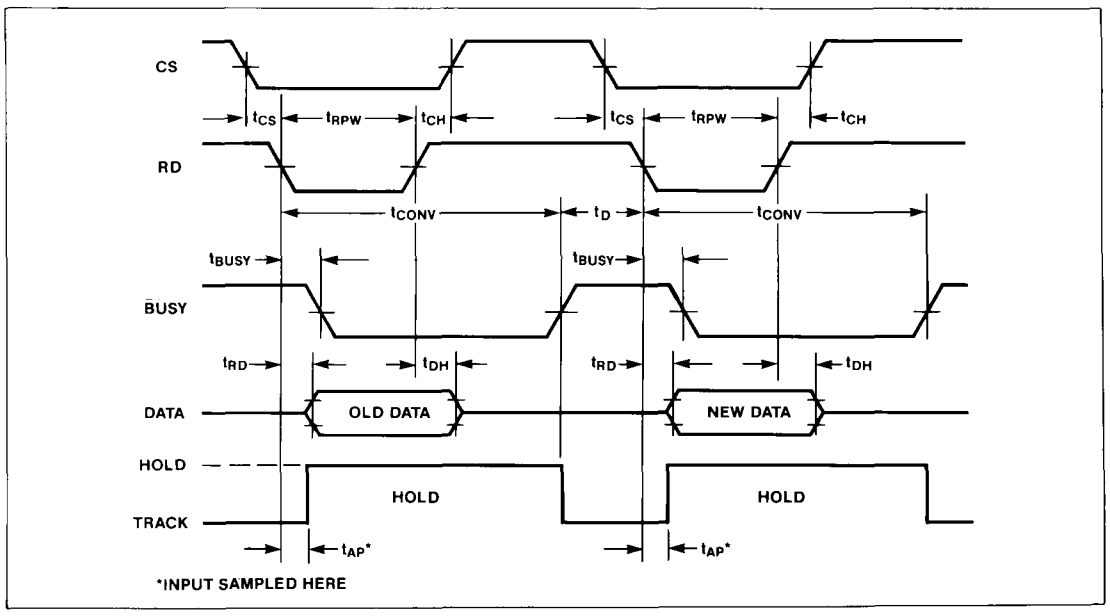


Figure 13. Timing Diagram—ROM Mode

Layout, Grounding and Bypassing

For best system performance, printed circuit boards should be used (wire-wrap boards are not recommended). In layout, separate the digital and analog signal lines as much as possible. Analog and digital lines should not run parallel, and digital lines should not run underneath the ADC package.

Figure 14 shows the recommended power-supply grounding connections. A single-point analog STAR ground should be established at AGND separate from the logic ground. All other analog grounds and DGND should be connected to this STAR ground. No other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

Power supplies should be bypassed to the analog STAR ground with 0.1μF and 10μF bypass capacitors. Capacitor leads should have minimum length for best noise rejection.

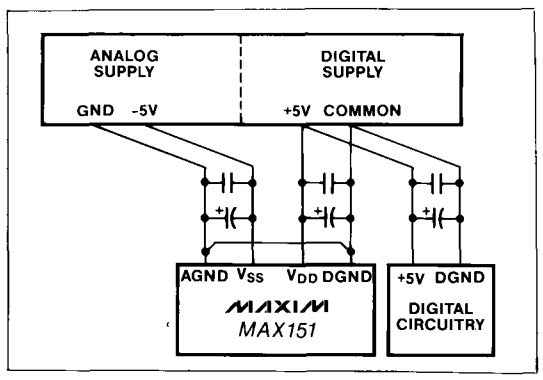


Figure 14. Power-Supply Grounding Practice

Dynamic Performance

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are accepted for specifying performance with DC and slowly varying signals, but less useful in signal processing where the A/D's impact on the system transfer is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

High-speed sampling capability and up to 333 ksamples/sec throughput make the MAX151 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the A/D's dynamic frequency response, distortion and noise at the rated throughput. This involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm to determine spectral content. Conversion errors are seen as spectral elements outside of the fundamental input frequency.

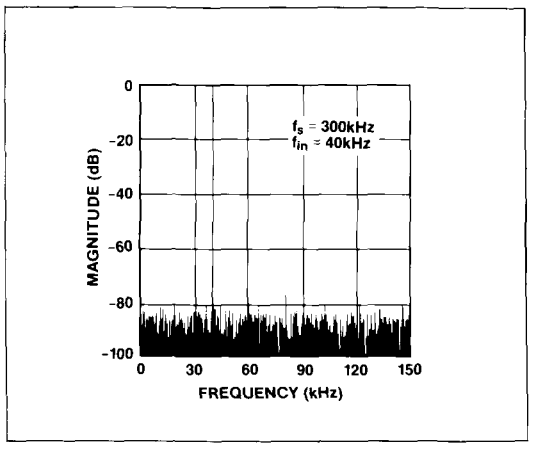


Figure 15. FFT Plot for the MAX151

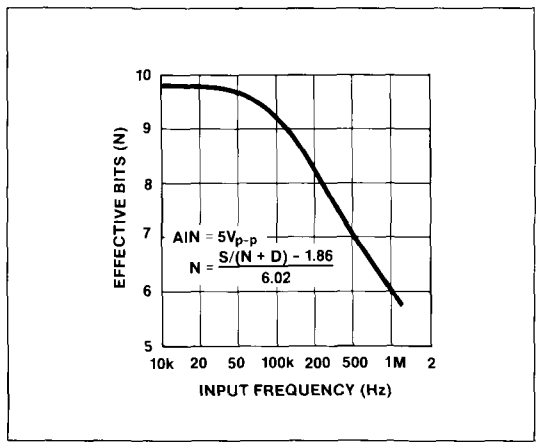


Figure 16. Effective Bits Curve

Signal-to-Noise Ratio and Effective Number of Bits

The ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). This includes distortion and noise components. For this reason, the ratio is also referred to as S/(N + D), or Signal-to-Noise plus Distortion.

The theoretical minimum A/D noise is caused by quantization error and a direct result of the A/D's resolution:

$$SNR = (6.02N + 1.76)dB$$

where N is the number of bits of resolution. A perfect 10-bit A/D can do no better than 62dB. Figure 15 shows the result of sampling a pure 40kHz sinusoid at a 300kHz rate. The FFT plot of the output shows the output level in various spectral bands (Figure 15).

By transposing the equation which converts resolution to SNR, the effective resolution or the "Effective Number of Bits" the A/D provides can be determined from the *measured* SNR:

$$N = (SNR-1.76)/6.02$$

Figure 16 shows the Effective Number of Bits as a function of the input frequency for the MAX151.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20Log[\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... + V_N^2)}/V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through nth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the RMS amplitude of the fundamental input frequency to the amplitude of the next largest spectral component is referred to as the Peak Harmonic or Spurious Noise. Usually this peak occurs at some harmonic of the input frequency. But, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Ordering Information (continued)

PART	TEMP.RANGE	PIN-PACKAGE	TUE (LSB)
MAX151AENG	-40°C to +85°C	24 Plastic DIP	1.0
MAX151BENG	-40°C to +85°C	24 Plastic DIP	1.5
MAX151AEWG	-40°C to +85°C	24 Wide SO	1.0
MAX151BEWG	-40°C to +85°C	24 Wide SO	1.5
MAX151AMRG	-55°C to +125°C	24 CERDIP	1.0
MAX151BMRG	-55°C to +125°C	24 CERDIP	1.5

300kHz 10-Bit A/D Converter with Reference and T/H

Chip Topography