ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/95

MAXIM

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

MAX1601

General Description

The MAX1601 DC power-switching IC contains a network of low-resistance MOSFET switches that deliver selectable VCC and VPP voltages to two Cardbus or PCMCIA host sockets. Key features include very low-resistance switches, small packaging, soft-switching action, and compliance with PCMCIA specifications for 3V/5V switching. 3.3V-only power switching for fast, 32-bit Cardbus applications is supported in two ways: stiff, low-resistance 3.3V switches allow high 3.3V load currents (up to 1A); and completely independent internal charge pumps let the 3.3V switch operate normally, even if the 5V and 12V supplies are disconnected or turned off in order to conserve power. The internal charge pumps are regulating types that draw reduced input current when the VCC switches are static. Also, power consumption is automatically reduced to 10µA when the switches are programmed to high-Z or GND states over the serial interface, unlike other solutions that may require a separate shutdown control input.

Other key features include guaranteed specifications for output current limiting level, and guaranteed specifications for output rise/fall times (in compliance with PCMCIA specifications). Reliability is enhanced by thermal overload protection, accurate current limiting, overcurrent fault flag output, undervoltage lockout, and extra ESD protection at the VCC/VPP outputs. The SMBus serial interface is flexible, and can tolerate logic input levels in excess of the positive supply rail.

The MAX1601 fits two complete Cardbus/PCMCIA switches into a space-saving, narrow (0.2", 5mm wide) shrink small-outline package.

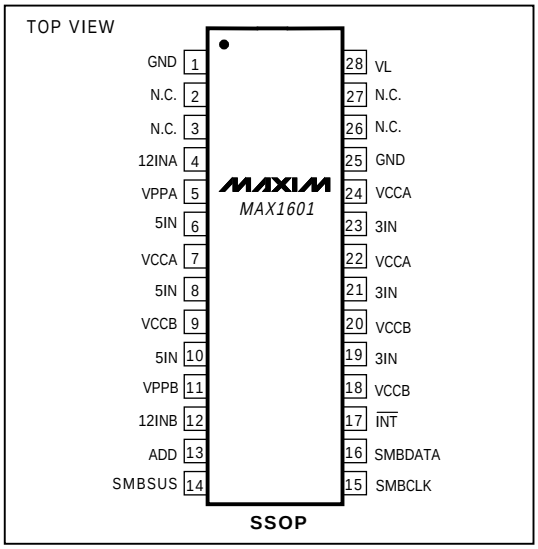
Features

- ♦ **Supports Two PCMCIA/Cardbus Sockets**
- ♦ **1A, 0.08Ω Max 3.3V VCC Switch**
  1A, 0.14Ω Max 5V VCC Switch
- ♦ **Soft Switching for Low Inrush Surge Current**
- ♦ **Overcurrent Protection**
- ♦ **Overcurrent/Thermal Fault Flag Output**
- ♦ **Thermal Shutdown at T_J = 150°C**
- ♦ **Independent Internal Charge Pumps**
- ♦ **Break-Before-Make Switching Action**
- ♦ **10µA Max Standby Supply Current**
- ♦ **5V and 12V Not Required for Low-$R_{DS(ON)}$ 3.3V Switching**
- ♦ **Complies with PCMCIA 3V/5V Switching Specifications**
- ♦ **Super-Small 28-Pin SSOP Package (0.2" or 5mm wide)**
- ♦ **System Management Bus (SMBus) Serial Interface**

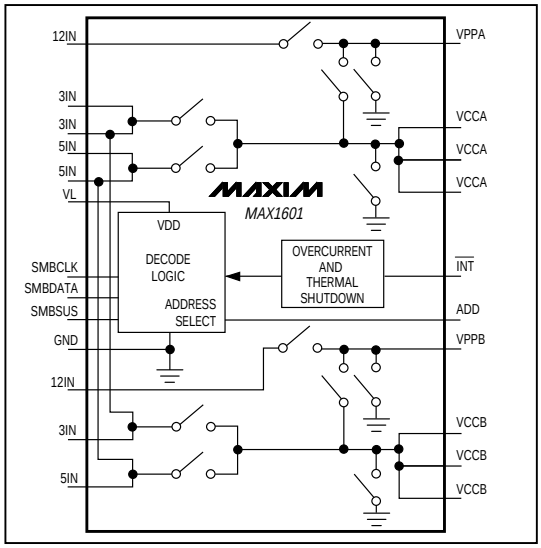
Applications

Desktop Computers	Data Loggers
Notebook Computers	Digital Cameras
Docking Stations	Printers
Handy-Terminals	PCMCIA Read/Write Drives

Pin Configuration



Simplified Block Diagram



SMBus is a trademark of Intel Corp.

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface

ABSOLUTE MAXIMUM RATINGS

Inputs/Outputs to GND
(VL, 3IN, 5IN, VCCA, VCCB) (Note 1) .....-0.3V, +6V
VPP Inputs/Outputs to GND
(12INA, 12INB, VPPA, VPPB) (Note 1) .....-0.3V, +15V
Inputs and Outputs to GND (SMBCLK, SMBDATA, SMBSUS, $\overline{INT}$) (Note 1) .....-0.3V, +6V
ADD Input to GND .....-0.3V, (VL + 0.3V)
VCCA, VCCB Output Current (Note 2).....2A
VPPA, VPPB Output Current (Note 2) 250mA
VCCA, VCCB Short Circuit to GND.....Continuous
VPPA, VPPB Short Circuit to GND.....Continuous
ESD Protection (VCC/VPP outputs) .....4000V Minimum
ESD Protection (other pins) .....2000V Minimum
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX1600CAI .....0°C to +70°C
MAX1600EAI.....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: There are no parasitic diodes between any of these pins, so there are no power-up sequencing restrictions (for example, logic input signals can be applied even if all of the supply voltage inputs are grounded).
Note 2: VCC and VPP outputs are internally current-limited to safe values. See the *Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-SUPPLY SECTION						
Input Voltage Range	3IN, 5IN or VL		3		5.5	V
	12INA, 12INB		11		13	
Undervoltage Lockout Threshold	Falling edge, hysteresis = 1%, 3IN or 5IN			2.5	2.8	V
Standby Supply Current	3IN or 5IN, all switches 0V or high-Z, control inputs = 0V or VL	T_A = +25°C		1	10	µA
		T_A = T_{MIN} to T_{MAX}		1	20	
3IN Quiescent Supply Current	Any combination of 3IN switches on, control inputs = 0V or VL, no VCC loads			30	200	µA
5IN Quiescent Supply Current	Any combination of 5IN switches on, control inputs = 0V or high-Z, no VCC loads			35	200	µA
12IN_ Standby Supply Current	12INA tied to 12INB, all switches 0V or high-Z, control inputs = 0V or VL	T_A = +25°C		1	10	µA
		T_A = T_{MIN} to T_{MAX}			20	
12IN_ Quiescent Supply Current	12INA tied to 12INB, VPPA and VPPB 12V switches on, control inputs = 0V or VL, no VPP loads			15	100	µA
VL Standby Supply Current	All switches 0V or high-Z, control inputs = 0V or VL			3.8	10	µA
VL Quiescent Supply Current	Any combination of switches on			25	300	µA
VL Fall Rate	When using VL as shutdown pin		0.25			V/sec
VCC SWITCHES						
Operating Output Current Range	VCCA or VCCB, 3IN = 5IN = 3V to 5.5V		0		1	A
On-Resistance, 3V Switches	3IN = VL = 3V, I_{SWITCH} = 1A, T_A = +25°C			0.06	0.08	Ω
On-Resistance, 5V Switches	5IN = 4.5V, 3IN = 3V to 3.6V, I_{SWITCH} = 1A, T_A = +25°C			0.10	0.14	Ω
Output Current Limit	VCCA or VCCB		1.5		3	A
Output Sink Current	VCCA or VCCB < 0.4V, programmed to 0V state		20			mA

ELECTRICAL CHARACTERISTICS (continued)

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Leakage Current	VCCA or VCCB forced to 0V, high-Z state				10	µA
Output Propagation Delay Plus Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, C_L = 30µF, R_L = 25Ω, 50% of input to 90% of output (Note 3)				10	ms
Output Rise Time	VCCA or VCCB, 0V to 3IN or 5IN, C_L = 1µF, R_L = open circuit, 10% to 90% points (Note 3)		100			µs
Output Propagation Delay Plus Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, C_L = 30µF, R_L = open circuit, 50% of input to 10% of output (Note 3)				60	ms
Output Fall Time	VCCA or VCCB, 3IN or 5IN to 0V, C_L = 1µF, R_L = 25Ω, 90% to 10% points (Note 3)		3			ms
VPP SWITCHES						
Operating Output Current Range	VPPA or VPPB		0		120	mA
On-Resistance, 12V Switches	12IN = 11.6V, I_{SWITCH} = 100mA, T_A = +25°C			0.65	1	Ω
On-Resistance, VPP = VCC Switches	Programmed to 5IN (5V) or 3IN (3.3V)			1	3	Ω
Output Current Limit	VPPA or VPPB		130	200	260	mA
Output Sink Current	VPPA or VPPB < 0.4V, programmed to 0V state		10			mA
Output Leakage Current	VPPA or VPPB forced to 0V, high-Z state				10	µA
Output Propagation Delay Plus Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 50% of input to 90% of output (Note 3)				30	ms
Output Rise Time	VPPA or VPPB, 0V to 12IN_, C_L = 0.1µF, 10% to 90% points (Note 3)		1			ms
Output Propagation Delay Plus Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 50% of input to 10% of output (Note 3)				60	ms
Output Fall Time	VPPA or VPPB, 12IN_ to 0V, C_L = 0.1µF, 90% to 10% points (Note 3)		1			ms
INTERFACE AND LOGIC SECTION						
$\overline{INT}$ Signal Propagation Delay	VCC_ or VPP_, load step to $\overline{INT}$ output, 50% point to 50% point (Note 4)		0		10	µs
$\overline{INT}$ Output Low Voltage	I_{SINK} = 1mA, low state				0.4	V
$\overline{INT}$ Output Leakage Current	$V_{\overline{INT}}$ = 5.5V, high state		-0.1		0.1	µA
Thermal Shutdown Threshold	Hysteresis = 20°C			150		°C
Logic Input Low Voltage	SMBSUS, SMBCLK, SMBDATA, VL = 3V to 5.5V				0.6	V
Logic Input High Voltage	SMBSUS, SMBCLK, SMBDATA	VL = 3V to 3.6V	1.4			V
		VL = 3V to 5.5V	2.3			V
Logic Output Low Voltage	SMBDATA, I_{SINK} = 4mA				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(VL = 3IN = 3.3V, 5IN = 5V, 12INA = 12INB = 12V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMB Input Capacitance	SMBSUS, SMBCLK, SMBDATA		5		pF
SMBCLK Clock Frequency	SMBus spec = 10kHz min	DC		100	kHz
SMBCLK Clock Low Time	T_{LOW} 10% to 10% points	4.7			µs
SMBCLK Clock High Time	T_{HIGH} 90% to 90% points	4			µs
SMB Rise Time	SMBCLK, SMBDATA 10% to 90%			1	µs
SMB Fall Time	SMBCLK, SMBDATA 90% to 10%			300	ns
SMB Repeated Start-Condition Setup Time	$T_{SU:STA}$ 90% to 90% points	250			ns
SMB Start-Condition Hold Time	$T_{HD:STA}$ 10% of SMBDATA to 90% of SMBCLK	4			µs
SMB Stop-Condition Setup Time	$T_{SU:STO}$ 90% of SMBCLK to 10% of SMBDATA	4			µs
SMB Data Valid to SMBCLK Rising-Edge Time	$T_{SU:DAT}$ 10% or 90% of SMBDATA to 10% of SMBCLK	250			ns
SMB Data Hold Time	$T_{HD:DAT}$ (Note 5)	0			ns
Bus Free Time	T_{BUF} between start and stop conditions	4.7			µs
ADD Input Low Voltage				0.6	V
ADD Input High Voltage		1.5			V
Logic Input Bias Current	ADD, SMBSUS, SMBCLK, SMBDATA	-1		1	µA
SCL Fall to SDA Valid (Master Clocking-In Data)				1000	ns
Start-Condition Setup		4.7			µs

Note 3: VCC/VPP timing specifications are 100% tested.
Note 4: Design target value, not production tested.
Note 5: Note that a transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of the falling edge of SMBCLK.

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2, 3, 26, 27	N.C.	No internal connection
4	12INA	12V Supply Voltage Input, internally connects to channel A VPP switch. Tie to VPPA if not used.
5	VPPA	0V/VCC/12V/High-Z VPP Output (channel A). Bypass to GND with 0.01µF for ESD protection.
6	5IN	5V Supply Voltage Input. Must be connected to other 5IN pins. Input range is 3V to 5.5V.
7, 22, 24	VCCA	0V/3.3V/5V/High-Z VCC Output (channel A). Bypass to GND with 0.01µF for ESD protection.
8, 10	5IN	5V Supply Voltage Input
9, 18, 20	VCCB	0V/3.3V/5V/High-Z VCC Output (channel B). Bypass to GND with 0.01µF for ESD protection.
11	VPPB	0V/VCC/12V/High-Z VPP Output (channel B). Bypass to GND with 0.01µF for ESD protection.
12	12INB	12V Supply Voltage Input, internally connects to channel B VPP switch. Tie to VPPB if not used.
13	ADD	Address Input, sets SMBus address location.
14	SMBSUS	SMBus Suspend-Mode Control Input. The device will execute commands previously stored in the normal-mode register if SMBSUS is high, or will execute commands previously stored in the suspend-mode register if SMBSUS is low.
15	SMBCLK	SMBus Clock Input
16	SMBDATA	SMBus Data Input/Output, open drain
17	$\overline{INT}$	Fault-Detection Interrupt Output. $\overline{INT}$ goes low if either channel VCC or VPP switch is current limiting or if the thermal protection circuit is activated. $\overline{INT}$ is an open-drain output that requires an external pull-up resistor.
19	3IN	3.3V Supply Voltage Input. Must be connected to other 3IN pins. Input range is 3V to 5.5V.
21, 23	3IN	3.3V Supply Voltage Input
25	GND	Test-Mode Input, normally grounded
28	VL	Logic Supply Voltage Input, usually connected to the 3.3V host system supply. Input range is 3V to 5.5V. If VL is disconnected or grounded, the device will enter standby mode. VL can be supplied via the output of a CMOS-logic gate, in order to produce an overriding shutdown. When being used as a shutdown input, VL should have an additional 0.01µF bypass capacitor to GND. If VL is cycled, a power-on reset occurs, which resets all of the SMBus data registers.

SMBus Interface Operation

The SMBus serial interface is a two-wire interface with multi-mastering capability, intended to control low-speed peripheral devices in low-power portable equipment applications. SMBus is similar to I²C™ and AccessBus, but has slightly different logic threshold voltage levels (intended to accommodate future low-voltage systems that might have 2V VCC levels, for example), different fixed addresses, and a suspend-mode register capability. To obtain a complete set of specifications on the SMBus interface, call Intel at (800) 253-3696 and ask for product code SBS5220.

SMBus Addressing

These dual-channel PCMCIA switch devices respond to two of four different addresses, depending on the state of the ADD address pin. Normal writing to the device is done by transmitting one of four addresses, followed by a single data byte, to program the channel selected. Write transmissions to the interrupt pointer address are not supported by these devices. Reading from the device is done by transmitting one of two addresses corresponding to either the A channel address (which will provide data about faults for both A and B channels) or to the interrupt pointer address (discussed later).

The normal start condition consists of a high-to-low transition on SMBDATA while SMBCLK is high. The 7-bit address is followed by a bit that designates a read or write operation; high = read, low = write. If the 7-bit address matches one of the supported function addresses, the IC issues an acknowledge pulse by pulling the SMBDATA line low. If the address is not a valid one, the IC stays off of the bus and ignores any data on the bus until a new start condition is detected. Once the IC receives a valid address that includes a write bit, it expects to receive one additional byte of data. If a stop condition or new start condition is detected before a complete byte of data is clocked in, the IC interprets this as an error and all of the data is rejected and lost.

Table 1. SMBus Addressing

SMB Address	ADD Pin	Write Function	Read Function
0001100	Don't care	N/A	Interrupt Pointer
1010000	Grounded	Channel A	Channel A/B faults
1010001	Grounded	Channel B	Channel A/B faults
1010010	Tied to VL	Channel A	Channel A/B faults
1010011	Tied to VL	Channel B	Channel A/B faults

SMBus Write Operations

If the IC receives a valid address immediately followed by a write bit, the IC becomes a slave receiver. The slave IC generates a first acknowledge after the address and write bit, and a second acknowledge after the command byte. A stop condition following the command (data) byte causes the immediate execution of the command, unless the data included a low SUS/OP bit. If the data included a low SUS/OP bit, the command is stored in the suspend-mode register, and is executed only when the SMBSUS pin is pulled low.

Table 2. Command Format for Channel A Write Operations (address 1010000 or 1010010)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: High = normal, Low = suspend.
6	VCCAON	0	Turns on VCCA when high, pulls VCCA to GND when low.
5	VCCA3/5	0	If VCCA is on, a high forces 3.3V output, and a low forces 5V output.
4	VCCAHIZ	0	Puts VCCA in a high-impedance state when high. Overrides VCCAON.
3	VPPAON	0	Turns on VPPA when high, pulls VPPA to GND when low.
2	VPPAPGM	0	If VPPA is on, a high forces VPPA to 12V, and a low forces VPPA to equal VCCA.
1	VPPAHIZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	MASKFLT	0	Masks fault interrupts from both channel A and channel B when high.

I²C is a trademark of Philips Corp.

Table 3. Command Format for Channel B Write Operations (address 1010001 or 1010011)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	OP/SUS	0	Operate/suspend bit. Selects which latch receives data: High = normal, Low = suspend.
6	VCCBON	0	Turns on VCCB when high, pulls VCCB to GND when low.
5	VCCB3/5	0	If VCCB is on, a high forces 3.3V output, and a low forces 5V output.
4	VCCBHIZ	0	Puts VCCB in a high-impedance state when high. Overrides VCCBON.
3	VPPBON	0	Turns on VPPB when high, pulls VPPB to GND when low.
2	VPPBPGM	0	If VPPA is on, a high forces VPPB to 12V, and a low forces VPPB to equal VCCB.
1	VPPAHIZ	0	Puts VPPA in a high-impedance state when high. Overrides VPPAON.
0 (LSB)	RFU	0	Reserved for future use.

Table 4. Read Format for Interrupt Pointer Address (0001100)

BIT	NAME	POR STATE	FUNCTION
7 (MSB)	ADD7	0	ADD7 to ADD1 provide a return address for any interrupt query. For these devices, the return addresses are: 1010000 = Channel A, ADD = low 1010001 = Channel B, ADD = low 1010010 = Channel A, ADD = high 1010011 = Channel B, ADD = high
6	ADD6	0	
5	ADD5	0	
4	ADD4	0	
3	ADD3	0	
2	ADD2	0	
1	ADD1	0	
0 (LSB)	ADD0	0	

Table 5. Read Format for Power Switch Address (1010000 or 1010010)

BIT	NAME	POR STATE	LATCHED?	FUNCTION
7 (MSB)	CATFAULT	0	Y	Indicates catastrophic (thermal or undervoltage lockout) fault when high.
6	FAULT1	0	Y	Indicates VCCA overcurrent fault when high.
5	FAULT2	0	Y	Indicates VPPA overcurrent fault when high.
4	FAULT3	0	Y	Indicates VCCB overcurrent fault when high.
3	FAULT4	0	Y	Indicates VPPB overcurrent fault when high.
2	SIG/DUAL	0	N	Indicates dual part (single-channel devices would read 1)
1	RFU	0	N	Reserved for future use.
0 (LSB)	RFU	0	N	Reserved for future use.

SMBus Read Operations

If the IC receives a valid address that includes a read bit, the IC becomes a slave transmitter. After receiving the address data, the IC generates an acknowledge during the acknowledge clock pulse and drives the SMBDATA line in sync with SMBCLK. The SMB protocol requires that the master end the read transmission by not acknowledging during the acknowledge bit of SMBCLK. These PCMCIA ICs support the repeated start-condition method for changing data transfer direction; that is, a write transmission followed by a repeated start instead of a stop condition prepares the IC for data reading.

SMBus Interrupts

These PCMCIA power-switch ICs are slave devices only, and never initiate communications except by asserting an interrupt (by pulling $\overline{INT}$ low). Interrupts are generated only for reporting fault conditions, including overcurrent at VCCA, VCCB, VPPA, or VPPB, plus IC thermal overload. If an interrupt occurs, it can be an indication of impending system failure. The host system can react by going into suspend mode or taking other action, and come back later to interrogate the IC via the interrupt pointer to determine status or perform corrective action (such as disabling the appropriate power switch that might be connected to a shorted PC card). The fastest method for turning off the switches in response to a fault condition is to cycle the voltage on VL in order to generate a power-on reset (which clears all of the SMBus registers). Note that the SMBus registers retain their data even if the main VCC supplies are turned off, provided that VL is kept powered.

When a fault occurs, $\overline{INT}$ is immediately asserted and latched low. If the fault is momentary and disappears before the IC is serviced, the data is still latched in the interrupt pointer and $\overline{INT}$ remains asserted. Normally, the master (host system or PCMCIA digital controller) now sends out the interrupt pointer address (0011000) followed by a read bit. $\overline{INT}$ is cleared and the PCMCIA IC responds by putting out its address on the bus. If the fault persists, $\overline{INT}$ is re-asserted, but the data in the fault registers is not re-loaded. The data in the fault latches only reflects the first time $\overline{INT}$ is asserted.

Normally, the master now sends out the appropriate PCMCIA switch address on the bus, followed by a read bit. The data in the fault registers is then clocked out onto the bus (an action which also clears the fault registers). If the fault still persists, the fault bits and $\overline{INT}$ are latched again.

The interrupt pointer address provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. The host can read the interrupt pointer to determine which slave device generated an $\overline{INT}$ interrupt signal. The interrupt pointer address can activate several different slave devices simultaneously, similar to an I^2C general call. Any slave device that generated an interrupt will attempt to identify itself by putting its own address on the bus during the first read byte. If more than one slave attempts to respond, bus arbitration rules apply and the device with the lower address code wins. The losing device won't generate an acknowledge and will continue to hold the $\overline{INT}$ line low until serviced, which implies that the host interrupt input must be level-sensitive.

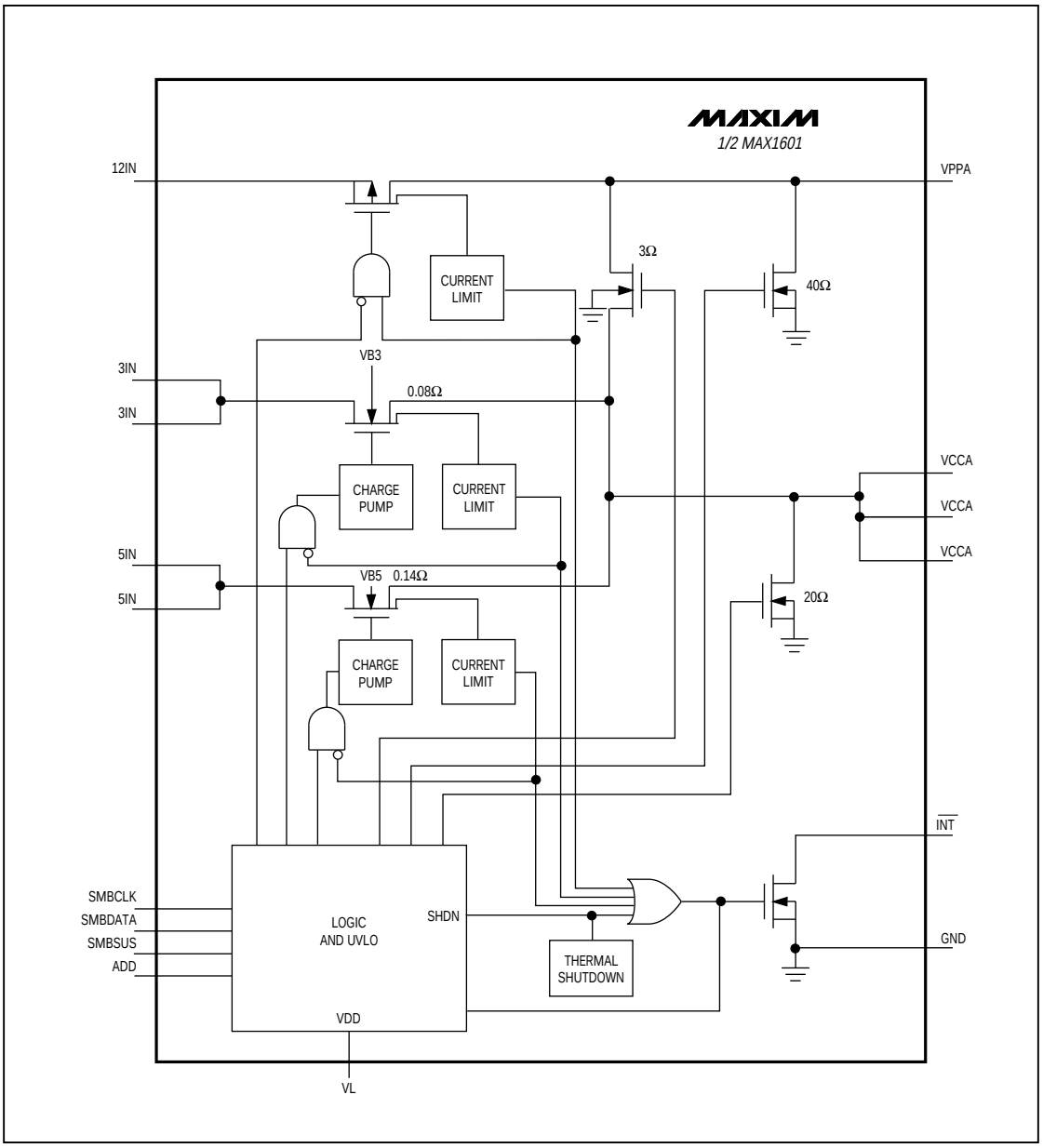


Figure 1. Detailed Block Diagram

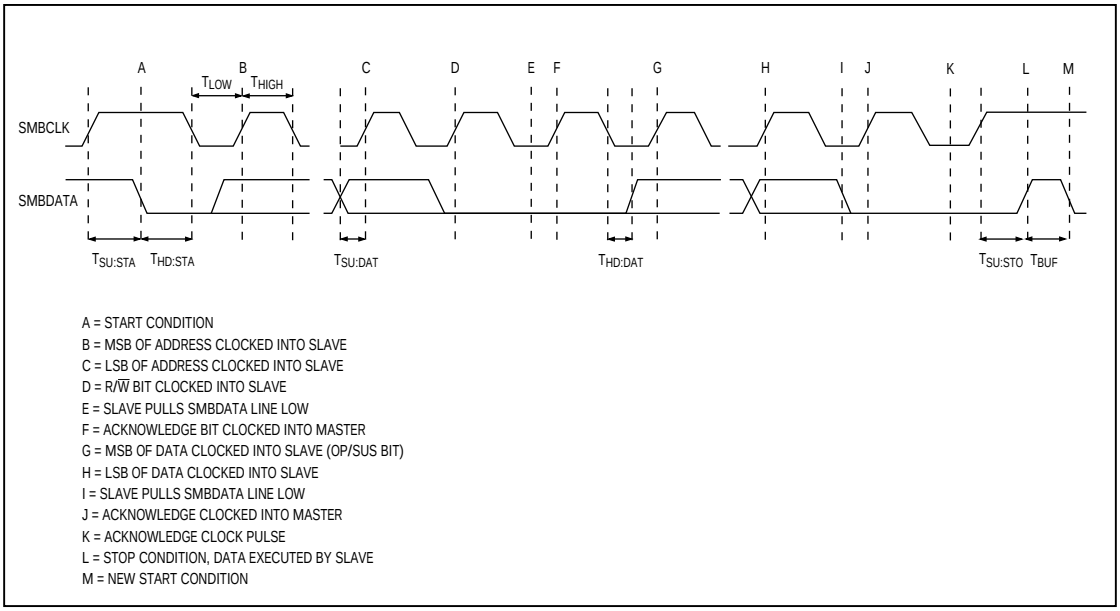


Figure 2. SMBus Write Timing Diagram

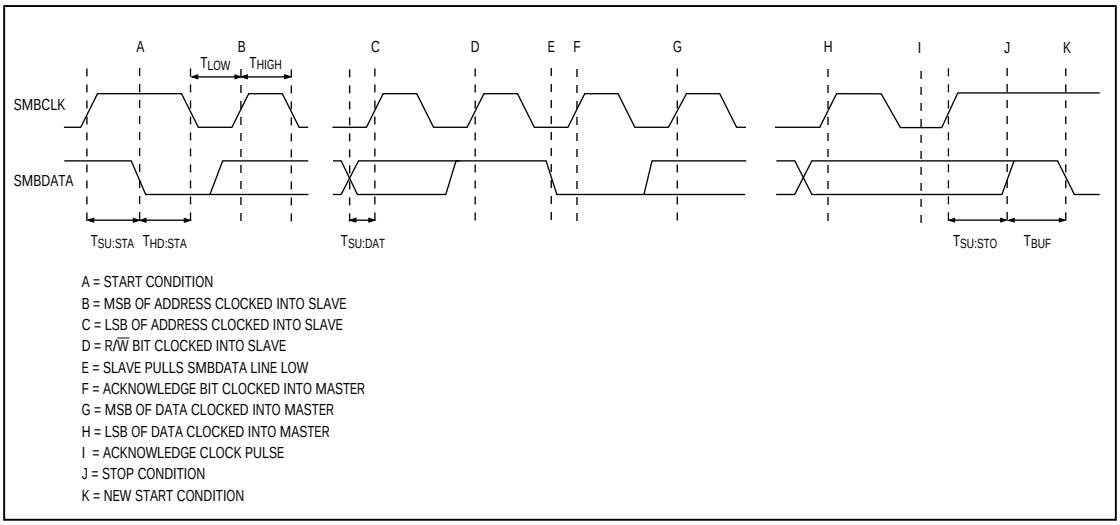


Figure 3. SMBus Read Timing Diagram

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1601CAI	0°C to +70°C	28 SSOP
MAX1601C/D	0°C to +70°C	Dice*
MAX1601EAI	-40°C to +85°C	28 SSOP

** Contact factory for dice specifications.*

Dual-Channel Cardbus and PCMCIA Power Switch with SMBus™ Serial Interface