19-0208; Rev 2; 9/95

MAXIM

Integrated µP Supervisor Module with Lithium Backup Battery

General Description

The MAX1691 reduces the complexity and number of components required for power-supply monitoring and battery control functions in microprocessor (µP) systems. The MAX1691 features switchover to internal backup battery, write protection of CMOS RAM or EEPROM, and a watchdog function.

The internal +3V, 125mAh lithium battery connects to the µP supervisory circuit through external pin strapping, minimizing battery drain during shipping.

The MAX1691 is shipped in special nonconductive material. **Note: Storing the MAX1691 in conductive foam will discharge the internal battery.**

Features

- ♦ **Internal 3V, 125mAh Lithium Battery**
- ♦ **200ms Power OK / Reset Time Delay**
- ♦ **1µA Standby Current, 35µA Operating Current**
- ♦ **On-Board Gating of Chip-Enable Signals, 10ns Max Delay**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **16-Pin, 0.6" Plastic DIP Module**

Applications

Computers

Controllers

Intelligent Instruments

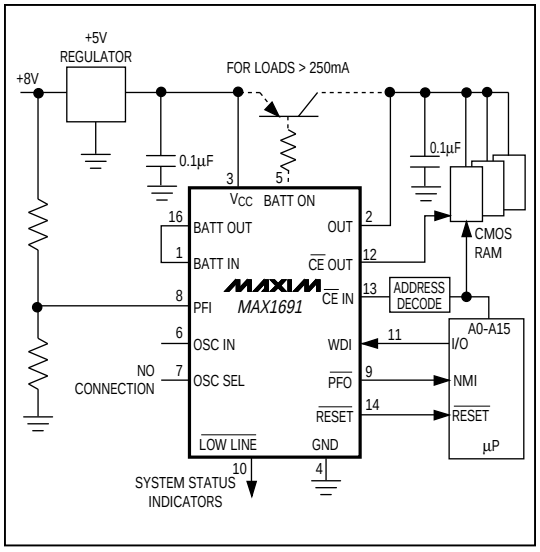
Automotive Systems

Critical µP Power Monitoring

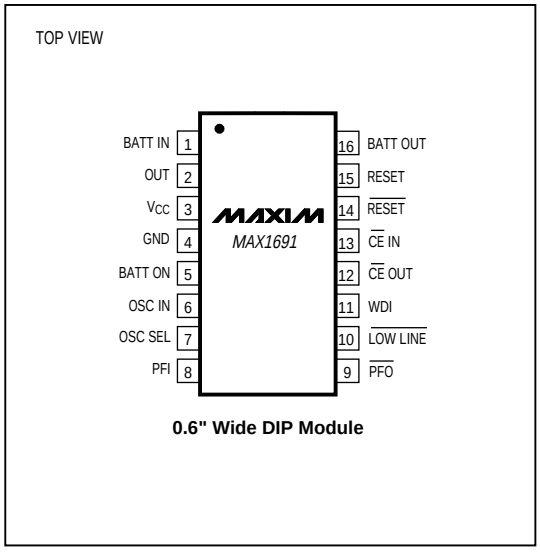
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1691CHE	0°C to +70°C	16 Plastic 0.6" Wide DIP Module

Typical Operating Circuit



Pin Configuration



0.6" Wide DIP Module

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} .....-0.3V to +6V
- All Other Inputs (Note 1) .....-0.3V to (V_{OUT} + 0.3V)

Input Current
- BATT OUT .....0mA to -25mA
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- BATT IN Peak.....250mA
- BATT IN Continuous.....25mA
- GND.....±25mA
- All Other Outputs.....±25mA

Continuous Power Dissipation
- Plastic DIP Module (derate 8.70mW/°C).....696mW

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range.....-40°C to +70°C
Lead Temperature (soldering, 10sec).....+260°C

Note 1: The input voltage limits on PFI and WDI may be exceeded if the current into these pins is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, $V_{BATT\ IN}$ = 2.8V applied externally, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}			0	5.0	5.5	V
Output Voltage, V_{OUT}	V_{CC} = 4.5V	I_{OUT} = 25mA	V_{CC} - 0.05	V_{CC} - 0.02		V
		I_{OUT} = 250mA	V_{CC} - 0.3	V_{CC} - 0.2		
V_{CC} to OUT On-Resistance	V_{CC} = 4.5V			0.8	1.2	Ω
V_{OUT} in Battery-Backup Mode	V_{CC} < V_{BATT}, I_{OUT} = 100µA		$V_{BATT\ IN}$ - 0.25			V
Supply Current in Normal Operating Mode (Excludes I_{OUT})	V_{CC} > $V_{BATT\ IN}$			35	100	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT}) (Note 2)	V_{CC} > $V_{BATT\ IN}$ - 1.2V	T_A = +25°C		0.04	1	µA
		T_A = T_{MIN} to T_{MAX}			5	
$V_{BATT\ IN}$ Standby Current (Note 3)	$V_{BATT\ IN}$ + 0.2V ≤ V_{CC}	T_A = +25°C	-0.1		0.02	µA
		T_A = T_{MIN} to T_{MAX}	-1.0		0.02	
Battery-Switchover Threshold	Power-up		$V_{BATT\ IN}$ + 0.03			V
	Power-down		$V_{BATT\ IN}$ - 0.03			
Battery-Switchover Hysteresis				60		mV
BATT ON Output Low Voltage	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current	Sink current			60		mA
	Source current		1	15	100	µA
Battery Capacity (Note 4)				125		mAh
Internal Battery Voltage (Note 4)				2.9		V
RESET AND WATCHDOG TIMER						
Reset Threshold Voltage			4.50	4.65	4.75	V
Reset Threshold Hysteresis				15		mV
V_{CC} to $\overline{RESET}$ Delay	Power-down			80		µs
$\overline{LOW\ LINE}$ to $\overline{RESET}$ Delay				800		ns
Reset Active Timeout Period, Internal Oscillator	Power-up		140	200	280	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, $V_{BATT\ IN}$ = 2.8V applied externally, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Active Timeout Period, External Clock	Power-up		2048		Clock Cycles
Watchdog Timeout Period, Internal Oscillator	Long period	1.00	1.60	2.25	sec
	Short period	70	100	140	ms
Watchdog Timeout Period, External Clock	Long period		4096		Clock Cycles
	Short period		1024		
Minimum Watchdog Input Pulse Width	V_{IL} = 0.8V, (V_{IH} = 0.75) (V_{CC})	100			ns
$\overline{RESET}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, $V_{BATT\ IN}$ = 0V, V_{CC} falling		0.004	0.300	V
	I_{SINK} = 3.2mA, V_{CC} = 4.25V		0.1	0.4	
	I_{SOURCE} = 1.6mA, V_{CC} = 5V	3.5			
$\overline{RESET}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current		7	20	
RESET Output Voltage Low (Note 5)	I_{SINK} = 3.2mA		0.1	0.4	V
RESET Output Short-Circuit Current (Note 5)	Output sink current		60		mA
$\overline{LOW\ LINE}$ Output Voltage	I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{LOW\ LINE}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	µA
WDI Threshold Voltage (Note 6)	V_{IH}	0.75 x V_{CC}			V
	V_{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		µA
	WDI = V_{OUT}		20	50	
POWER-FAIL COMPARATOR					
PFI Input Threshold	V_{CC} = 5V	1.20	1.25	1.30	V
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{PFO}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	µA
PFI to $\overline{PFO}$ Delay	V_{IN} = -20mV, V_{OD} = 15mV		25		µs
	V_{IN} = 20mV, V_{OD} = 15mV		60		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disabled mode		±0.005	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 7)	Enabled mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disabled mode, $\overline{CE}$ OUT = 0V	0.10	0.75	2.00	mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 8)	50Ω source impedance driver, C_{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V_{CC} = 5V, I_{OUT} = -100µA	3.5			V
	V_{CC} = 0V, $V_{BATT\ IN}$ = 2.8V, I_{OUT} = 1µA	2.7			
$\overline{RESET}$ to $\overline{CE}$ OUT Delay	Power-down		12		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, $V_{BATT\ IN}$ = 2.8V applied externally, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at 25°C.)

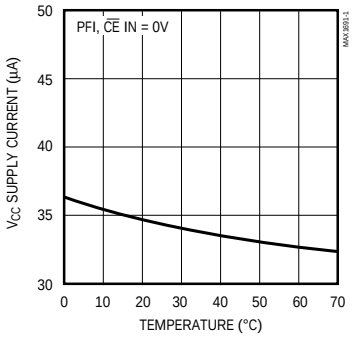
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR					
OSC IN Leakage Current	OSC SEL = 0V		0.10	±5	µA
OSC IN Input Pull-Up Current	OSC SEL = V_{OUT} or floating, OSC IN = 0V		10	100	µA
OSC SEL Input Pull-Up Current	OSC SEL = 0V		10	100	µA
OSC IN Frequency Range	OSC SEL = 0V		50		kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, C_{OSC} = 47pF		100		kHz

Note 2: The supply current drawn from the battery excluding I_{OUT} typically goes to 18µA when ($V_{BATT\ IN}$ - 1V) < V_{CC} < $V_{BATT\ IN}$. In most applications, this is a brief period as V_{CC} falls through this region.
Note 3: "+" = battery-discharging current, "-" = battery-charging current.
Note 4: See *Typical Operating Characteristics.*
Note 5: RESET is an open-drain output and sinks current only.
Note 6: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.
Note 7: The chip-enable resistance is tested with V_{CC} = 4.75V. $V_{\overline{CE}\ IN}$ = $V_{\overline{CE}\ OUT}$ = V_{CC} / 2.
Note 8: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

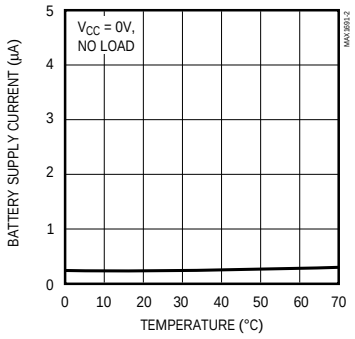
Typical Operating Characteristics

($V_{BATT\ IN}$ = 2.8V externally applied, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

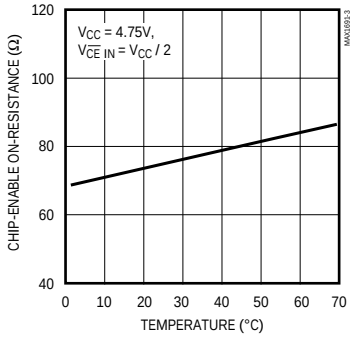
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



BATT IN SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



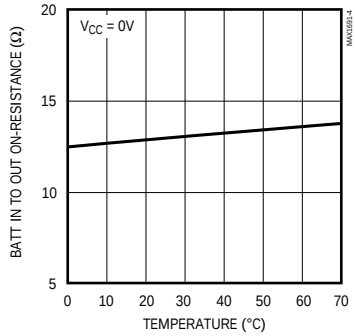
CHIP-ENABLE ON-RESISTANCE vs. TEMPERATURE



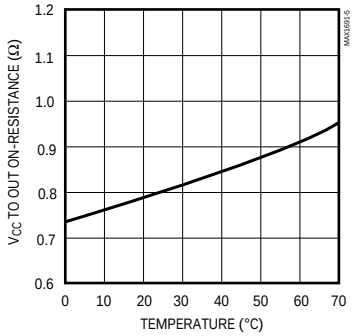
Typical Operating Characteristics (continued)

($V_{BATT\ IN}$ = 2.8V externally applied, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

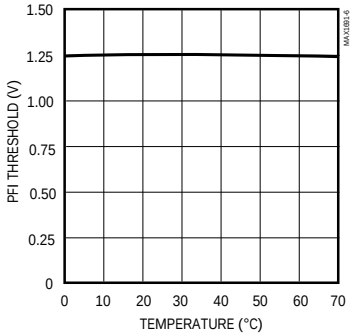
$V_{BATT\ IN}$ TO OUT ON-RESISTANCE vs. TEMPERATURE



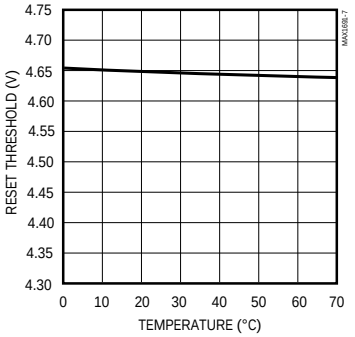
V_{CC} TO OUT ON-RESISTANCE vs. TEMPERATURE



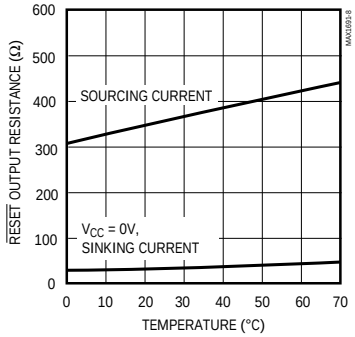
PFI THRESHOLD vs. TEMPERATURE



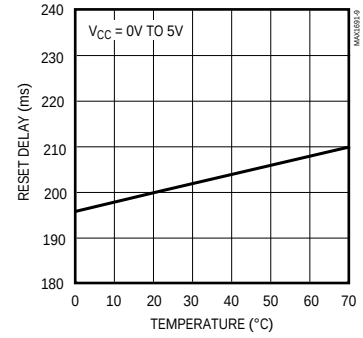
RESET THRESHOLD vs. TEMPERATURE



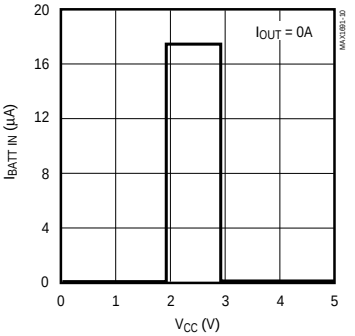
$\overline{RESET}$ OUTPUT RESISTANCE vs. TEMPERATURE



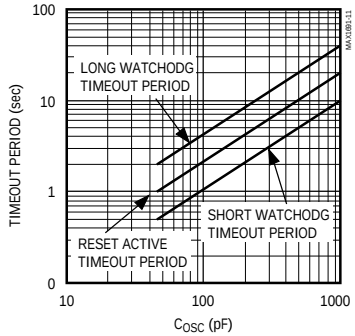
RESET DELAY vs. TEMPERATURE



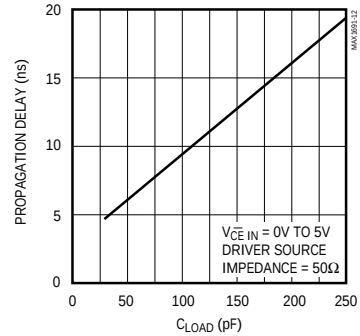
BATT IN CURRENT vs. INPUT SUPPLY VOLTAGE



WATCHDOG AND RESET TIMEOUT PERIOD vs. OSC IN TIMING CAPACITOR (C_{OSC})



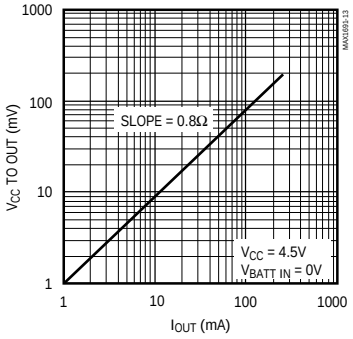
CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



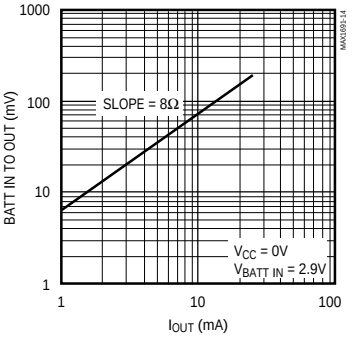
Typical Operating Characteristics (continued)

($V_{BATT\ IN}$ = 2.8V externally applied, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

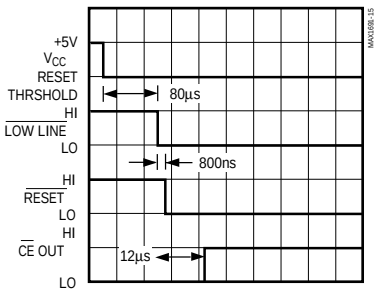
V_{CC} TO V_{OUT} vs. OUTPUT CURRENT (NORMAL OPERATING MODE)



BATT IN TO V_{OUT} vs. OUTPUT CURRENT (BATTERY-BACKUP MODE)



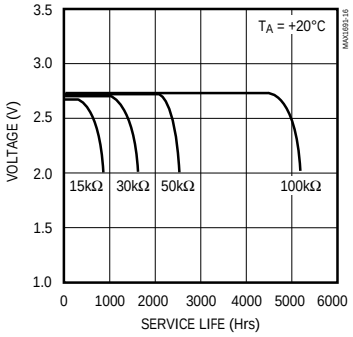
V_{CC} TO $\overline{\text{LOW LINE}}$ AND $\overline{\text{CE}}$ OUT DELAY



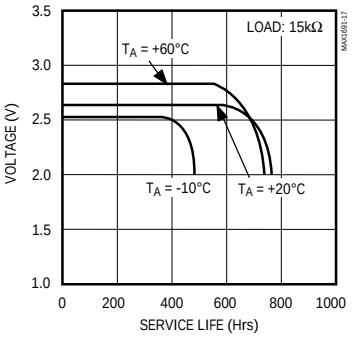
Typical Battery Characteristics*

(Note 9)

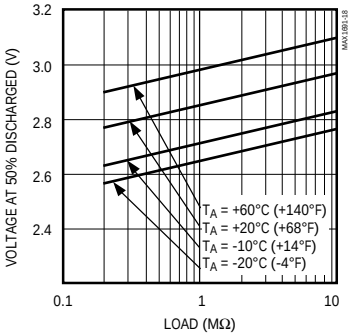
LOAD CHARACTERISTICS



TEMPERATURE CHARACTERISTICS



EFFECT OF LOAD RESISTANCE ON OPERATING VOLTAGE



*Source: Rayovac

Note 9: Nominal voltage is 3.0V, nominal capacity is 130mAh at 30kΩ to 2.0V at +21°C. Typical storage life is less than 0.5% per year at +21°C. Operating temperature range is -40°C to +70°C; prolonged operation and/or storage at elevated temperatures affects life and reliability.

Pin Description

PIN	NAME	FUNCTION
1	BATT IN	Backup-battery input. Connect to BATT OUT.
2	OUT	Output supply voltage connects to V_{CC} when V_{CC} is greater than $V_{BATT\ IN}$ and above the reset threshold. When V_{CC} falls below $V_{BATT\ IN}$ and is below the reset threshold, OUT connects to BATT IN. Connect a 0.1µF capacitor from OUT to GND.
3	V_{CC}	Input supply voltage, +5V input.
4	GND	Ground. 0V reference for all signals. Connected to the negative terminal of the internal battery.
5	BATT ON	Battery-on output goes high when OUT switches to BATT IN. BATT ON goes low when OUT switches to V_{CC}. Connect the base of a PNP to BATT ON for OUT current requirements greater than 250mA.
6	OSC IN	External oscillator input . When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. The timing can be adjusted by connecting an external capacitor to this pin (Figure 2). When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog timeout periods.
7	OSC SEL	Oscillator select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and the watchdog timeout period. Setting OSC SEL low enables OSC IN (Table 1). OSC SEL has a 10µA internal pull-up.
8	PFI	Power-fail input is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or OUT when not used.
9	$\overline{PFO}$	Power-fail output is the output of the power-fail comparator. $\overline{PFO}$ goes low when PFI is less than 1.25V. $\overline{PFO}$ is an uncommitted comparator, and has no effect on any other internal circuitry.
10	$\overline{LOW\ LINE}$	$\overline{LOW\ LINE}$ output goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
11	WDI	Watchdog input—a three level input. If WDI remains either high or low for longer than the watchdog timeout period, reset is asserted. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between OUT and GND that sets it to mid-supply when left unconnected.
12	$\overline{CE}$ OUT	Chip-enable output goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 12µs or until $\overline{CE}$ IN goes high, whichever occurs first.
13	$\overline{CE}$ IN	Chip-enable input to $\overline{CE}$ gating circuit. Connect to GND or OUT if not used.
14	$\overline{RESET}$	$\overline{RESET}$ output goes low whenever V_{CC} falls below the reset threshold. RESET remains low typically for 200ms after V_{CC} crosses the reset threshold on power-up.
15	RESET	Active-high reset output is open drain and the inverse of $\overline{RESET}$.
16	BATT OUT	Battery output connects to the positive terminal of the internal 125mAh lithium battery. Connect BATT OUT to BATT IN.

Integrated µP Supervisor Module with Lithium Backup Battery

Detailed Description

The MAX1691 combines a MAX691A integrated circuit and a 125mAh battery in one package. All pins on the MAX691A are available on the MAX1691 except $\overline{WDO}$. The MAX1691 is not pin compatible with the MAX691A.

$\overline{RESET}$ and RESET Outputs

The MAX1691's $\overline{RESET}$ and RESET outputs ensure the µP (with reset inputs either asserted high or low) powers up in a known state and prevent code execution errors during power-down or brownout conditions.

The active-low $\overline{RESET}$ output both sources and sinks current, while the open-drain RESET output sinks current only. For a battery voltage ≥ 2V, RESET and $\overline{RESET}$ remain valid for V_{CC} from 0V to 5.5V. RESET and $\overline{RESET}$are asserted when V_{CC} falls below the 4.65V reset threshold and typically remain asserted for 200ms after V_{CC} rises above the reset threshold on power-up (Figure 1). The MAX1691 battery switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter battery-backup mode.

Watchdog Function

The watchdog monitors µP activity via the watchdog input (WDI). If the µP becomes inactive, $\overline{RESET}$ and RESET are asserted. To use the watchdog function, connect WDI to a bus line or µP input/output (I/O) line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), RESET and $\overline{RESET}$ are asserted (see *RESET and $\overline{RESET}$ Outputs* section).

WDI Watchdog Input

Changing WDI's state (high-to-low, low-to-high, or a minimum 100ns pulse) during the watchdog period resets the watchdog timer. The watchdog timer default period is 1.6sec.

Disable the watchdog function by floating WDI. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Selecting Alternative Watchdog and Reset Timeout Periods

The OSC SEL and OSC IN inputs control the watchdog and reset timeout periods. Floating OSC SEL and OSC IN or tying them both to OUT selects the nominal 1.6sec watchdog timeout period and 200ms reset timeout period. Connecting OSC IN to GND and floating or

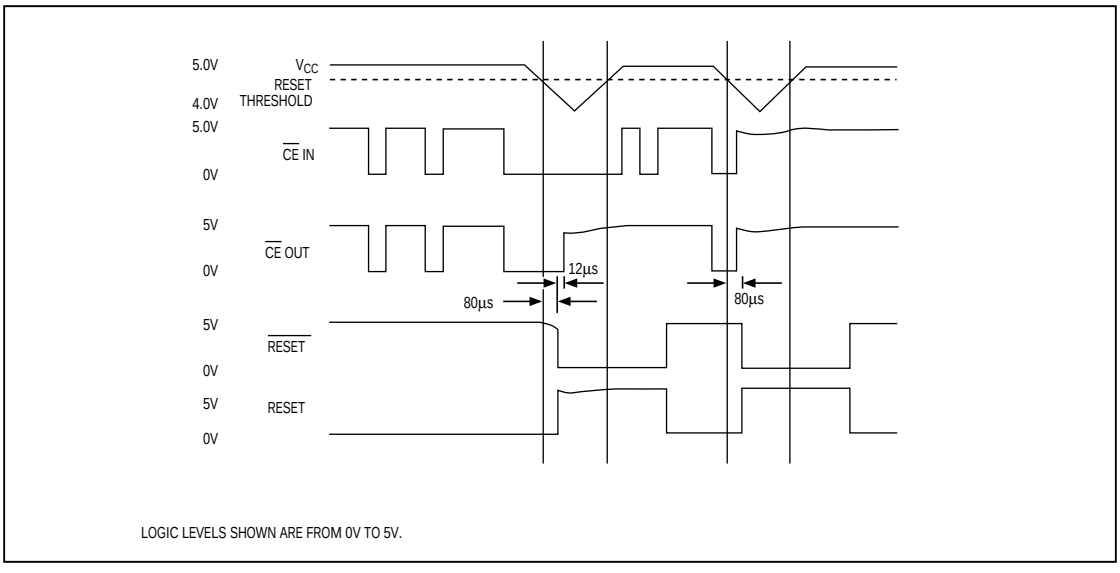


Figure 1. Reset and Chip-Enable Timing

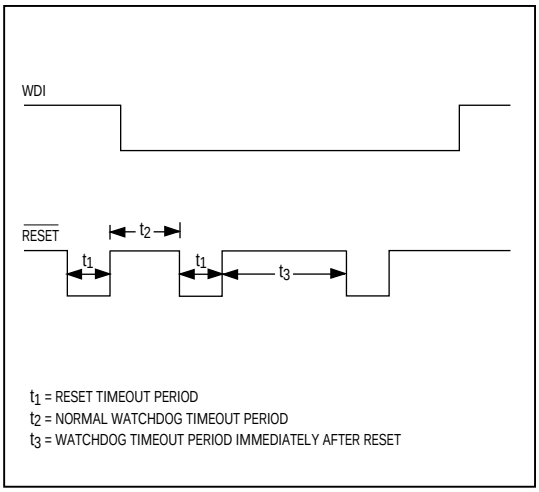


Figure 2. Watchdog Timeout Period and Reset Active Time

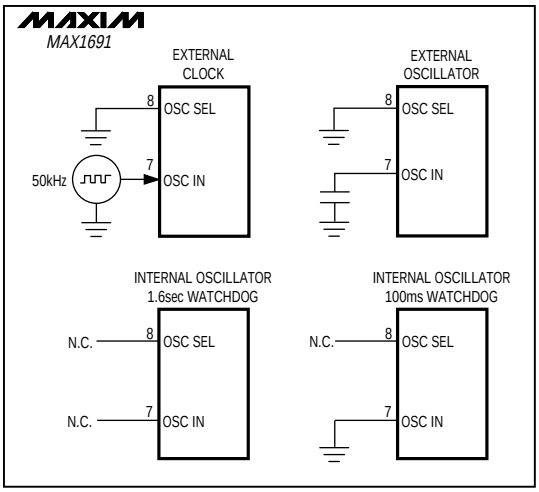


Figure 3. Oscillator Circuits

Table 1. Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External clock input	1-24 clks	4096 clks	2048 clks
Low	External capacitor	(600/47pF x C)ms	(2.4/47pF x C)sec	(1200/47pF x C)ms
Floating	Low	100ms	1.6sec	200ms
Floating	Floating	1.6sec	1.6sec	200ms

connecting OSC SEL to OUT selects the 100ms normal watchdog timeout delay and 1.6sec delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and a capacitor between OSC IN and GND or externally driving OSC IN (see Table 1 and Figure 3).

Chip-Enable Signal Gating

The MAX1691 provides internal gating of chip-enable signals to prevent erroneous data from being written to CMOS RAM in case of power failure. During normal operation, the chip-enable gate is enabled and passes all chip-enable (CE) transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX1691 uses a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 4).

The 10ns (max) CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT makes the MAX1691 compatible with most µPs (Figure 5 shows the test circuit for CE propagation delay).

$\overline{CE}$ IN Chip-Enable Input

$\overline{CE}$ IN is high impedance (disabled mode) while RESET and $\overline{RESET}$ are asserted.

During a power-down sequence where V_{CC} falls below the reset threshold, or when a watchdog fault occurs, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 1).

During a power-up sequence, $\overline{CE}$ IN remains high impedance regardless of $\overline{CE}$ IN activity until reset is deasserted following the reset timeout period. In the low-impedance mode, $\overline{CE}$ IN's impedance appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on the chip-enable output ($\overline{CE}$ OUT) (see Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay

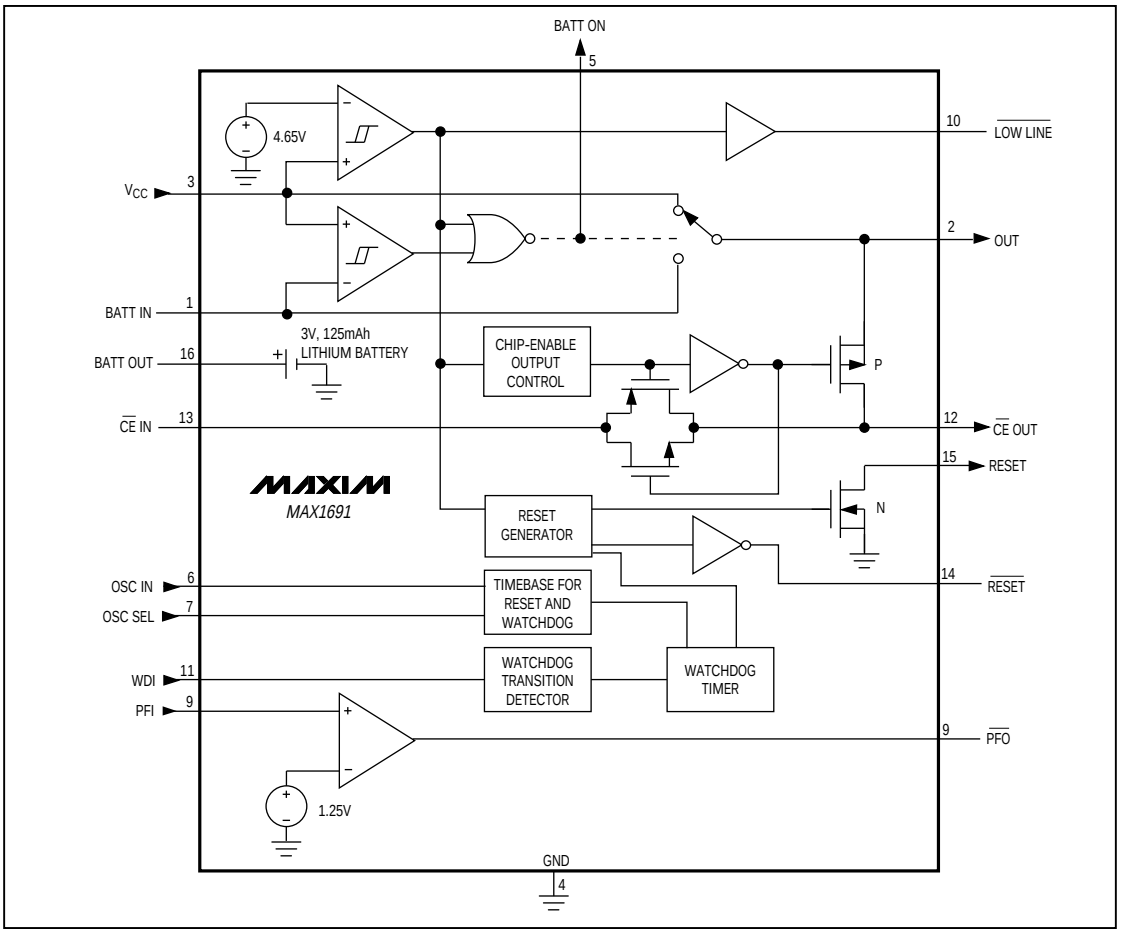


Figure 4. Block Diagram

is production tested from the 50% point of $\overline{CE}$ IN to the 50% point of $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 5). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low output impedance driver.

Chip-Enable Output $\overline{CE}$ OUT

In the enabled mode, $\overline{CE}$ OUT's impedance is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω analog switch is off and $\overline{CE}$ OUT is pulled to OUT. This source turns off when the analog gate is enabled.

$\overline{LOW\ LINE}$ Output

$\overline{LOW\ LINE}$ is the buffered output of the reset threshold comparator and is pulled low when V_{CC} is below the reset threshold. For normal operation (V_{CC} above the reset threshold), $\overline{LOW\ LINE}$ is pulled to OUT.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the IC's other functions. Common uses include low-battery indication (Figure 6) and early power-fail warning (see *Typical Operating Circuit*).

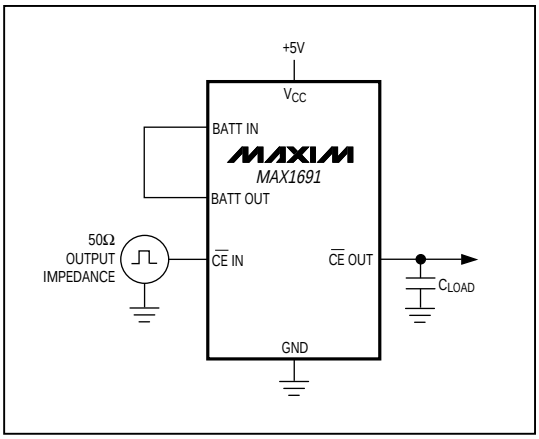


Figure 5. CE Propagation Delay Test Circuit

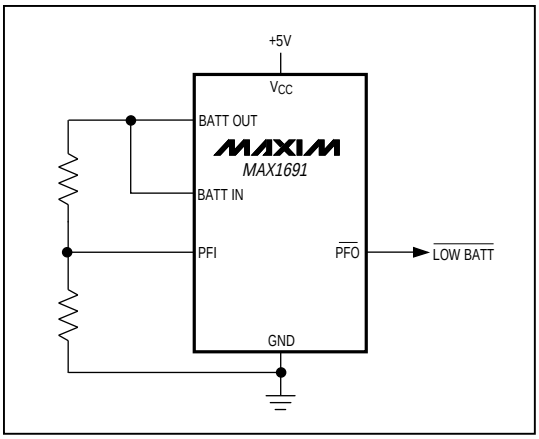


Figure 6. Low-Battery Indicator

PFI Power-Fail Input

PFI is the power-fail comparator's input. PFI has a guaranteed maximum input leakage of ±25nA over temperature, so the current through the resistive divider connected to PFI should be at least 1µA to maintain trip point accuracy. The typical comparator delay is 25µs from V_{IL} to V_{OL}, and 70µs from V_{IH} to V_{OH}. If unused, connect PFI to ground.

$\overline{PFO}$ Power-Fail Output

The power-fail output ($\overline{PFO}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a 0.1V saturation voltage. With PFI above 1.25V, $\overline{PFO}$ is pulled to OUT with only 1µA source capability, so an external pull-up resistor is often required.

Battery-Backup Mode

The MAX1691 requires two conditions to switch to battery-backup mode: (1) V_{CC} must be below the reset threshold, and (2) V_{CC} must be below $V_{BATT\ IN}$. Table 2 lists the status of the inputs and outputs in battery-backup mode.

BATT ON Output

The battery-on (BATT ON) output indicates the status of the internal V_{CC}/battery switchover comparator, which in turn controls the internal V_{CC} and battery switches. For V_{CC} greater than $V_{BATT\ IN}$ (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at less than 0.1V saturation voltage. In battery-backup mode, BATT ON is pulled up to OUT. Use BATT ON to indicate battery switchover status or to supply base drive to an external PNP pass transistor for higher current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The input supply voltage (V_{CC}) should be a regulated +5V. V_{CC} connects to OUT through a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A without damage (Figure 7).

Backup-Battery Input

The backup-battery input (BATT IN) is similar to the V_{CC} input except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of both the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of BATT IN is less than 1µA over temperature and supply voltage. To use the internal 125mAh backup battery, connect BATT IN to BATT OUT.

Output Supply Voltage

The output supply voltage (OUT) pin internally connects to the IC's substrate and supplies current to the external system and internal circuitry. All open-circuit outputs except RESET will, for example, assume V_{OUT} in their high states and not the V_{CC} voltage. At the maximum source current of 250mA, V_{OUT} is typically 200mV below V_{CC}. Decouple this terminal with a 0.1µF capacitor to GND.

Table 2. Input and Output Status in Battery-Backup Mode

PIN	NAME	STATUS
1	BATT IN	Supply current is 1µA maximum.
2	OUT	OUT is connected to BATT IN through an internal PMOS switch.
3	V_{CC}	Battery switchover comparator monitors V_{CC} for active switchover.
4	GND	GND, 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V_{OUT}.
6	OSC IN	OSC IN is ignored.
7	OSC SEL	OSC SEL is ignored.
8	PFI	The power-fail comparator remains active in battery-backup mode until V_{CC} < VBATT IN - 1.2V, below which PFI is inactive.
9	$\overline{PFO}$	The power-fail comparator remains active in battery-backup mode until V_{CC} < VBATT IN - 1.2V, below which $\overline{PFO}$ is inactive.
10	$\overline{LOWLINE}$	Logic low.
11	WDI	Watchdog is ignored.
12	$\overline{CE}$ IN	High impedance.
13	$\overline{CE}$ OUT	Logic high. The open-circuit voltage is equal to V_{OUT}.
14	$\overline{RESET}$	Logic low.
15	RESET	High impedance.
16	BATT OUT	Connect BATT OUT to BATT IN.

Applications Information

The MAX1691 is not short-circuit protected. Shorting OUT to ground will destroy the device.

If long leads connect to the chip inputs, ensure these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

Storing the MAX1691 in conductive foam can slowly discharge the internal battery.

There are three distinct modes of operation:

(1) Normal operating mode with all circuitry powered up. Typical supply current from V_{CC} is 35µA while only leakage currents (<1µA) flow from the battery.

(2) Battery-backup mode where V_{CC} is typically within 1.2V below $V_{BATT\ IN}$. All circuitry is powered up and the supply current from the battery is typically less than 60µA.

(3) Battery-backup mode where V_{CC} is less than $V_{BATT\ IN}$ by at least 1.2V. BATT IN supply current is 1µA max.

Alternative CE Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to OUT and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device as in Figure 8. The CE input of each part then connects directly to the chip select logic, which then does not have to be gated.

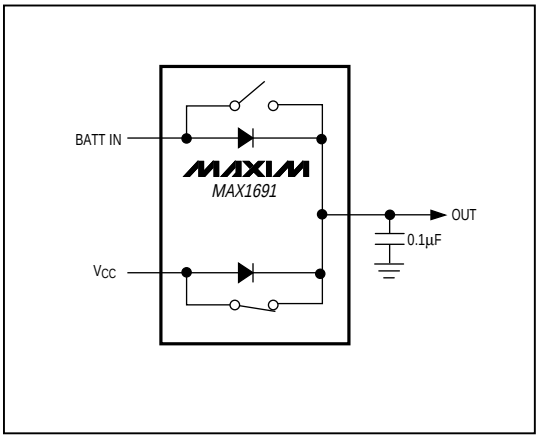


Figure 7. V_{CC} and BATT IN to OUT Switch

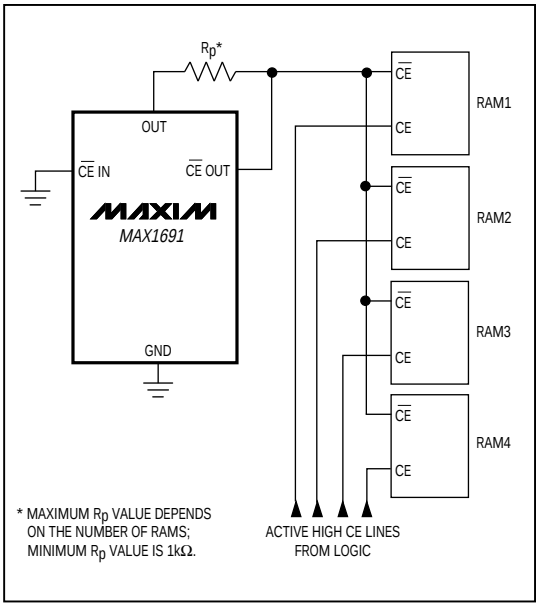


Figure 8. Alternate CE Gating

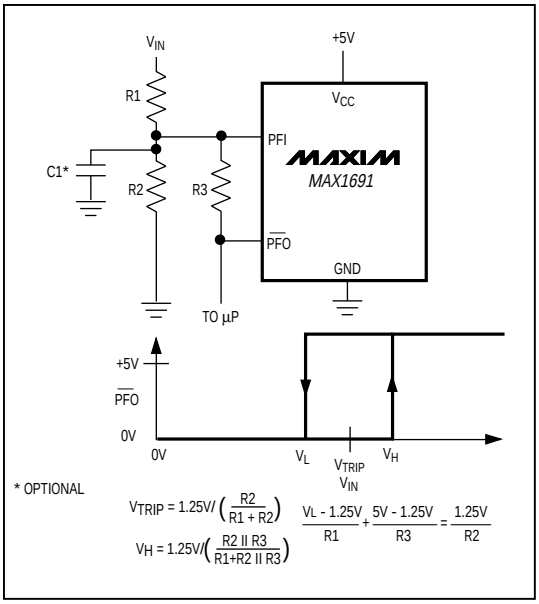


Figure 9. Adding Hysteresis to the Power-Fail Comparator

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when V_{IN} is near the power-fail comparator trip point. Figure 9 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 is optional and adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 10's circuit. $\overline{PFO}$ is low when the negative supply is valid. $\overline{PFO}$ goes high when the negative supply voltage droops. This circuit's accuracy is affected by variations in the PFI threshold, the V_{CC} voltage, and resistors R1 and R2.

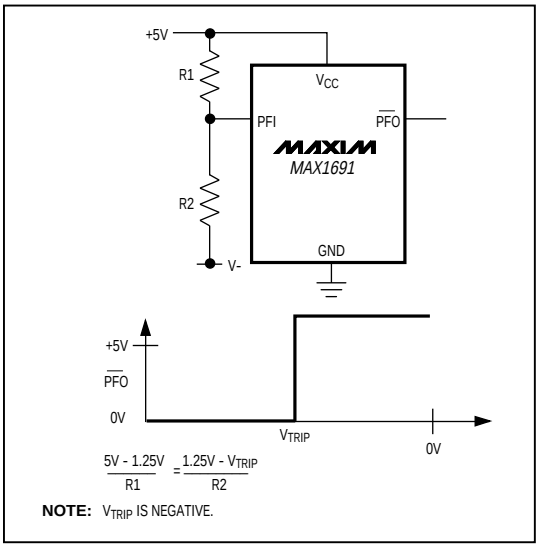


Figure 10. Monitoring a Negative Voltage

Integrated µP Supervisor Module with Lithium Backup Battery

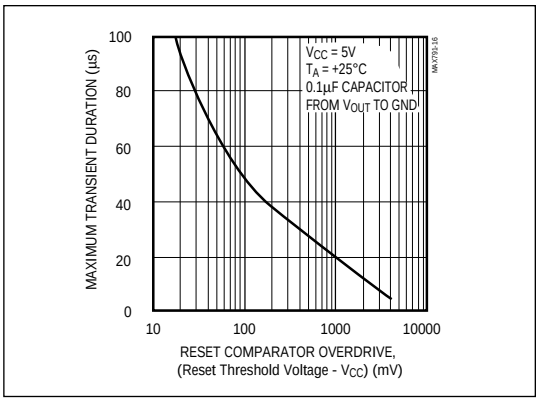


Figure 11. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 11 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Connecting a Timing Capacitor at OSC IN

When OSC SEL is connected to ground, OSC IN disconnects from its internal 10µA (typ) pull-up and is internally connected to a ±100nA current source. When a capacitor is connected from OSC IN to ground (to select alternative reset and watchdog timeout periods), the current source charges and discharges the timing capacitor to create the oscillator that controls the reset and watchdog timeout period. To prevent timing errors or oscillator start-up problems, minimize external current leakage sources at this pin, and locate the capacitor as close to OSC IN as possible. The sum of PC board leakage + OSC capacitor leakage must be small compared to ±100nA.

Maximum V_{CC} Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule of thumb for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse or 1A/100µF = 0.01V/µs. The V_{CC} fall rate decreases with time as V_{CC} falls exponentially, which more than satisfies the maximum fall-time requirement.

Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 12 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

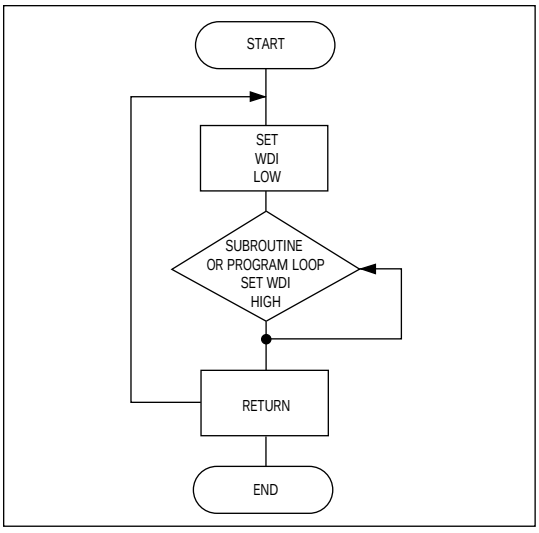
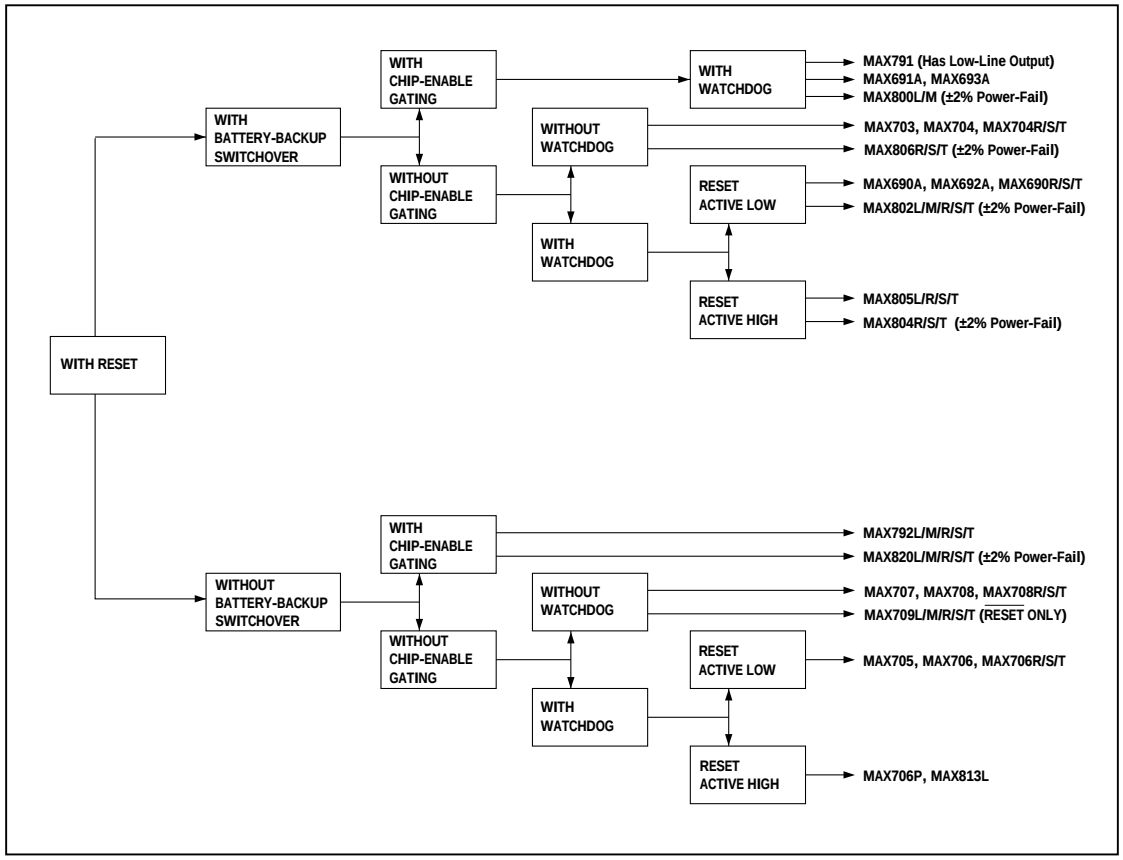
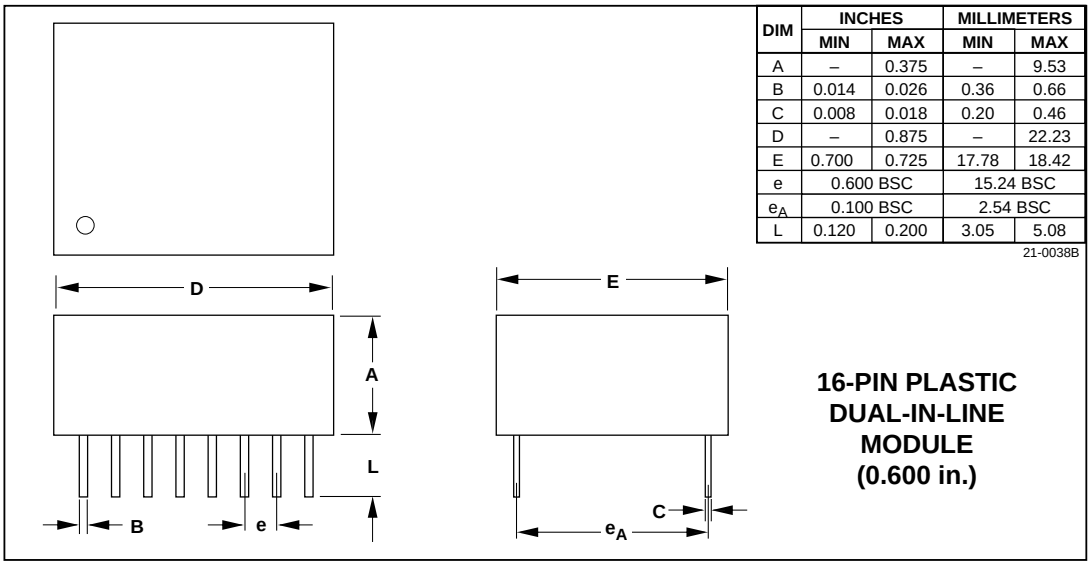


Figure 12. Watchdog Flow Diagram


WITH RESET
WITH BATTERY-BACKUP SWITCHOVER
WITH CHIP-ENABLE GATING
WITHOUT CHIP-ENABLE GATING
WITH WATCHDOG
WITHOUT WATCHDOG
RESET ACTIVE LOW
RESET ACTIVE HIGH
MAX791 (Has Low-Line Output)
MAX691A, MAX693A
MAX800L/M (±2% Power-Fail)
MAX703, MAX704, MAX704R/S/T
MAX806R/S/T (±2% Power-Fail)
MAX690A, MAX692A, MAX690R/S/T
MAX802L/M/R/S/T (±2% Power-Fail)
MAX805L/R/S/T
MAX804R/S/T (±2% Power-Fail)
WITHOUT BATTERY-BACKUP SWITCHOVER
WITH CHIP-ENABLE GATING
WITHOUT CHIP-ENABLE GATING
WITH WATCHDOG
WITHOUT WATCHDOG
RESET ACTIVE LOW
RESET ACTIVE HIGH
MAX792L/M/R/S/T
MAX820L/M/R/S/T (±2% Power-Fail)
MAX707, MAX708, MAX708R/S/T
MAX709L/M/R/S/T (RESET ONLY)
MAX705, MAX706, MAX706R/S/T
MAX706P, MAX813L

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.375	–	9.53
B	0.014	0.026	0.36	0.66
C	0.008	0.018	0.20	0.46
D	–	0.875	–	22.23
E	0.700	0.725	17.78	18.42
e	0.600 BSC		15.24 BSC	
e_A	0.100 BSC		2.54 BSC	
L	0.120	0.200	3.05	5.08

21-0038B

16-PIN PLASTIC DUAL-IN-LINE MODULE (0.600 in.)