

General Description

The MAX9110/MAX9112 single/dual low-voltage differential signaling (LVDS) transmitters are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single +3.3V supply, and feature ultra-low 250ps (max) pulse skew required for high-resolution imaging applications, such as laser printers and digital copiers.

The MAX9110 is a single LVDS transmitter, and the MAX9112 is a dual LVDS transmitter.

Both devices conform to the EIA/TIA-644 LVDS standard. They accept LVTTL/CMOS inputs and translate them to low-voltage (350mV) differential outputs, minimizing electromagnetic interference (EMI) and power dissipation. These devices use a current-steering output stage, minimizing power consumption, even at high data rates. The MAX9110/MAX9112 are available in space-saving 8-pin SOT23 and SO packages. Refer to the MAX9111/ MAX9113 data sheet for single/dual LVDS line receivers.

Applications

Laser Printers Network Switches/Routers **Digital Copiers** LCD Displays Cellular Phone Base Backplane Interconnect Stations Clock Distribution

Features

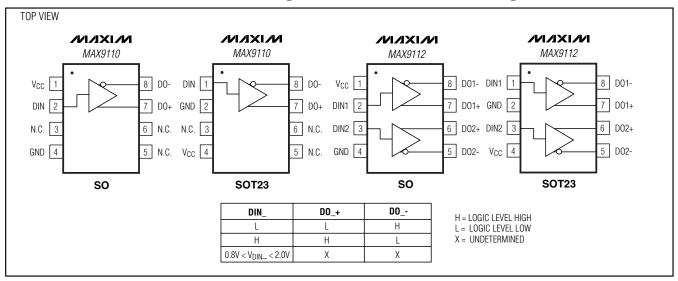
- ♦ Low 250ps (max) Pulse Skew for High-Resolution **Imaging and High-Speed Interconnect**
- ♦ Space-Saving 8-Pin SOT23 and SO Packages
- ♦ Pin-Compatible Upgrades to DS90LV017/017A and DS90LV027/027A (SO Packages)
- ♦ Guaranteed 500Mbps Data Rate
- ♦ Low 22mW Power Dissipation at 3.3V (31mW for MAX9112)
- ♦ Conform to EIA/TIA-644 Standard
- ♦ Single +3.3V Supply
- **♦** Flow-Through Pinout Simplifies PC Board Layout
- ♦ Driver Outputs High Impedance when Powered Off

Ordering Information

PART	TEMP. RANGE	PIN- PACKAGE	TOP MARK	
MAX9110EKA-T	-40°C to +85°C	8 SOT23-8	AADN	
MAX9110ESA	-40°C to +85°C	8 SO	_	
MAX9112 EKA-T	-40°C to +85°C	8 SOT23-8	AADO	
MAX9112ESA	-40°C to +85°C	8 SO	_	

Typical Operating Circuit appears at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Table



MIXIM

Telecom Switching

Equipment

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC} to GND)0.3V to +4V	Continuous
Input Voltage (V _{DIN} to GND)0.3V to (V _{CC} + 0.3V)	8-Pin S0
Output Voltage (VDO_+, VDO to GND or VCC)0.3V to +3.9V	8-Pin S0
Output Short-Circuit Duration	Operating
(DO_+, DO to V _{CC} or GND)Continuous	Storage Te
ESD Protection (Human Body Model, DO_+, DO)±11kV	Lead Temp

Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
8-Pin SOT23 (derate 7.52mW/°C above +70°C	
8-Pin SO (derate 5.88mW/°C above +70°C).	471mW
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +3.0 \text{V to } +3.6 \text{V}, R_L = 100\Omega \pm 1\%, T_A = -40 ^{\circ}\text{C}$ to $+85 ^{\circ}\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3 \text{V}, T_A = +25 ^{\circ}\text{C}$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
Differential Output Voltage	V _{OD}	Figure 1	250	350	450	mV		
Change in Magnitude of Output Voltage for Complementary Output States	ΔV _{OD}	Figure 1		0	2	35	mV	
Offset Voltage	Vos	Figure 1		1.125	1.25	1.375	V	
Change in Magnitude of Offset Voltage for Complementary Output States	ΔV _{OS}	Figure 1		0	2	25	mV	
Power-Off Leakage Current	IO(OFF)	V_{DO} = 0 or V_{CC} , V_{CC} = 0 or	-10		+10	μΑ		
Short-Circuit Output Current	IO(SHORT)	DIN_ = V _{CC} , V _{DO_+} = 0 or DIN_ = GND, V _{DO_} - = 0				-20	mA	
Input High Voltage	VIH					Vcc	V	
Input Low Voltage	VIL			GND		0.8	V	
Input Current High	lін	DIN_ = V _{CC} or 2V		0	10	20	μΑ	
Input Current Low	Ι _Ι L	DIN_ = GND or 0.8V		-20	-3	0	μΑ	
No-Load Supply Current	Icc	No load, DIN_ = V _{CC} or 0		4.5	6	mA		
Supply Current	Icc	DIN_ = V _{CC} or 0	MAX9110		6.7	8	mA	
Cappiy Carron	100	DII V_ = VOC 51 0	MAX9112		9.4	13	1117 (

AC CHARACTERISTICS

 $(V_{CC} = +3.0 \text{V to } +3.6 \text{V}, R_L = 100\Omega \pm 1\%, C_L = 5 \text{pF}, T_A = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +3.3 \text{V}, T_A = +25 ^{\circ}\text{C}.)$ (Notes 3, 4, 5; Figures 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential High-to-Low Propagation Delay	tpHLD		1	1.54	2.5	ns
Differential Low-to-High Propagation Delay	tpLHD		1	1.58	2.5	ns
Differential Pulse Skew ItPHLD - tPLHDI (Note 6)	tskD1			40	250	ps
Channel-to-Channel Skew (Note 7)	tskD2			70	400	ps

AC CHARACTERISTICS (continued)

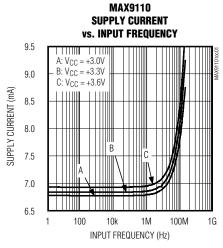
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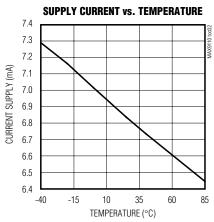
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Part-to-Part Skew	tskD3	(Note 8)			1	
Part-to-Part Skew	t _{SKD4}	(Note 9)			1.5	ns
High-to-Low Transition Time	tTHL		0.25	0.6	1	ns
Low-to-High Transition Time	tTLH		0.25	0.6	1	ns
Maximum Operating Frequency	fMAX	(Note 10)	250			MHz

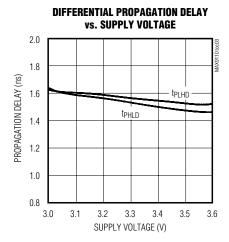
- Note 1: Maximum and minimum limits over temperature are guaranteed by design. Devices are production tested at T_A = +25°C.
- **Note 2:** By definition, current into the device is positive and current out of the device is negative. Voltages are referred to device ground except V_{OD}.
- Note 3: AC parameters are guaranteed by design and characterization.
- Note 4: CL includes probe and fixture capacitance.
- **Note 5:** Signal generator conditions for dynamic tests: $V_{OL} = 0$, $V_{OH} = 3V$, f = 20MHz, 50% duty cycle, $R_O = 50\Omega$, $t_R \le 1$ ns, and $t_F \le 1$ ns (0 to 100%).
- Note 6: tskp1 is the magnitude difference of differential propagation delays in a channel; tskp1 = | tpHLD tpLHD |.
- Note 7: t_{SKD2} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of the other channel on the same device (MAX9112).
- Note 8: t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.
- **Note 9:** t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.
- Note 10: f_{MAX} signal generator conditions: $V_{OL} = 0$, $V_{OH} = +3V$, frequency = 250MHz, $t_R \le 1$ ns, $t_F \le 1$ ns (0 to 100%) 50% duty cycle. Transmitter output criteria: duty cycle = 45% to 55%, $V_{OD} \ge 250$ mV.

Typical Operating Characteristics

 $(V_{CC} = +3.3V, R_L = 100\Omega, C_L = 5pF, V_{IH} = +3V, V_{IL} = GND, f_{IN} = 20MHz, T_A = +25^{\circ}C, unless otherwise noted.)$ (Figures 2, 3)

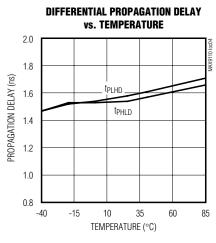


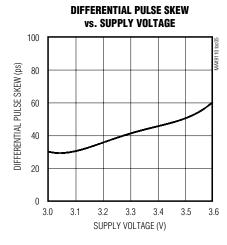


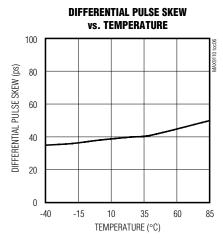


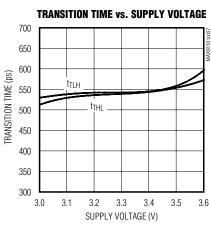
Typical Operating Characteristics (continued)

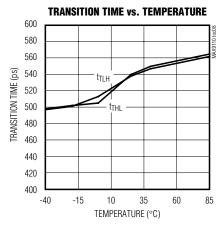
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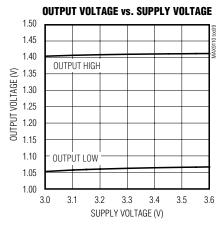


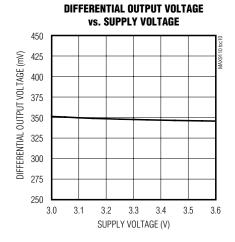


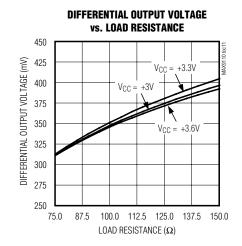






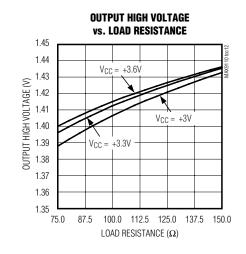


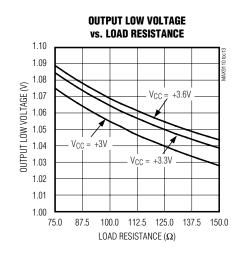




Typical Operating Characteristics (continued)

 $(V_{CC} = +3.3V, R_L = 100\Omega, C_L = 5pF, V_{IH} = +3V, V_{IL} = GND, f_{IN} = 20MHz, T_A = +25^{\circ}C, unless otherwise noted.)$ (Figures 2, 3)





Pin Description

	PIN				
МАХ	9110	MAX	9112	NAME	FUNCTION
SOT23	so	SOT23	so		
4	1	4	1	V _C C	Positive Supply
1	2	_	_	DIN	Transmitter langet
_	_	1, 3	2, 3	DIN1, DIN2	Transmitter Input
3, 5, 6	3, 5, 6	_	_	N.C.	No Connection. Not internally connected.
2	4	2	4	GND	Ground
7	7	_	_	DO+	Nanipuarting Transmitter Output
_	_	6, 7	6, 7	DO2+, DO1+	Noninverting Transmitter Output
8	8	_	_	DO-	Investing Transmitter Output
_	_	5, 8	5, 8	DO2-, DO1-	Inverting Transmitter Output

Detailed Description

The MAX9110/MAX9112 single/dual LVDS transmitters are intended for high-speed, point-to-point, low-power applications. These devices accept CMOS/LVTTL inputs with data rates exceeding 500Mbps. The MAX9110/MAX9112 reduce power consumption and

EMI by translating these signals to a differential voltage in the 250mV to 450mV range across a 100 Ω load while drawing only 9.4mA of supply current for the dual-channel MAX9112.

A current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The output

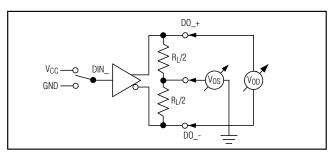


Figure 1. LVDS Transmitter VoD and Vos Test Circuit

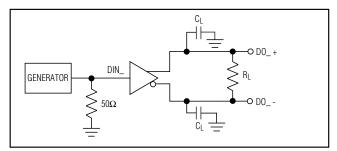


Figure 2. Transmitter Propagation Delay and Transition Time Test Circuit

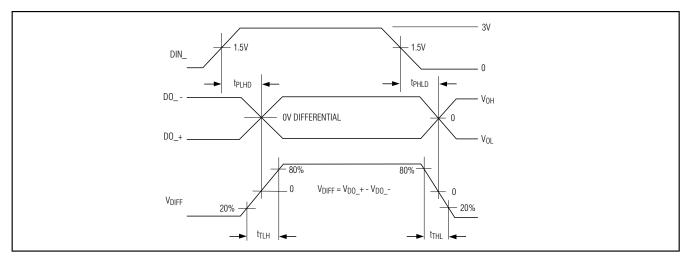


Figure 3. Transmitter Propagation Delay and Transition Time Waveforms

stage presents a symmetrical, high-impedance output, reducing differential reflection and timing distortion. The driver outputs are short circuit current limited and enter a high-impedance state when the device is not powered.

LVDS Operation

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance medium as defined by the EIA/TIA-644 LVDS standard. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

LVDS transmitters such as the MAX9110/MAX9112 convert CMOS/LVTTL signals to low-voltage differential signals at rates in excess of 500Mbps. The MAX9110/MAX9112 current-steering architecture requires a resistive load to terminate the signal and complete the trans-

mission loop. Because the device switches the direction of current flow and not voltage levels, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver. Logic states are determined by the direction of current flow through the termination resistor. With a typical 3.5mA output current, the MAX9110/MAX9112 produce an output voltage of 350mV when driving a 100Ω load. The steady-state-voltage peak-to-peak swing is twice the differential voltage, or 700mV (typ).

Applications Information

Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic $0.1\mu\text{F}$ and $0.001\mu\text{F}$ capacitors in parallel, as close to the device as possible, with the smaller valued capacitor the closest. For additional supply bypassing, place a $10\mu\text{F}$ tantalum or ceramic capacitor at the point where power enters the circuit board.

Differential Traces

Output trace characteristics affect the performance of the MAX9110/MAX9112. Use controlled impedance traces to match trace impedance to both transmission medium impedance and termination resistor. Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a differential characteristic impedance of about 100Ω . Use cables and connectors that have matched impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon or simple coaxial cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

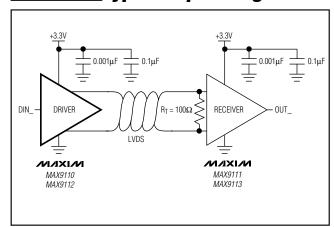
Termination resistors should match the differential characteristic impedance of the transmission line. Because the MAX9110/MAX9112 are current-steering devices, an output voltage will not be generated without a termination resistor. Output voltage levels are dependent upon the termination resistor value. Resistance values may range between 75Ω and 150Ω .

Minimize the distance between the termination resistor and receiver inputs. Use a single 1% to 2% surfacemount resistor across the receiver inputs.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the input and LVDS signals from each other to prevent coupling. Separate the input and LVDS signal planes with the power and ground planes for best results.

Typical Operating Circuit

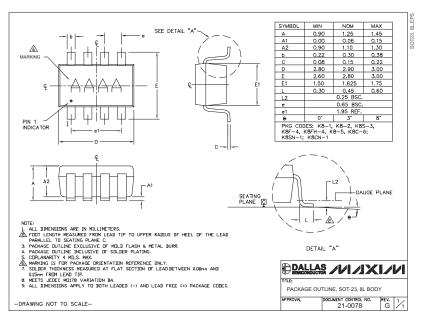


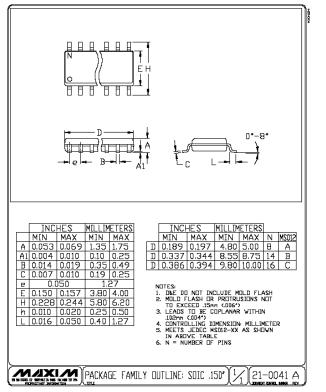
Chip Information

MAX9110 TRANSISTOR COUNT: 765 MAX9112 TRANSISTOR COUNT: 765

PROCESS: CMOS

Package Information





Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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