

MC10E457, MC100E457

5V ECL Triple Differential 2:1 Multiplexer

The MC10E457/100E457 is a 3-bit differential 2:1 multiplexer. The fully differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals.

The higher frequency outputs provide the device with a >1.0 GHz bandwidth to meet the needs of the most demanding system clock.

Both, separate selects and a common select, are provided to make the device well suited for both data path and random logic applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below V_{CC} .

The 100 Series contains temperature compensation.

Multiple V_{BB} pins are provided to ease AC coupling input signals. The V_{BB} pins, internally generated voltage supply pins, are available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

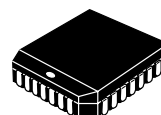
- Differential D and Q; V_{BB} available
- 700 ps Max. Propagation Delay
- High Frequency Outputs
- Separate and Common Select
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 218 devices



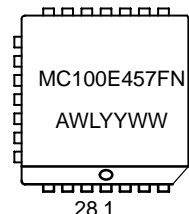
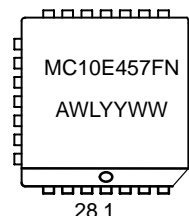
ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAMS



PLCC-28
FN SUFFIX
CASE 776



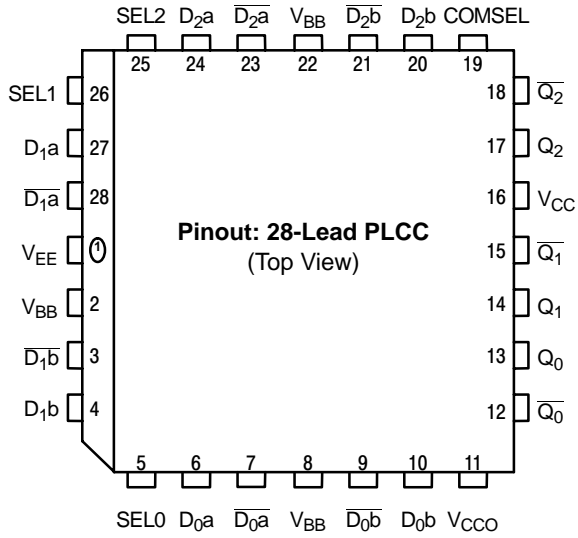
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E457FN	PLCC-28	37 Units/Rail
MC10E457FNR2	PLCC-28	500 Units/Reel
MC100E457FN	PLCC-28	37 Units/Rail
MC100E457FNR2	PLCC-28	500 Units/Reel

MC10E457, MC100E457

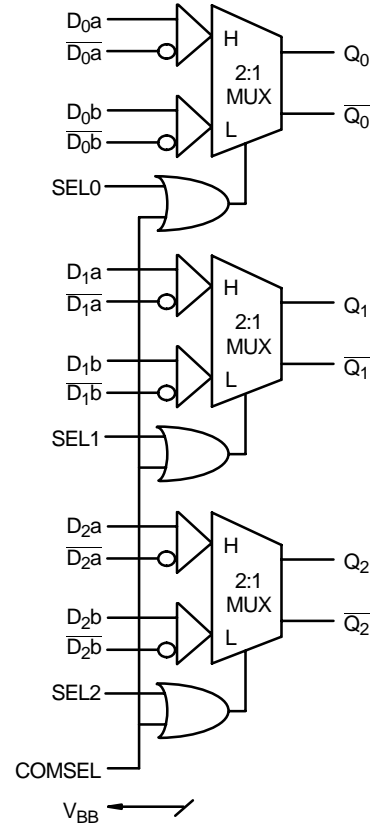
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_n[0:2]; \overline{D}_n[0:2]$	ECL Differential Data Inputs
SEL	ECL Individual Select Input
COMSEL	ECL Common Select Input
$Q[0:2], \overline{Q}[0:2]$	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

SEL	Data
H	a
L	b

MC10E457, MC100E457

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V _{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V V
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		92	110		92	110		92	110	mA
V _{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V _{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= -5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		92	110		92	110		92	110	mA
V _{OH}	Output HIGH Voltage (Note 2.)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V _{OL}	Output LOW Voltage (Note 2.)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V _{IH}	Input HIGH Voltage (Single Ended)	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V _{IL}	Input LOW Voltage (Single Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
V _{BB}	Output Voltage Reference	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	-2.3		0.0	-2.3		0.0	-2.3		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

MC10E457, MC100E457

100E SERIES PECL DC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		92	110		92	110		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

100E SERIES NECL DC CHARACTERISTICS $V_{CCx}=0.0\text{ V}$; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		92	110		92	110		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V_{IL}	Input LOW Voltage (Single Ended)	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	-2.3		0.0	-2.3		0.0	-2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

AC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$; $V_{EE}=0.0\text{ V}$ or $V_{CCx}=0.0\text{ V}$; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz	
t_{PLH} t_{PHL}	Propagation Delay to Output D (Differential) D (Single-Ended) SEL COMSEL	325 275 300 325	475 475 500 525	700 750 775 800				375 325 350 375	475 475 500 525	650 700 725 750		ps
t_{skew}	Within-Device Skew (Note 2.)		40						40		ps	
t_{skew}	Duty Cycle Skew (Note 3.) $t_{PLH} - t_{PHL}$		± 10						± 10		ps	
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps	
$V_{PP(AC)}$	Minimum Input Swing (Note 4.)	150						150			mV	
t_r/t_f	Rise/Fall Time 20-80%	125	275	500				150	275	450	ps	

1. 10 Series: V_{EE} can vary +0.46 V / -0.06 V.
100 Series: V_{EE} can vary +0.46 V / -0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. Minimum input swing for which AC parameters are guaranteed.

MC10E457, MC100E457

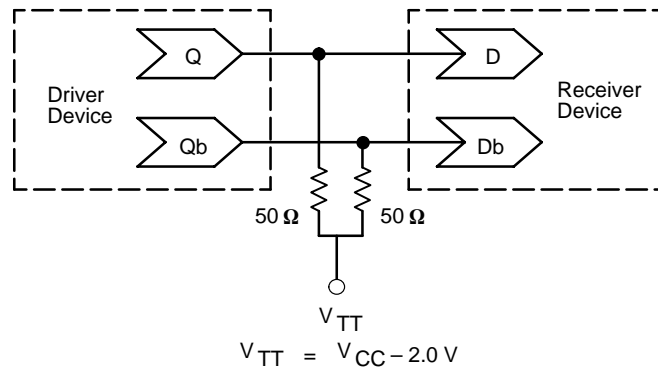


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

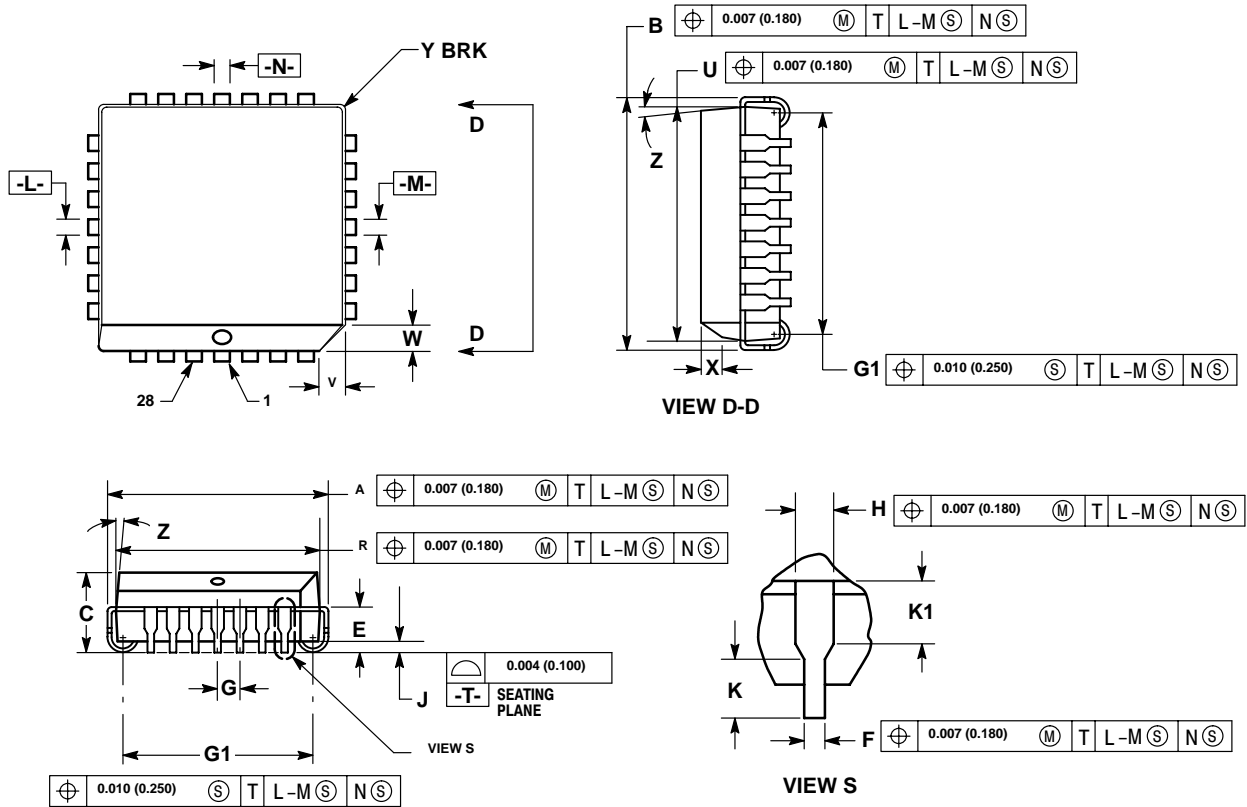
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC10E457, MC100E457

PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.