

## Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

The Motorola MC100ES6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6111 supports various applications that require distribution of precisely aligned differential clock signals. Using SiGe:C technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

- 1:10 differential clock distribution
- 35 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe:C technology supports near-zero output skew
- Supports DC to 2.7 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP111

### Functional Description

The MC100ES6111 is designed for low skew clock distribution systems and supports clock frequencies up to 2.7 GHz. The device accepts two clock sources. The CLKA input can be driven by ECL or PECL compatible signals, the CLKB input accepts HSTL compatible signals. The selected input signal is distributed to 10 identical, differential ECL/PECL outputs. If VBB is connected to the CLKA input and bypassed to GND by a 10 nF capacitor, the MC100ES6111 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6111 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6111 supports positive (PECL) and negative (ECL) supplies. The MC100ES6111 is pin and function compatible to the MC100EP111.

**MC100ES6111**

**LOW-VOLTAGE  
1:10 DIFFERENTIAL  
ECL/PECL/HSTL  
CLOCK FANOUT DRIVER**



**FA SUFFIX**  
32-LEAD LQFP PACKAGE  
CASE 873A

# MC100ES6111

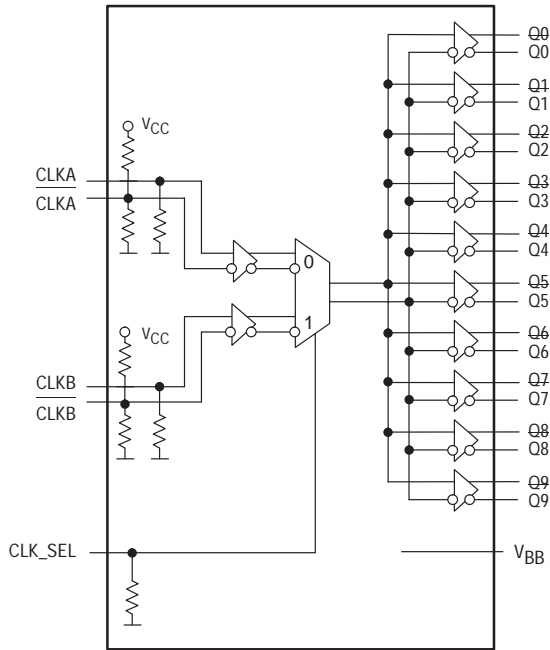


Figure 1. MC100ES6111 Logic Diagram

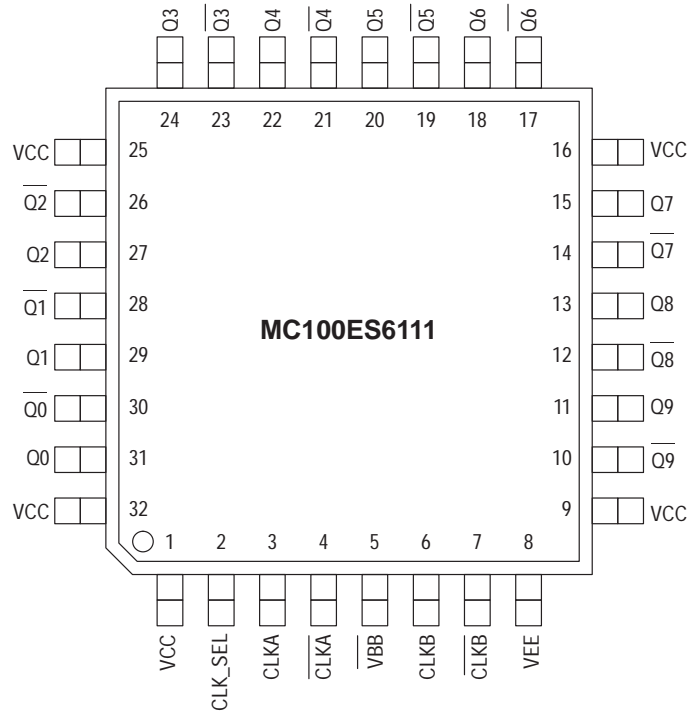


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CLKA, CLKA	Input	ECL/PECL	Differential reference clock signal input
CLKB, CLKB	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Active clock input select
Q[0–9], Q[0–9]	Output	ECL/PECL	Differential clock outputs
VEE <sup>a</sup>	Supply		Negative power supply
VCC	Supply		Positive power supply. All VCC pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V). In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	0	CLKA, CLKA input pair is active. CLKA can be driven by ECL or PECL compatible signals.	CLKB, CLKB input pair is active. CLKB can be driven by HSTL compatible signals.

**Table 3. Absolute Maximum Ratings<sup>a</sup>**

Symbol	Characteristics	Min	Max	Unit	Condition
V <sub>CC</sub>	Supply Voltage	-0.3	3.6	V	
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> + 0.3	V	
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> + 0.3	V	
I <sub>IN</sub>	DC Input Current		±20	mA	
I <sub>OUT</sub>	DC Output Current		±50	mA	
T <sub>S</sub>	Storage temperature	-65	125	°C	
T <sub>Func</sub>	Functional temperature range	T <sub>A</sub> = -40	T <sub>J</sub> = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>TT</sub>	Output termination voltage		V <sub>CC</sub> - 2 <sup>a</sup>		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	4000			V	
CDM	ESD Protection (Charged device model)	2000			V	
LU	Latch-up immunity	200			mA	
C <sub>IN</sub>			4.0		pF	Inputs
θ <sub>JA</sub>	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1 73.3 68.9 63.8 57.4	86.0 75.4 70.9 65.3 59.6	°C/W °C/W °C/W °C/W °C/W	Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0 54.4 52.5 50.4 47.8	60.6 55.7 53.8 51.5 48.8	°C/W °C/W °C/W °C/W °C/W	Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
θ <sub>JC</sub>	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T <sub>J</sub>	Operating junction temperature <sup>b</sup> (continuous operation) MTBF = 9.1 years			110	°C	

- a. Output termination voltage V<sub>TT</sub> = 0V for V<sub>CC</sub> = 2.5V operation is supported but the power consumption of the device will increase
- b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. PECL/HSTL DC Characteristics** ( $V_{CC} = 2.5V \pm 5\%$  or  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = GND$ ,  $T_J = 0^\circ C$  to  $+110^\circ C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control input CLK_SEL						
$V_{IL}$	Input voltage low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
$V_{IH}$	Input voltage high	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
$I_{IN}$	Input Current <sup>a</sup>			100	$\mu A$	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLKA, CLKA (PECL differential signals)						
$V_{PP}$	Differential input voltage <sup>b</sup>	0.1		1.3	V	Differential operation
$V_{CMR}$	Differential cross point voltage <sup>c</sup>	1.0		$V_{CC} - 0.3$	V	Differential operation
$I_{IN}$	Input Current <sup>a</sup>			100	$\mu A$	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLKB, CLKB (HSTL differential signals)						
$V_{DIF}$	Differential input voltage <sup>d</sup>				V	
	$V_{CC} = 3.3V$	0.4			V	
	$V_{CC} = 2.5V$	0.4			V	
$V_X$	Differential cross point voltage <sup>e</sup>	0.68		0.9	V	
$I_{IN}$	Input Current			200	$\mu A$	$V_{IN} = V_X \pm 0.2V$
PECL clock outputs (Q0-9, Q0-9)						
$V_{OH}$	Output High Voltage	$V_{CC} - 1.2$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 mA^f$
$V_{OL}$	Output Low Voltage	$V_{CC} = 3.3V \pm 5\%$ $V_{CC} = 2.5V \pm 5\%$	$V_{CC} - 1.9$ $V_{CC} - 1.9$	$V_{CC} - 1.705$ $V_{CC} - 1.705$	$V_{CC} - 1.5$ $V_{CC} - 1.3$	$I_{OL} = -5 mA^f$
Supply current and $V_{BB}$						
$I_{EE}$	Maximum Quiescent Supply Current without output termination current <sup>g</sup>			100	mA	$V_{EE}$ pin
$V_{BB}$	Output reference voltage	$V_{CC} - 1.4$		$V_{CC} - 1.2$	V	$I_{BB} = 200 \mu A$

a. Input have internal pullup/pulldown resistors which affect the input current

b.  $V_{PP}$  (DC) is the minimum differential input voltage swing required to maintain device functionality

c.  $V_{CMR}$  (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the  $V_{CMR}$  (DC) range and the input swing lies within the  $V_{PP}$  (DC) specification.

d.  $V_{DIF}$  (DC) is the minimum differential HSTL input voltage swing required for device functionality.

e.  $V_X$  (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the  $V_X$  (DC) range and the input swing lies within the  $V_{PP}$  (DC) specification.

f. Equivalent to a termination of  $50\Omega$  to  $V_{TT}$ .

g.  $I_{CC}$  calculation:  $I_{CC} = (\text{number of differential output pairs used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$$I_{CC} = (\text{number of differential output pairs used}) \times (V_{OH} - V_{TT})/R_{load} + (V_{OL} - V_{TT})/R_{load} + I_{EE}$$

**Table 6. ECL DC Characteristics** ( $V_{EE} = -2.5V \pm 5\%$  or  $V_{EE} = -3.3V \pm 5\%$ ,  $V_{CC} = GND$ ,  $T_J = 0^\circ C$  to  $+110^\circ C$ )

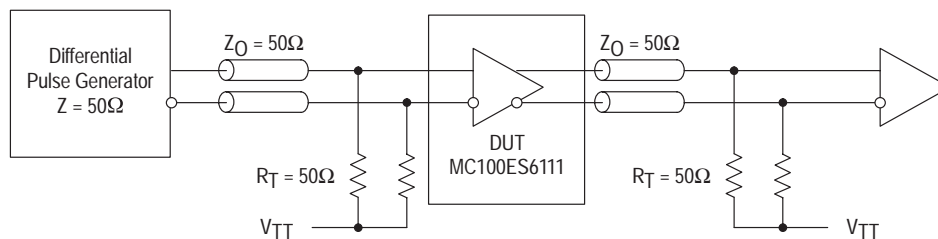
Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control input CLK_SEL						
$V_{IL}$	Input voltage low	-1.810		-1.475	V	
$V_{IH}$	Input voltage high	-1.165		-0.880	V	
$I_{IN}$	Input Current <sup>a</sup>			100	$\mu A$	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLKA, CLKB, CLKB (ECL differential signals)						
$V_{PP}$	Differential input voltage <sup>b</sup>	0.1		1.3	V	Differential operation
$V_{CMR}$	Differential cross point voltage <sup>c</sup>	$V_{EE} + 1.0$		-0.3	V	Differential operation
$I_{IN}$	Input Current <sup>a</sup>			100	$\mu A$	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (Q0-9, Q0-9)						
$V_{OH}$	Output High Voltage	-1.2	-1.005	-0.7	V	$I_{OH} = -30 \text{ mA}^d$
$V_{OL}$	Output Low Voltage	$V_{EE} = -3.3V \pm 5\%$ $V_{EE} = -2.5V \pm 5\%$	-1.9 -1.9	-1.705 -1.705	-1.5 -1.3	V $I_{OL} = -5 \text{ mA}^d$
Supply current and $V_{BB}$						
$I_{EE}$	Maximum Quiescent Supply Current without output termination current <sup>e</sup>			100	mA	$V_{EE}$ pin
$V_{BB}$	Output reference voltage	$V_{CC} - 1.4$		$V_{CC} - 1.2$	V	$I_{BB} = 200 \mu A$

- a. Input have internal pullup/pulldown resistors which affect the input current
- b.  $V_{PP}$  (DC) is the minimum differential input voltage swing required to maintain device functionality
- c.  $V_{CMR}$  (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the  $V_{CMR}$  (DC) range and the input swing lies within the  $V_{PP}$  (DC) specification.
- d. Equivalent to a termination of  $50\Omega$  to  $V_{TT}$ .
- e.  $I_{CC}$  calculation:  $I_{CC} = (\text{number of differential output pairs used}) \times (I_{OH} + I_{OL}) + I_{EE}$   
 $I_{CC} = (\text{number of differential output pairs used}) \times (V_{OH} - V_{TT})/R_{load} + (V_{OL} - V_{TT})/R_{load} + I_{EE}$ .

**Table 7. AC Characteristics** (ECL:  $V_{EE} = -3.3V \pm 5\%$  or  $V_{EE} = -2.5V \pm 5\%$ ,  $V_{CC} = GND$ ) or (HSTL/PECL:  $V_{CC} = 3.3V \pm 5\%$  or  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = GND$ ,  $T_J = 0^\circ C$  to  $+ 110^\circ C$ ) <sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, CLKB (PECL or ECL differential signals)						
$V_{PP}$	Differential input voltage <sup>b</sup> (peak-to-peak)	0.15		1.3	V	
$V_{CMR}$	Differential input crosspoint voltage <sup>c</sup>					
	PECL	$V_{EE} + 1.0$		$V_{CC} - 0.3$	V	
$f_{CLK}$	Input Frequency <sup>d</sup>			2.7	GHz	Differential
$t_{PD}$	Propagation Delay CLKA or CLKB to Q0-9	280	400	530	ps	Differential
Clock input pair CLKB, CLKB (HSTL differential signals)						
$V_{DIF}$	Differential input voltage <sup>e</sup> (peak-to-peak) <sup>e</sup>	0.4		1.0	V	
$V_X$	Differential input crosspoint voltage <sup>f</sup>	$V_{EE} + 0.68$		$V_{EE} + 0.9$	V	
$f_{CLK}$	Input Frequency			2.7	GHz	Differential
$t_{PD}$	Propagation Delay CLKB to Q0-9	280	400	530	ps	Differential
ECL clock outputs (Q0-9, Q0-9)						
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)					
	$f_O < 300$ MHz	0.45	0.72	0.95	V	
	$f_O < 1.5$ GHz	0.3	0.55	0.95	V	
	$f_O < 2.7$ GHz	TBD	0.37	0.95	V	
$t_{sk(O)}$	Output-to-output skew			35	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			250	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter		TBD			
$t_{sk(P)}$	Output Pulse skew <sup>g</sup>			75	ps	
$t_r, t_f$	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%

- a. AC characteristics apply for parallel output termination of  $50 \Omega$  to  $V_{TT}$
- b.  $V_{PP}$  (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including  $t_{pd}$  and device-to-device skew
- c.  $V_{CMR}$  (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the  $V_{CMR}$  (AC) range and the input swing lies within the  $V_{PP}$  (AC) specification. Violation of  $V_{CMR}$  (AC) or  $V_{PP}$  (AC) impacts the device propagation delay, device and part-to-part skew
- d. The MC100ES6111 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
- e.  $V_{DIF}$  (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including  $t_{pd}$  and device-to-device skew.
- f.  $V_X$  (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the  $V_X$  (AC) range and the input swing lies within the  $V_{DIF}$  (AC) specification. Violation of  $V_X$  (AC) or  $V_{DIF}$  (AC) impacts the device propagation delay, device and part-to-part skew
- g. Output pulse skew is the absolute difference of the propagation delay times:  $|t_{PLH} - t_{PHL}|$ .



**Figure 1. MC100ES6111 AC test reference**

## APPLICATIONS INFORMATION

### Understanding the junction temperature range of the MC100ES6111

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6111, the MC100ES6111 is specified, characterized and tested for the junction temperature range of  $T_J=0^{\circ}\text{C}$  to  $+110^{\circ}\text{C}$ . Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of  $54.4^{\circ}\text{C/W}$  (2s2p board, 200 ft/min airflow, see table 4) and a typical power consumption of 610 mW (all outputs terminated 50 ohms to  $V_{TT}$ ,  $V_{CC}=3.3\text{V}$ , frequency independent), the junction temperature of the MC100ES6111 is approximately  $T_A + 33^{\circ}\text{C}$ , and the minimum ambient temperature in this example case calculates to  $-33^{\circ}\text{C}$  (the maximum ambient temperature is  $77^{\circ}\text{C}$ . See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6111 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6111 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

**Table 8: Ambient temperature ranges ( $P_{tot} = 610\text{ mW}$ )**

$R_{thja}$ (2s2p board)		$T_{A, \text{min}}$	$T_{A, \text{max}}$
Natural convection	$59.0^{\circ}\text{C/W}$	$-36^{\circ}\text{C}$	$74^{\circ}\text{C}$
100 ft/min	$54.4^{\circ}\text{C/W}$	$-33^{\circ}\text{C}$	$77^{\circ}\text{C}$
200 ft/min	$52.5^{\circ}\text{C/W}$	$-32^{\circ}\text{C}$	$78^{\circ}\text{C}$
400 ft/min	$50.4^{\circ}\text{C/W}$	$-30^{\circ}\text{C}$	$79^{\circ}\text{C}$
800 ft/min	$47.8^{\circ}\text{C/W}$	$-29^{\circ}\text{C}$	$81^{\circ}\text{C}$

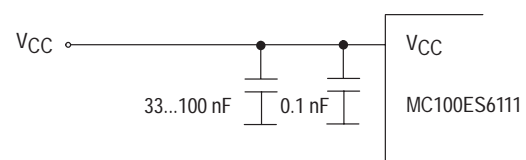
a. The MC100ES6111 device function is guaranteed from  $T_A=-40^{\circ}\text{C}$  to  $T_J=110^{\circ}\text{C}$

### Maintaining Lowest Device Skew

The MC100ES6111 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

### Power Supply Bypassing

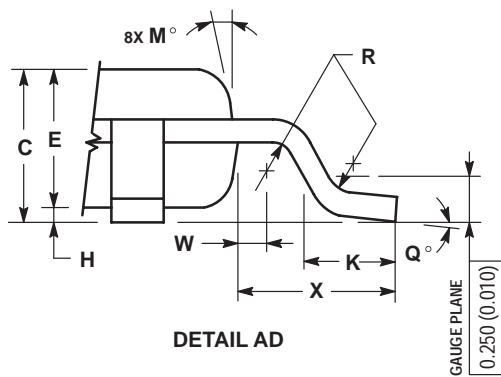
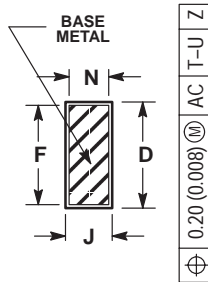
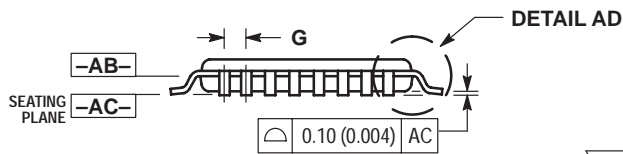
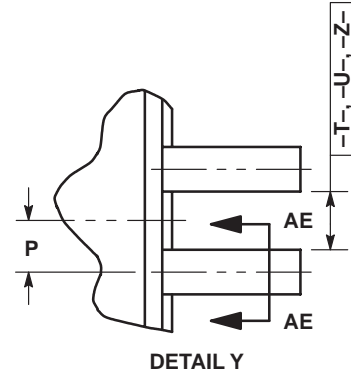
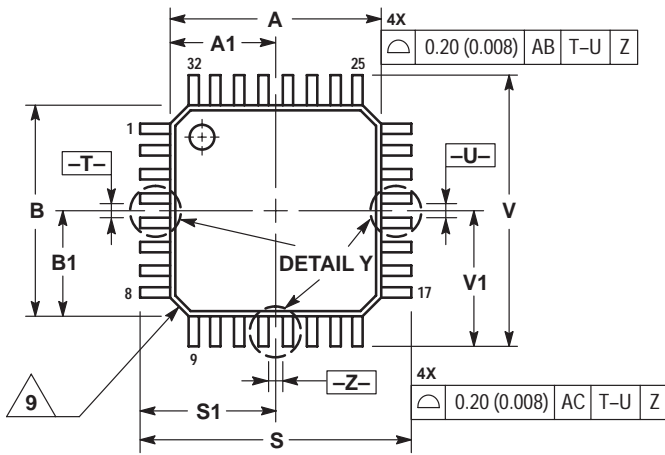
The MC100ES6111 is a mixed analog/digital product. The differential architecture of the MC100ES6111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all  $V_{CC}$  pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.



**Figure 2.  $V_{CC}$  Power Supply Bypass**

OUTLINE DIMENSIONS

FA SUFFIX  
LQFP PACKAGE  
CASE 873A-02  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
  8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC	0.276 BSC		
A1	3.500 BSC	0.138 BSC		
B	7.000 BSC	0.276 BSC		
B1	3.500 BSC	0.138 BSC		
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC	0.031 BSC		
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF	12° REF		
N	0.090	0.160	0.004	0.006
P	0.400 BSC	0.016 BSC		
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC	0.354 BSC		
S1	4.500 BSC	0.177 BSC		
V	9.000 BSC	0.354 BSC		
V1	4.500 BSC	0.177 BSC		
W	0.200 REF	0.008 REF		
X	1.000 REF	0.039 REF		



## NOTES

## NOTES

## NOTES

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