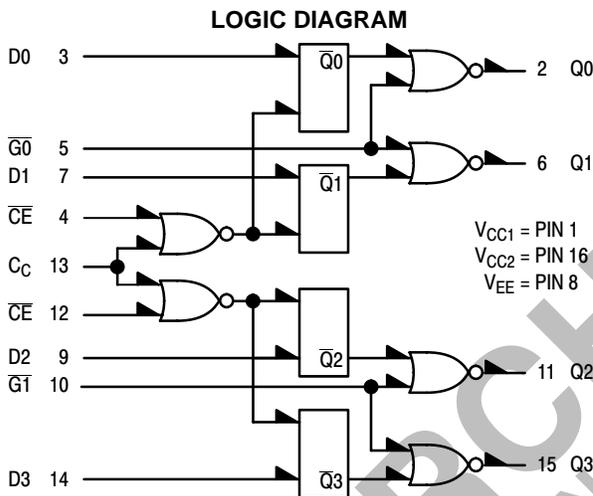


MC10153

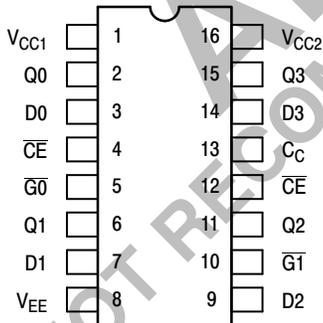
Quad Latch

The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

- $P_D = 310 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 4.0 \text{ ns typ}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

TRUTH TABLE

\bar{G}	C	D	Q_{n+1}
H	X	X	L
L	H	X	Q_n
L	L	L	L
L	L	H	H

$$C = C_c + \bar{C}\bar{E}$$



ON Semiconductor

<http://onsemi.com>

MARKING DIAGRAMS



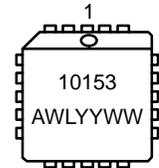
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

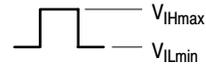
Device	Package	Shipping
MC10153L	CDIP-16	25 Units / Rail
MC10153P	PDIP-16	25 Units / Rail
MC10153FN	PLCC-20	46 Units / Rail

MC10153

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit		
			-30°C		+25°C			+85°C			
			Min	Max	Min	Typ	Max	Min		Max	
Power Supply Drain Current	I_E	8		83			75		83	mAdc	
Input Current	I_{inH}	3		390			245		245	μ Adc	
		4		390			245		245		
5			560			350		350			
13			460			290		290			
	I_{inL}	3	0.5		0.5			0.3		μ Adc	
Output Voltage Logic 1	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		
Output Voltage Logic 0	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		
Threshold Voltage Logic 1	V_{OHA}	2	-1.080		-0.980			-0.910		Vdc	
		2	-1.080		-0.980			-0.910			
		2	-1.080		-0.980			-0.910			
		2†	-1.080		-0.980			-0.910			
		2‡	-1.080		-0.980			-0.910			
		2‡	-1.080		-0.980			-0.910			
		2	-1.080		-0.980			-0.910			
		2	-1.080		-0.980			-0.910			
Threshold Voltage Logic 0	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc	
		2		-1.655			-1.630		-1.595		
		2		-1.655			-1.630		-1.595		
		2†		-1.655			-1.630		-1.595		
		2‡		-1.655			-1.630		-1.595		
		2‡		-1.655			-1.630		-1.595		
Switching Times (50Ω Load)	Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns
		t_{4-2+}	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2	
		t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4	
		t_{setup}	3	2.5		2.5	0.7		2.5		
		t_{hold}	3	1.5		1.5	0.7		1.5		
	Rise Time (20 to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	
	Fall Time (20 to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8	

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

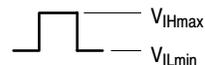
* Latch set to zero state before test.

MC10153

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}	
@ Test Temperature								
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2	
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2	
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}	
Power Supply Drain Current	I _E	8		13			8	1, 16
Input Current	I _{inH}	3	3				8	1, 16
		4	4				8	1, 16
		5	5				8	1, 16
		13	13				8	1, 16
	I _{inL}	3		3			8	1, 16
Output Voltage	Logic 1	V _{OH}	2	3	4		8	1, 16
			2	3	13		8	1, 16
Output Voltage	Logic 0	V _{OL}	2		3,13		8	1, 16
			2	3,5	13		8	1, 16
			2		3,4		8	1, 16
Threshold Voltage	Logic 1	V _{OHA}	2	3	4	5	8	1, 16
			2		4	3	8	1, 16
			2	3	4		8	1, 16
			2†	3			8	1, 16
			2‡				8	1, 16
			2‡				8	1, 16
			2	3		4	8	1, 16
			2	3		13	8	1, 16
Threshold Voltage	Logic 0	V _{OLA}	2	3	4	5	8	1, 16
			2		4		8	1, 16
			2		4	3	8	1, 16
			2		4		8	1, 16
			2†				8	1, 16
			2‡	3			8	1, 16
			2‡	3		13	8	1, 16
Switching Times (50Ω Load)			+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₃₊₂₊ t ₄₋₂₊ t ₅₋₂₊ t _{setup} t _{hold}	2			3	2	8	1, 16
		2		3*	4	2	8	1, 16
		2			5	2	8	1, 16
		3			3	2	8	1, 16
		3			3	2	8	1, 16
Rise Time (20 to 80%)	t ₂₊	2			3	2	8	1, 16
Fall Time (20 to 80%)	t ₂₋	2			3	2	8	1, 16

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4)



‡ Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

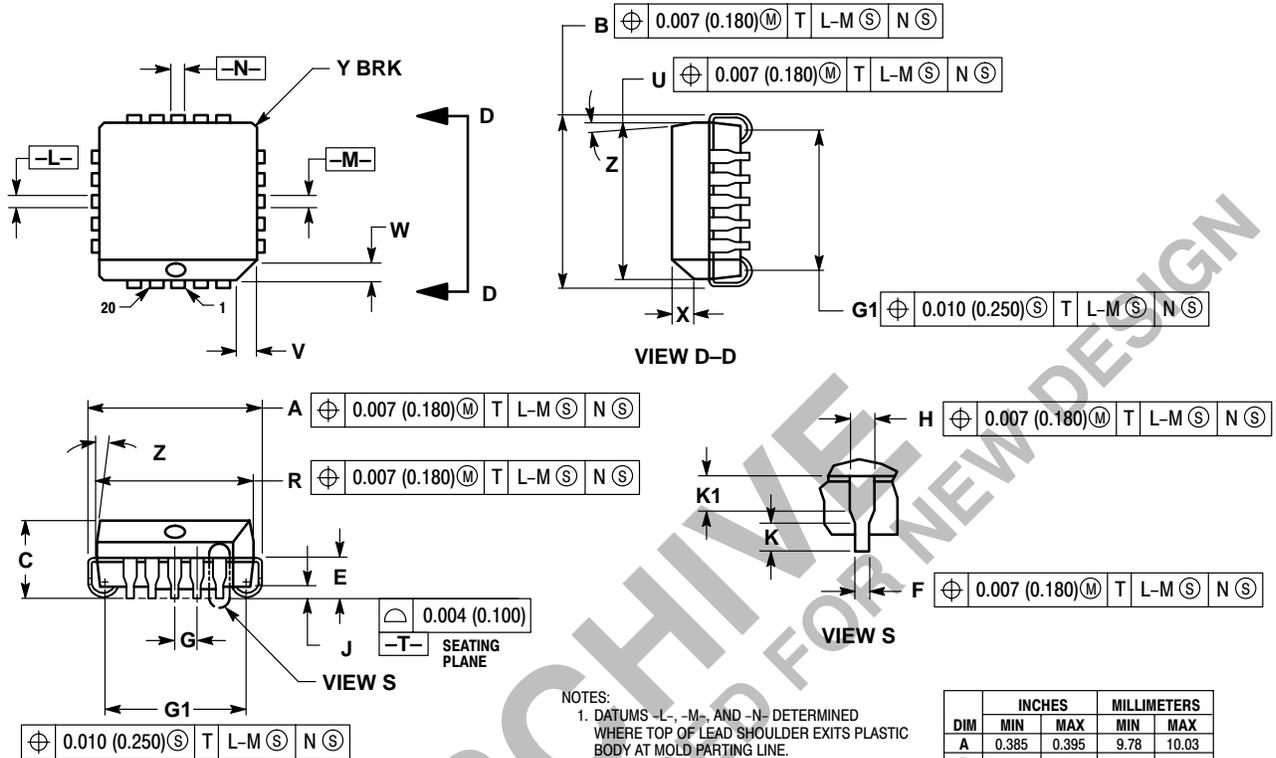
* Latch set to zero state before test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10153

PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



NOTES:

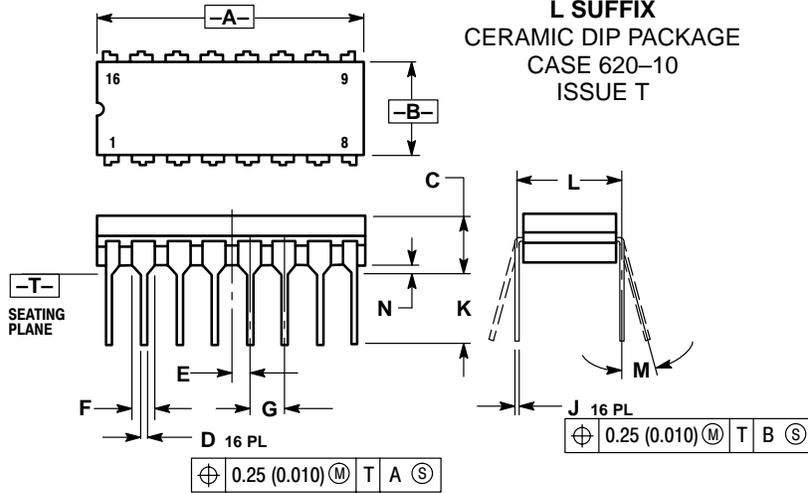
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10153

PACKAGE DIMENSIONS

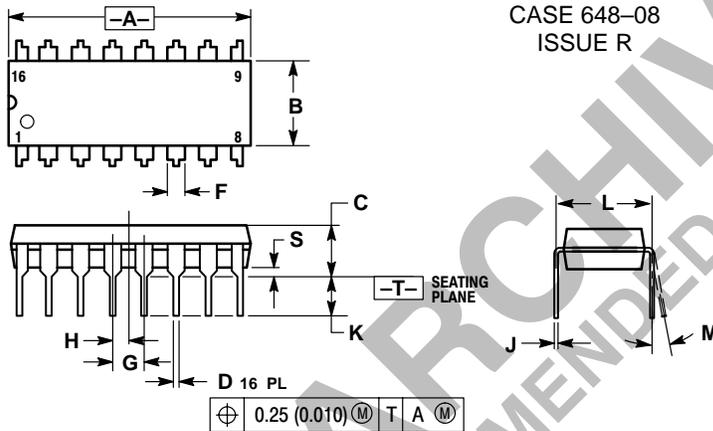
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

Notes

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DEVICE NOT RECOMMENDED FOR NEW DESIGN

Notes

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

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RECOMMENDED FOR NEW DESIGN

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