# **5 V ECL 1:4 Clock Distribution Chip**

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu F$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable  $(\overline{\text{EN}})$  is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The 100 series contains temperature compensation.

#### **Features**

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- PECL Mode Operating Range:
  - $V_{CC} = 4.2 \text{ V}$  to 5.7 V with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
  - $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V}$  to -5.7 V
- Internal Input Pulldown Resistors on CLKs, SCLK, SEL, and EN.
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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SOIC-16 D SUFFIX CASE 751B-05

#### **MARKING DIAGRAMS\***

A = Assembly Location

WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

\*For additional marking information, refer to Application Note <u>AND8002/D</u>.

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC10EL15DG	SOIC-16 (Pb-Free)	48 Units/Tube
MC10EL15DR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel
MC100EL15DG	SOIC-16 (Pb-Free)	48 Units/Tube
MC100EL15DR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

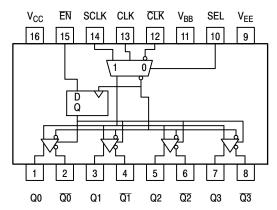


Figure 1. Logic Diagram and Pinout Assignment

**Table 1. PIN DESCRIPTION** 

PIN	FUNCTION
CLK, CLK	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
EN	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0-3}, \overline{Q_{0-3}}$	ECL Diff Clock Outputs
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

**Table 2. FUNCTION TABLE** 

CLK*	SCLK*	SEL*	EN*	Q
L	X	L	L	L
H	X	L	L	
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L(1)

**Table 3. ATTRIBUTES** 

Characteristics	Value
Internal Input Pulldown Resistor	75 KΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 1 kV > 100 V 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	103
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

<sup>1.</sup> For additional information, see Application Note AND8003/D.

<sup>\*</sup>Pins will default low when left open.

1. On next negative transition of CLK or SCLK

**Table 4. MAXIMUM RATINGS** 

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8	V
l <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	$\begin{array}{c} V_I \leq V_{CC} \\ V_I \geq V_{EE} \end{array}$	6 -6	V
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θЈА	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-16	130 75	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-16	33 to 36	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. 10EL SERIES PECL DC CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V}$ ;  $V_{EE} = 0.0 \text{ V}$  (Note 1))

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		25	35		25	35		25	35	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
$V_{BB}$	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.5		4.6	2.5		4.6	2.5		4.6	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.3			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.06 V / -0.5 V.
   Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> 2.0 V.
   V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP</sub>min and 1 V.

Table 6. 10EL SERIES NECL DC CHARACTERISTICS (V<sub>CC</sub> = 0 V; V<sub>EE</sub> = -5.0 V (Note 1))

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		25	35		25	35		25	35	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	-1230		-890	-1130		-810	-1060		-720	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	-1950		-1500	-1950		-1480	-1950		-1445	mV
$V_{BB}$	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.3			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V $_{CC}$ . V $_{EE}$  can vary +0.06 V / -0.5 V. 2. Outputs are terminated through a 50  $\Omega$  resistor to V $_{CC}$  2.0 V.
- 3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP</sub>min and 1 V.

Table 7. 100EL SERIES PECL DC CHARACTERISTICS (V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1))

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Min Typ Max			Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		25	35		25	35		25	38	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
$V_{BB}$	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.5		4.6	2.5		4.6	2.5		4.6	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
- 2. Outputs are terminated through a 50  $\Omega$  resistor to V<sub>CC</sub> 2.0 V.
- V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP</sub>min and 1 V.

Table 8. 100EL SERIES NECL DC CHARACTERISTICS (V<sub>CC</sub> = 0 V; V<sub>EE</sub> = -5.0 V (Note 1))

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Min Typ Max			Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		25	35		25	35		25	38	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V $_{CC}$ . V $_{EE}$  can vary +0.8 V / -0.5 V. 2. Outputs are terminated through a 50  $\Omega$  resistor to V $_{CC}$  2.0 V.
- V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP</sub>min and 1 V.

Table 9. AC CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V}$ ;  $V_{EE} = 0.0 \text{ V}$  or  $V_{CC} = 0 \text{ V}$ ;  $V_{EE} = -5.0 \text{ V}$  (Note 1))

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>MAX</sub>	Maximum Toggle Frequency					1.25					GHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	460 410 410		660 710 710	470 420 420		670 720 720	500 450 470		700 750 750	ps
tskew	Part-to-Part Skew Within-Device Skew (Note 2)			200 50			200 50			200 50	ps
t <sub>JITTER</sub>	Random Clock Jitter (RMS)					2.6					ps
t <sub>S</sub>	Setup Time EN	150			150			150			ps
t <sub>H</sub>	Hold Time EN	400			400			400			ps
V <sub>PP</sub>	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	325		575	325		575	325		575	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. 10 Series: V<sub>EE</sub> can vary +0.06 V / -0.5 V. 100 Series: VEE can vary +0.8 V / -0.5 V.
- 2. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
- 3. V<sub>PP</sub>(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40.

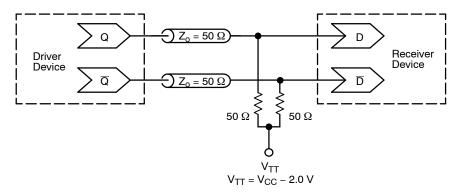


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> – Termination of ECL Logic Devices.)

### **Resource Reference of Application Notes**

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS ™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

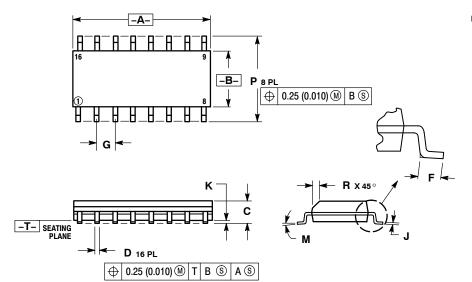
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

## **PACKAGE DIMENSIONS**

# SOIC-16 CASE 751B-05 ISSUE K



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MALL I IN	METERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α	9.80	10.00	0.386	0.393		
В	3.80	4.00	0.150	0.157		
C	1.35	1.75	0.054	0.068		
D	0.35	0.49	0.014	0.019		
F	0.40	1.25	0.016	0.049		
G	1.27	BSC	0.050 BSC			
J	0.19	0.25	0.008	0.009		
K	0.10	0.25	0.004	0.009		
M	0°	7°	0°	7°		
Р	5.80	6.20	0.229	0.244		
R	0.25	0.50	0.010	0.010		

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8. COLLECTOR #2 8. CATHODE 8. COLLECTOR, #2 8. COLLECTOR, #4 9. BASE, #3 10. EMITTER 10. ANODE 10. BASE, #3 11. BASE, #3 11. ANODE 13. COLLECTOR, #4 13. BASE, #3 11. ANODE 15. COMMON DRAIN (OUTPUT) 16. DRAIN, #4 7. CATHODE 2. COMMON DRAIN (OUTPUT) 17. GATE, #3 1. ANODE 14. ANODE 15. COMMON DRAIN (OUTPUT) 17. GATE, #3 11. ANODE 16. COMMON DRAIN (OUTPUT) 18. GATE, #4 9. ANODE 17. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 12. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 14. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE, #4 9. ANODE 15. COMMON DRAIN (OUTPUT) 19. GATE,	7									16X 1.12 < ➤
9. BASE 9. CATHODE 9. COLLECTOR,#3 9. BASE,#3 10. EMITTER,#4 11. NO CONNECTION 11. NO CONNECTION 11. NO CONNECTION 11. SUPPLY 11. NO CONNECTION 11. NO CONNECTION 11. EMITTER,#3 11. BASE,#3 11. BASE,	8									<u> </u>
10. EMITTER 10. ANODE 10. BASE,#3 10. EMITTER,#4 11. NO CONNECTION 11. NO CONNECTION 11. EMITTER,#3 11. BASE,#3 12. EMITTER,#3 12. EMITTER,#3 13. BASE 13. CATHODE 12. COLLECTOR,#3 12. EMITTER,#3 16X 14. COLLECTOR 14. NO CONNECTION 14. BASE,#4 14. EMITTER,#2 15. EMITTER 15. ANODE 15. EMITTER,#4 15. BASE,#1 16. COLLECTOR 16. CATHODE 16. COLLECTOR,#4 16. EMITTER,#1 16. EMITTER,#1 17. CATHODE 17. CATHODE 18. STYLE 5: STYLE 6: STYLE 7: PIN 1. DRAIN,#1 2. CATHODE 2. COMMON DRAIN (OUTPUT) 2. DRAIN,#1 2. CATHODE 2. COMMON DRAIN (OUTPUT) 3. DRAIN,#2 3. CATHODE 3. COMMON DRAIN (OUTPUT) 4. DRAIN,#2 4. CATHODE 4. GATE P.CH 5. DRAIN,#3 5. CATHODE 5. COMMON DRAIN (OUTPUT) 6. DRAIN,#3 6. CATHODE 6. COMMON DRAIN (OUTPUT) 7. DRAIN,#4 7. CATHODE 7. COMMON DRAIN (OUTPUT) 8. DRAIN,#4 8. CATHODE 8. SOURCE P-CH 9. GATE,#4 9. ANODE 9. SOURCE P-CH 11. GATE,#3 11. ANODE 10. COMMON DRAIN (OUTPUT) 11. GATE,#3 11. ANODE 11. COMMON DRAIN (OUTPUT) 12. SOURCE,#4 10. ANODE 12. COMMON DRAIN (OUTPUT) 13. GATE,#3 11. ANODE 12. COMMON DRAIN (OUTPUT) 14. SOURCE,#4 10. ANODE 12. COMMON DRAIN (OUTPUT) 15. GATE,#3 11. ANODE 13. GATE N-CH 14. SOURCE,#2 14. ANODE 15. COMMON DRAIN (OUTPUT) 15. GATE,#1 15. ANODE 15. COMMON DRAIN (OUTPUT) 16. GATE,#1 15. ANODE 15. COMMON DRAIN (OUTPUT) 17.									1	16 🗔
11. NO CONNECTION 12. EMITTER 12. CATHODE 12. COLLECTOR, #3 13. BASE 13. CATHODE 13. COLLECTOR, #4 14. COLLECTOR 14. NO CONNECTION 14. NO CONNECTION 15. EMITTER 15. ANODE 15. EMITTER, #4 16. COLLECTOR 16. CATHODE 17. CATHODE 18. CATHODE 19. CATHODE 19. SOURCE N-CH 19. DRAIN, DYE #1 19. CATHODE 19. CATHODE 19. CATHODE 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #2 10. DRAIN, #2 11. DRAIN, #3 11. DRAIN, #3 12. EMITTER, #3 14. EMITTER, #3 15. BASE, #3 16. CATHODE 16. COLLECTOR, #4 16. EMITTER, #1 16. EMITTER, #1 17. CATHODE 18. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #3 10. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #3 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #3 10. CATHODE 10. COMMON DRAIN (OUTPUT) 11. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT) 12. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 11. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT) 12. SOURCE, #8 12. ANODE 13. GATE, #2 14. ANODE 15. COMMON DRAIN (OUTPUT) 16. GATE, #1 17. ANODE 18. COMMON DRAIN (OUTPUT) 19. SOURCE, #8 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. COMMON DRAIN (OUTPUT) 19. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT) 11. GATE, #3 11. ANODE 12. COMMON DRAIN (OUTPUT) 13. GATE, #2 14. ANODE 15. COMMON DRAIN (OUTPUT) 16. GATE, #1 17. ANODE 18. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. ANODE 19. COMMON DRAIN (OUTPUT) 19. GATE, #1 19. CATHODE 19. CA									<b>↓</b>	'
12. EMITTER 12. CATHODE 12. COLLECTOR, #3 12. EMITTER, #3 16X 13. BASE 13. CATHODE 13. COLLECTOR, #4 13. BASE, #2 0.58 13. CATHODE 14. NO CONNECTION 14. BASE, #4 14. EMITTER, #2 15. EMITTER 15. ANODE 15. EMITTER, #4 15. BASE, #1 16. COLLECTOR #4 16. CATHODE 16. COLLECTOR, #4 16. EMITTER, #1 15. BASE, #1 16. COLLECTOR #4 16. EMITTER, #1 16. EMITTER, #1 17. CATHODE 16. COMMON DRAIN (OUTPUT) 17. DRAIN, #2 17. CATHODE 17. COMMON DRAIN (OUTPUT) 18. DRAIN, #3 18. CATHODE 18. COMMON DRAIN (OUTPUT) 18. DRAIN, #4 7. CATHODE 18. COMMON DRAIN (OUTPUT) 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. CATHODE 19. SOURCE P-CH 19. SOURCE, #4 10. ANODE 19. SOURCE P-CH 19. SOURCE P-CH 19. SOURCE, #4 10. ANODE 19. SOURCE P-CH 19. SOURCE, #4 10. ANODE 19. SOURCE P-CH 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 19. SOURCE #5 and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference 19. SOURCE #6 19. SOUR									<del>'</del>	
13. BASE 13. CATHODE 13. COLLECTOR, #4 13. BASE, #2 14. NO CONNECTION 14. NO CONNECTION 14. BASE, #4 14. EMITTER, #2 15. BASE, #4 15. BASE, #1 14. EMITTER, #2 15. BASE, #1 15. BASE, #1 16. COLLECTOR 16. CATHODE 16. COLLECTOR, #4 16. EMITTER, #1 16. EMITTER, #1 17. EMITTER, #1 17. EMITTER, #1 17. EMITTER, #1 18. EMITTER, #1 18								EMITTED #0	<b>-</b>	
14. COLLECTOR 15. EMITTER 15. ANODE 15. EMITTER, #4 15. EMITTER, #4 16. COLLECTOR 16. CATHODE 16. COLLECTOR, #4 16. COLLECTOR 16. CATHODE 16. COLLECTOR, #4 16. EMITTER, #1 16. EMITTER, #1 16. EMITTER, #1 16. EMITTER, #1 17. DRAIN, DYE #1 18. DRAIN, DYE #1 19. DRAIN, DYE #1 19. DRAIN, #1 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #2 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #3 19. CATHODE 19. COMMON DRAIN (OUTPUT) 19. DRAIN, #3 10. SOURCE, #4 10. SOURCE, #4 10. SOURCE, #4 10. SOURCE, #4 10. ANODE 11. COMMON DRAIN (OUTPUT) 11. GATE, #3 11. ANODE 12. COMMON DRAIN (OUTPUT) 13. GATE, #3 14. SOURCE, #3 15. EMITTER, #2 15. BASE, #1 16. EMITTER, #2 16. EM								10/	Ĵ ┌──	· —
16. COLLECTOR 16. CATHODE 16. COLLECTOR, #4 16. EMITTER, #1  STYLE 5: STYLE 6: STYLE 7:  PIN 1. DRAIN, DYE #1 PIN 1. CATHODE PIN 1. SOURCE N-CH  2. DRAIN, #1 2. CATHODE 2. COMMON DRAIN (OUTPUT)  3. DRAIN, #2 3. CATHODE 3. COMMON DRAIN (OUTPUT)  4. DRAIN, #2 4. CATHODE 4. GATE P-CH  5. DRAIN, #3 5. CATHODE 5. COMMON DRAIN (OUTPUT)  6. DRAIN, #3 6. CATHODE 6. COMMON DRAIN (OUTPUT)  7. DRAIN, #4 7. CATHODE 7. COMMON DRAIN (OUTPUT)  8. DRAIN, #4 8. CATHODE 8. SOURCE P-CH  9. GATE, #4 9. ANODE 9. SOURCE P-CH  10. SOURCE, #4 10. ANODE 10. COMMON DRAIN (OUTPUT)  11. GATE, #3 11. ANODE 11. COMMON DRAIN (OUTPUT)  12. SOURCE, #3 12. ANODE 12. COMMON DRAIN (OUTPUT)  13. GATE, #2 13. ANODE 14. COMMON DRAIN (OUTPUT)  14. SOURCE, #2 14. ANODE 15. COMMON DRAIN (OUTPUT)  15. GATE, #1 15. ANODE 15. COMMON DRAIN (OUTPUT)  16. EMITTER, #1  11. CATHODE 10. EMITTER, #1  11. ANODE 11. COMMON DRAIN (OUTPUT)  11. SOURCE, #3  12. ANODE 12. COMMON DRAIN (OUTPUT)  13. GATE, #2  14. SOURCE, #2  15. GATE, #1  15. GATE, #1  15. ANODE 15. COMMON DRAIN (OUTPUT)  16. EMITTER, #1  17. CATHODE 17. CATHODE 17. COMMON DRAIN (OUTPUT)  18. EMITTER, #1  19. CATHODE 18. EMITTER, #1  11. SOURCE, #2  12. CATHODE 18. SOURCE #2  13. ANODE 14. COMMON DRAIN (OUTPUT)  14. COMMON DRAIN (OUTPUT)  15. GATE, #1  16. EMITTER, #1  17. CATHODE 18. EMITTER, #1  18. SOURCE #2  19. CATHODE 18. SOURCE #4  19. CATHODE 18. SOURCE #4  19. CATHODE 18. SOURCE #1  10. CATHODE 18. SOURCE #1  11. CATHODE 18. SOURCE #1  12. COMMON DRAIN (OUTPUT)  13. GATE, #2  14. SOURCE, #2  15. CATHODE 18. SOURCE #1  16. COMMON DRAIN (OUTPUT)  17. CATHODE 18. SOURCE #1  18. SOURCE #1  19. CATHODE 18. SOURCE #1  19. CATHODE 18. SOURCE #1  10. CATHODE 18. SOURCE #1  11. CATHODE 18. SOURCE #1  1										1
STYLE 5:   STYLE 6:   STYLE 7:   PIN 1. DRAIN, DYE #1   PIN 1. CATHODE   PIN 1. SOURCE N-CH	15.	EMITTER			15.		15.	BASE, #1		
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