MC1544L
MC1444L

Advance Information

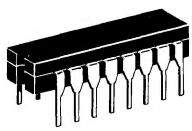
IDEAL FOR PLATED-WIRE, THIN-FILM AND OTHER HIGH-SPEED LOW-LEVEL SENSING APPLICATIONS

MC1544L/MC1444L features four input channels with decoded selection, two stages of gain employing capacitive coupling, and a MTTL compatible output gate. AC coupling reduces access times by eliminating the problems usually associated with input line offset voltages.

- Threshold Level – 1.0 mV typ
- Propagation Delay Time – 18 ns typ
- Decoded Input Channel Selection
- MTTL Compatible Inputs and Outputs
- Wired OR Output Capability
- DC Level Restore Gate on Capacitors Eliminates Repetition Rate Problems Common to ac-Coupled Circuits
- Output Strobe Capability

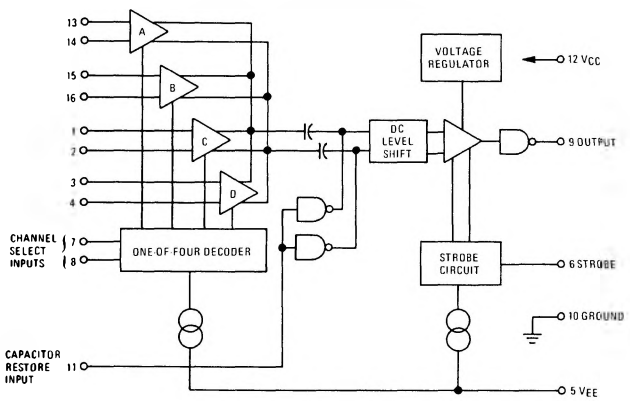
AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

FIGURE 1 – BLOCK DIAGRAM



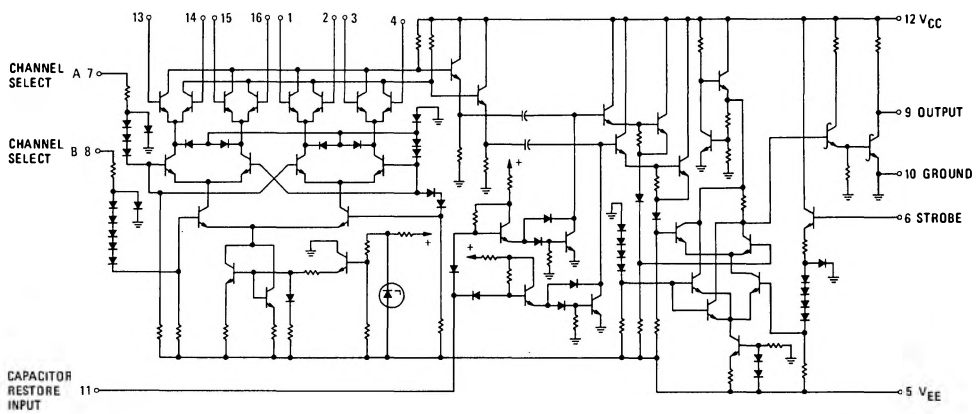
TRUTH TABLE		
PIN 7	PIN 8	CHANNEL SELECTED
HI	HI	A
LO	HI	B
HI	LO	C
LO	LO	D

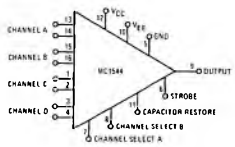
This is advance information and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −8.0	Vdc
Common-Mode Input Voltage	V_{CM^+} V_{CM^-}	+5.0 −6.0	Vdc
Differential-Mode Input Voltage	V_{DM^+} V_{DM^-}	+5.0 −6.0	Vdc
Capacitor Restore, Channel Select, and Strobe Input Voltage	V_{CR}, V_{CS}, V_S	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	1.0 6.7	W mW/°C
Operating Temperature Range MC1544L MC1444L	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

FIGURE 2 – CIRCUIT SCHEMATIC





ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

								TEST CURRENT/VOLTAGE VALUES															
								μA		mA		VOLTS											
								I_{CM}+	I_{CM}−	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}	
								200	−10	10	−0.4	0.8	2.0	0	3.5	4.75	5.0	5.25	−5.7	−6.0	−6.3	
								TEST CURRENT/VOLTAGES APPLIED TO PINS LISTED BELOW:														
CHARACTERISTIC		Symbol	Pin Under Test	Min	Typ	Max	Unit	I_1	I_2	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IL2}	V_{IH2}	V_{CCL}	V_{CC}	V_{CCH}	V_{EEL}	V_{EE}	V_{EEH}	GND
Input Threshold Voltage (Note 1)	MC1544L	V_{TH}	13	–	1.0	–	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
T_{low}* to T_{high}*	MC1444L		13	–	1.0	–	mV	–	–	–	–	–	–	–	–	–	12	–	–	5	–	10
Input Bias Current (Note 1)		I_b	13	–	20	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Input Offset Current		I_{io}	13, 14	–	1.0	–	μA	–	–	–	–	–	–	13, 14	7, 8	–	–	12	–	–	5	10
Channel Select Input Current (Note 2)	High Level	I_{CSH}	7	–	1.8	3.0	mA	–	–	–	–	–	–	–	7	–	–	12	–	–	5	10
	Low Level	I_{CSL}	7	–	0.6	1.0	mA	–	–	–	–	–	–	7	–	–	–	12	–	–	5	10
Capacitor Restore Input Current	High Level	I_{CRH}	11	–	0	10	μA	–	–	–	–	–	–	–	11	–	–	12	–	–	5	10
	Low Level	I_{CRL}	11	–	−2.5	−3.5	mA	–	–	–	–	–	–	11	–	–	–	12	–	–	5	10
Strobe Input Current	Low/High Level	I_S	6	–	40	200	μA	–	–	–	–	–	–	–	6	–	–	12	–	–	5	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	7	2.1	1.6	–	V	–	–	–	–	–	7	3, 8 13, 15	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	7	–	1.2	0.7	V	–	–	–	–	7	–	1, 8 13, 15	–	–	12	–	–	5	–	10
Channel Select Input Voltage (Note 3)	High Level	V_{CSH}	8	2.1	1.5	–	V	–	–	–	–	–	8	1, 3 7, 13	–	–	12	–	–	5	–	10
	Low Level	V_{CSL}	8	–	1.0	0.7	V	–	–	–	–	8	–	1, 7 13, 15	–	–	12	–	–	5	–	10
Capacitor Restore Input Voltage (Note 4)	High Level	V_{CRH}	11	2.0	1.5	–	V	–	–	–	–	–	11	–	6	–	12	–	–	5	–	10
	Low Level	V_{CRL}	11	–	1.5	0.8	V	–	–	–	–	11	–	–	6	–	12	–	–	5	–	10
Strobe Input Voltage (Note 4)	High Level	V_{SH}	6	2.0	1.5	–	V	–	–	–	–	–	6	11	–	–	12	–	–	5	–	10
	Low Level	V_{SL}	6	–	1.5	0.8	V	–	–	–	–	6	–	11	–	–	12	–	–	5	–	10
Output Voltage	High Level	V_{OH}	9	2.4	3.6	–	V	–	–	–	9	6	–	–	–	12	–	–	5	–	–	10
	Low Level	V_{OL}	9	–	0.4	0.5	V	–	–	9	–	–	–	–	–	12	–	–	–	–	–	10
Power Supply Currents	Positive	I_{CC}	12	15	22	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
	Negative	I_{EE}	5	15	20	30	mA	–	–	–	–	–	–	6, 13, 14	7, 8, 11	–	–	12	–	–	5	10
Common-Mode Range Voltage (Note 1)		V_{CM}+	13, 14	–	4.7	–	Vdc	13, 14	–	–	–	–	–	–	7, 8	–	12	–	–	5	–	10
		V_{CM}−	13, 14	–	−6.0	–	Vdc	13, 14	–	–	–	–	–	–	7, 8	–	12	–	–	5	–	10
Differential-Mode Range Voltage		V_{DM}	13	–	3.7	–	Vdc	13	–	–	–	–	–	14	7, 8	–	12	–	–	5	–	10

*MC1544 T_{low} = −55°C, T_{high} = +125°C. MC1444 T_{low} = 0°C, T_{high} = +75°C.

NOTES:
1. Only one input test is shown, other inputs are tested in the same manner and are selected according to the truth table in Figure 1.
2. Pin 8 is tested in the same manner.
3. This requirement is considered satisfied if the input bias currents of all unselected channels total less than 1.0 μA which guarantees that these channels are "off."
4. This requirement is evaluated during the ac threshold test (Figures 1, 2): A 10 mV signal (e_{in_1}) is applied to the input, V_{CRH} will result in V_{OH} at the output while V_{CRL} will allow normal operation.
5. This requirement is evaluated as in Note 4 except V_{SH} allows normal operation and V_{SL} causes V_{OH} at the output.

SWITCHING CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic		Symbol	Figure	Min	Typ	Max	Unit
Propagation Delay Time		t_{pd}− t_{pd}+	1, 5	– –	18 40	25 –	ns
Strobe to Input Lead Time		t_{si}	1, 5	–	10	–	ns
Strobe to Output Delay Time		t_{so}− t_{so}+	1, 6	– –	18 30	25 –	ns
Channel Select to Input Lead Time		t_{csi}	1, 5	–	15	–	ns
Channel Select to Output Delay Time		t_{cso}− t_{cso}+	1, 7	– –	25 40	– –	ns
Capacitor Restore to Input Lead Time		t_{cri}	1, 5	–	10	–	ns
Capacitor Restore Time (50 mV Offset)		t_{cr}	1, 8	–	15	–	ns
Common-Mode Recovery Time	e_{in_1} = +2.0 V e_{in_1} = −2.0 V	t_{CMR}+ t_{CRM}−	19	– –	50 50	– –	ns
Differential-Mode Recovery Time	e_{in_1} = +1.0 V e_{in_1} = −1.0 V	t_{DMR}+ t_{DMR}−	20	– –	65 65	– –	ns

FIGURE 3 – AC TEST CIRCUIT

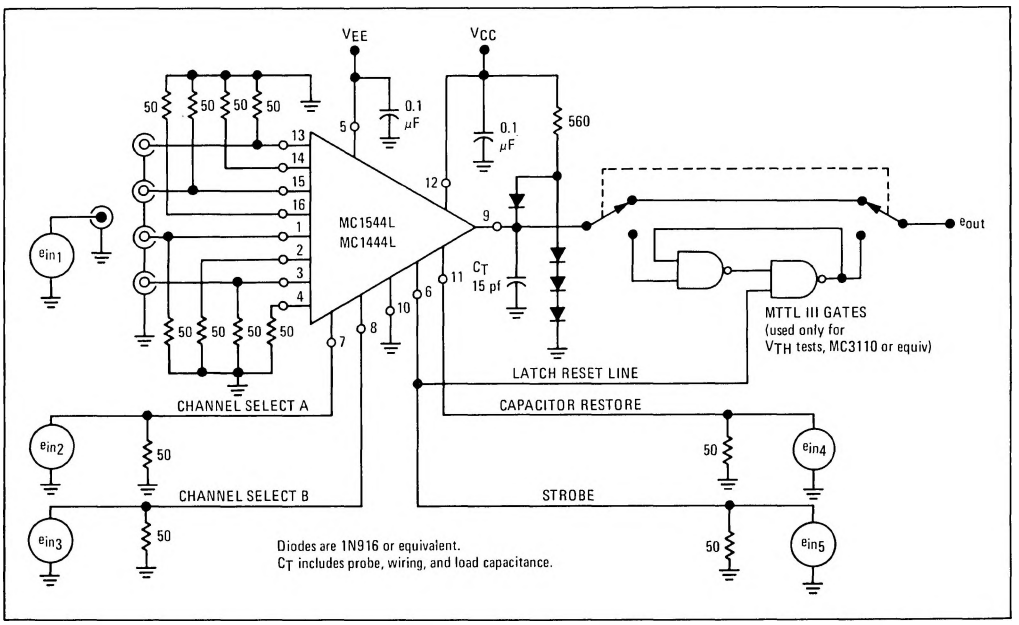


FIGURE 4 – THRESHOLD VOLTAGE TEST

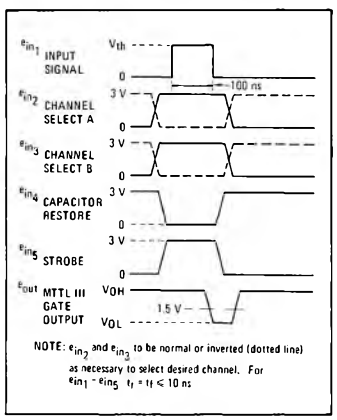


FIGURE 5 – t_{csi}, t_{cri}, t_{si}, t_{pd-}, t_{pd+}

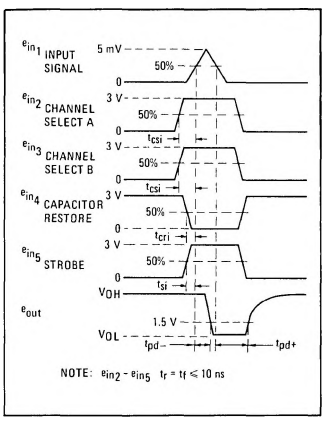


FIGURE 6 – t_{so-}, t_{so+}

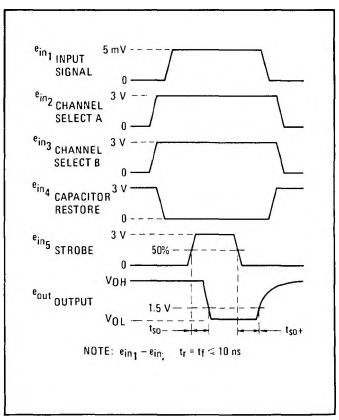
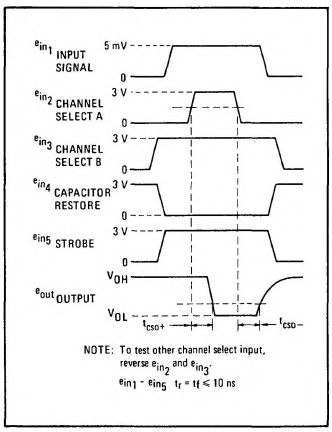
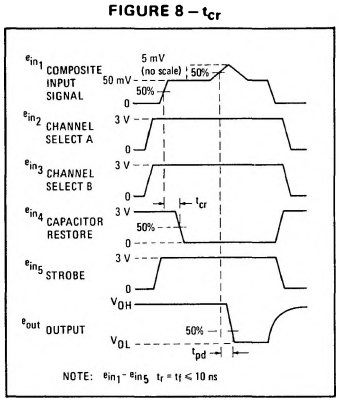


FIGURE 7 – t_{cso+}, t_{cso-}



NOTE: To test other channel select input, reverse e_{in_2} and e_{in_3}.
e_{in_1} - e_{in_5} $t_r = t_f \leq 10$ ns

FIGURE 8 – t_{cr}



NOTE: e_{in_1} - e_{in_5} $t_r = t_f \leq 10$ ns

DEFINITIONS

I_b	Input current to the base of any input transistor when the base of the other transistor of the differential pair is at the same voltage
I_{CC}	Positive power supply current
I_{CRH}	The current into the channel select input when the input is at a high-level of 3.5 volts
I_{CRL}	The current out of the capacitor restore input when the input is at a low-level of 0 volts
I_{CSH}	The input current to a channel select input when that input is at a high-level of 3.5 volts
I_{CSL}	The current into a channel select input when the input is at a low-level of 0 volts
I_{EE}	Negative power supply current
I_{io}	The difference between the base currents of any input differential pair of transistors when the base voltages are equal
I_{OH}	Output logic "1" state source current
I_{OL}	Output logic "0" state sink current
I_{SH}	The current into the strobe input when the input is at a high-level of 3.5 volts
I_{SL}	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 2 volt common-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 21
t_{cr}	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 8
t_{cri}	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{csi}	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
t_{cso+}	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
t_{cso-}	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 1 volt differential-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
t_{pd+}	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 5
t_{pd-}	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 5
t_{si}	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 5
t_{so+}	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the "1" level as shown in Figure 6
t_{so-}	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the "1" level as shown in Figure 6
V_{CC}	Positive power supply voltage
V_{CCH}	Maximum operating positive power supply voltage
V_{CCL}	Minimum operating positive power supply voltage
V_{CM^+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{CM^-}	The minimum common-mode input voltage that will not break down the amplifier
V_{CRH}	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
V_{CRL}	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
V_{CSH}	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{CSL}	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{DM}	The maximum differential-mode input voltage that will not saturate the amplifier
V_{EE}	Negative power supply voltage
V_{EEH}	Maximum operating negative power supply voltage
V_{EEL}	Minimum operating negative power supply voltage
V_{OH}	Logic "1" state output voltage
V_{OL}	Logic "0" state output voltage
V_{SH}	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
V_{SL}	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal (e_{in_1}) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 4

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 9 – THRESHOLD VOLTAGE versus TEMPERATURE

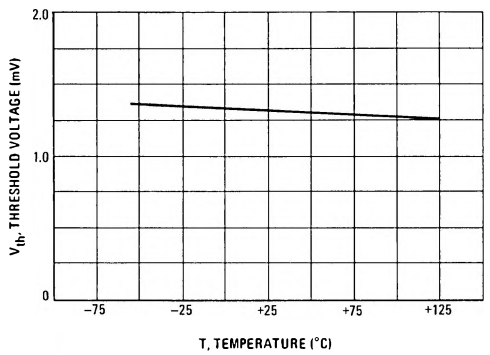


FIGURE 10 – THRESHOLD VOLTAGE versus POWER SUPPLIES

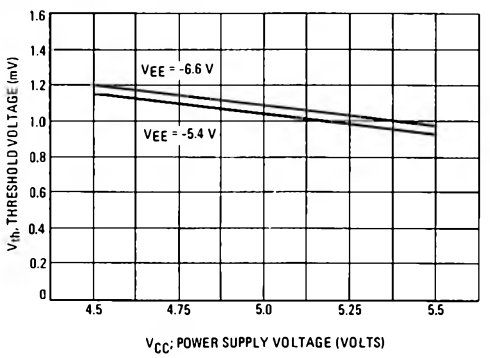


FIGURE 11 – THRESHOLD versus INPUT OFFSET VOLTAGE

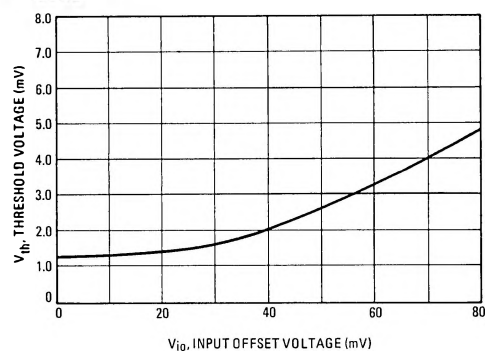


FIGURE 12 – THRESHOLD VOLTAGE versus PULSE WIDTH

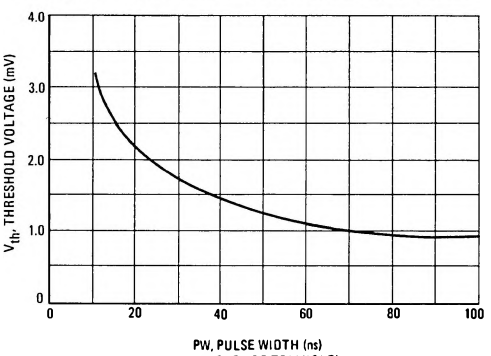


FIGURE 13 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

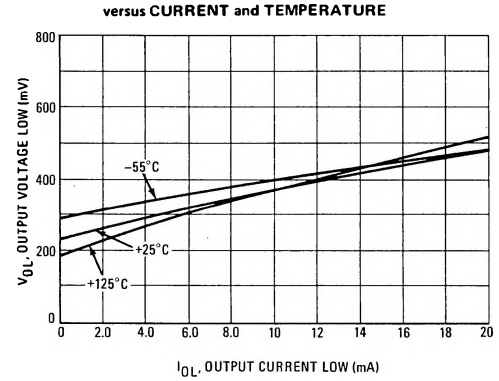
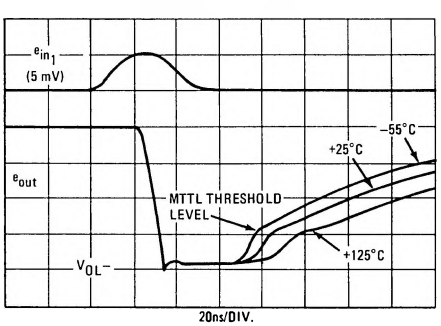


FIGURE 14 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figures 3 and 5)



TYPICAL CHARACTERISTICS (continued)

FIGURE 15 – INPUT IMPEDANCE versus FREQUENCY

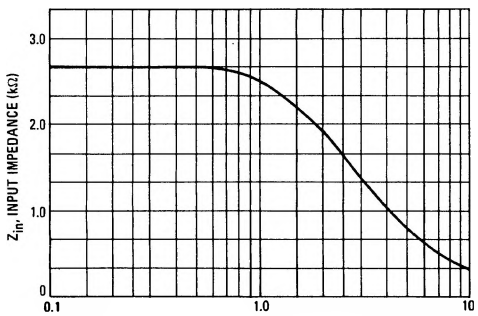


FIGURE 16 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

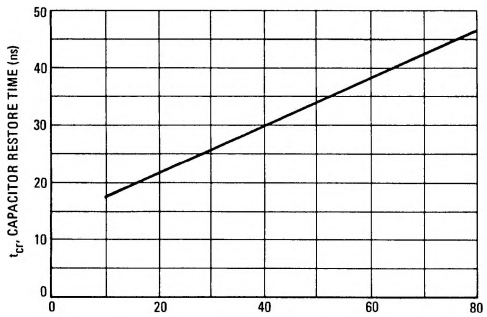


FIGURE 17 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

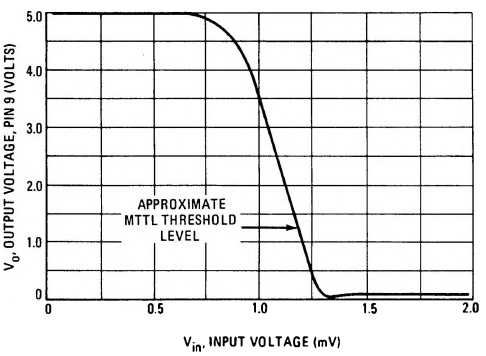


FIGURE 18 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

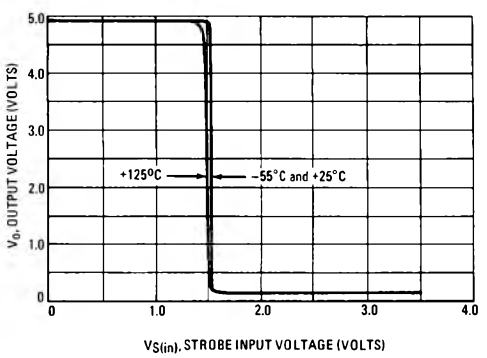


FIGURE 19 – CHANNEL SELECT A to OUTPUT TRANSFER CHARACTERISTICS

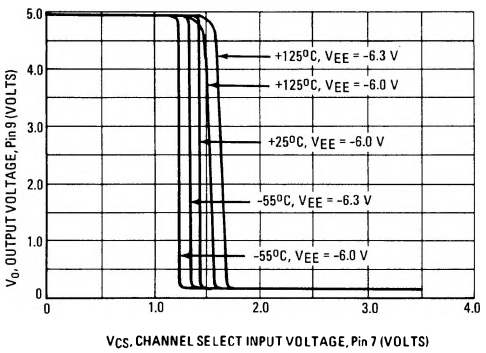


FIGURE 20 – CHANNEL SELECT B to OUTPUT TRANSFER CHARACTERISTICS

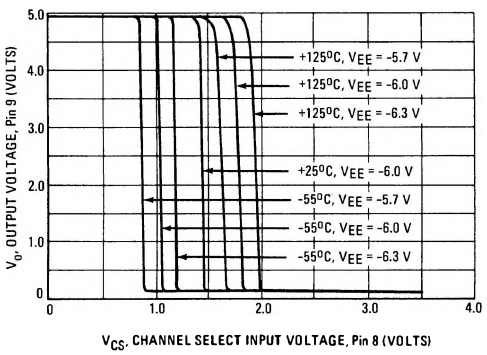


FIGURE 21 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.

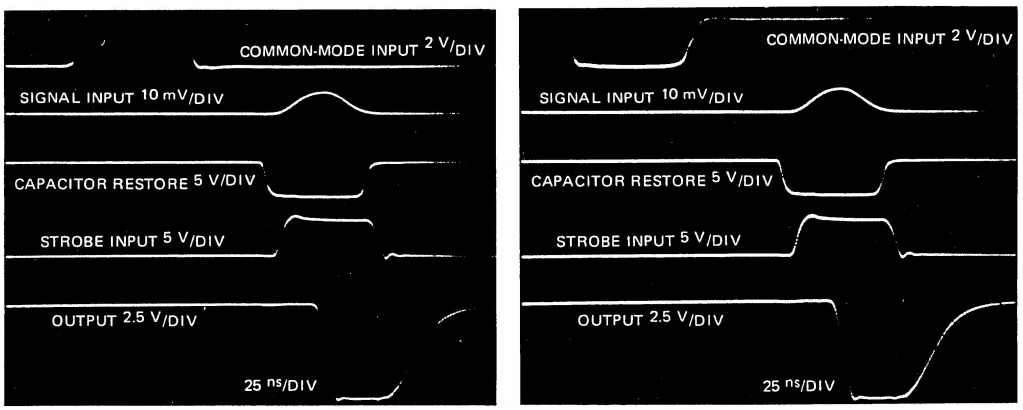


FIGURE 22 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only.