MC1546L
MC1446L

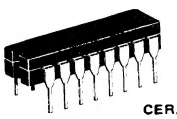
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

. . . a sense amplifier designed to convert positive or negative 3.0 mV signals from plated-wire memories to transistor-transistor logic levels (MTTL). The problems encountered with ac-coupled plated-wire sense amplifiers are eliminated with this direct-coupled sense amplifier.

- Positive or Negative 3.0 mV Signal to Any of Four Input Channels Produces a Logic 1 or 0 Output (MC1446 – Positive or Negative 4.0 mV).
- Low Input Offset Voltages Apply to All Four Channels – 0.5 mV typ
- Wired "OR" Capability at Amplifier Output Results in Fewer Associated Circuits
- 2 by 4 Internal Decoder Simplifies Channel Selection
- Fast Recovery Time from Overload Signals – 40 ns typ
- Good Isolation Between ON and OFF Channels
- Channel Select and Strobe Operate from Standard MTTL Levels

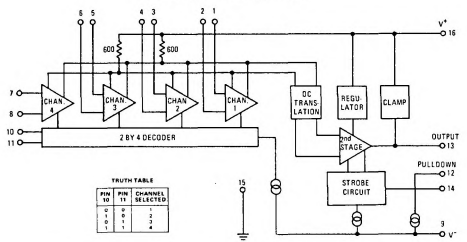
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

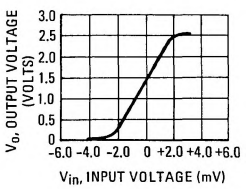


CERAMIC PACKAGE
CASE 620

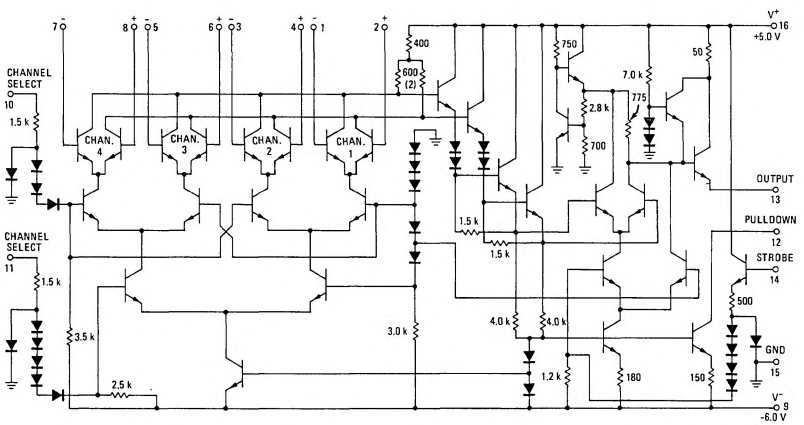
BLOCK DIAGRAM



TRANSFER CHARACTERISTICS



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V^+ V^-	+10 -10	Vdc
Differential Input Signal		V_{in}	±5.0	Volts
Common-Mode Input		CMV_{in}	±5.0	Volts
Output Current		I_{out}	25	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C		P_D	 575 3.85	 mW mW/°C
Operating Temperature Range	MC1546L MC1446L	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	MC1546L MC1446L	T_{stg}	-65 to +175 -55 to +125	°C

ELECTRICAL CHARACTERISTICS

(V^+ = +5.0 Vdc ±1%, V^- = -6.0 Vdc ±1%, T_A = +25°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1546L			MC1446L			Unit
			Min	Typ	Max	Min	Typ	Max	
Voltage Gain	1	A_V	–	600	–	–	600	–	–
Output Voltage Level MC1546, MC1446	2	V_o							Vdc
$T_A = T_{low}$* to T_{high}* e_{in} = 0, 0			0.8	1.4	2.0	0.4	1.4	2.4	
e_{in} = +3.0, +4.0 mV			2.0	–	–	2.0	–	–	
e_{in} = -3.0, -4.0 mV			–	–	0.4	–	–	0.4	
Input Bias Current	3	I_b	–	15	40	–	15	60	µA
Input Offset Current	3	I_{io}	–	0.1	2.0	–	0.1	4.0	µA
Channel Select Current	4								
High Level		I_{CH}	–	1.7	2.4	–	1.7	2.6	mA
Low Level		I_{CL}	–	0.5	0.9	–	0.5	1.0	
Channel Select Voltage	5								
High Level		V_{CH}	2.0	–	–	2.0	–	–	Volts
Low Level		V_{CL}	–	–	0.8	–	–	0.8	
Strobe Voltage	5								
High Level		V_{SH}	2.0	–	–	2.0	–	–	Volts
Low Level		V_{SL}	–	–	0.8	–	–	0.8	
Strobe Input Current	4	I_S	–	30	100	–	30	150	µA
Output Source Current	6	I_{o+}	5.0	8.0	–	4.0	8.0	–	mA
Output Sink Current	6	I_{o-}	-3.0	-4.0	–	-2.5	-4.0	–	mA
Positive Supply Current	6	I^+	–	19	25	–	19	27	mA
Negative Supply Current	6	I^-	–	-17	-22	–	-17	-24	mA
Input Common-Mode Voltage Range	7	$CMV_{(in)}$							
Channel Selected			–	+2.7	–	–	+2.7	–	Volts
			–	-1.0	–	–	-1.0	–	
Channels Not Selected			–	+2.7	–	–	+2.7	–	
			–	-6.0	–	–	-6.0	–	
Input Differential-Mode Voltage Range	7	$DMV_{(in)}$							Volts
Channel Selected			–	±0.5	–	–	±0.5	–	
Channels Not Selected			–	±2.0	–	–	±2.0	–	

*T_{low} = -55°C for MC1546, 0°C for MC1446; T_{high} = +125°C for MC1546, +75°C for MC1446

SWITCHING CHARACTERISTICS

Propagation Delay Time	8	t_{pd}	10	14	18	–	14	–	ns
Output Rise or Fall Time	8	t_r or t_f	–	30	–	–	30	–	ns
Strobe Delay Time	9	t_{dS}	–	14	18	–	14	–	ns
Strobe Width (min)	9	$t_{S(min)}$	–	20	–	–	20	–	ns
Channel Select Time	10	t_{Csel}	–	14	18	–	14	–	ns
Common-Mode Recovery Time (channel selected)	7	t_{CMR}	–	60	–	–	60	–	ns
Differential-Mode Recovery Time (channel selected)	8	t_{DMR}	–	40	–	–	40	–	ns

TEST CIRCUITS

FIGURE 1 – VOLTAGE GAIN

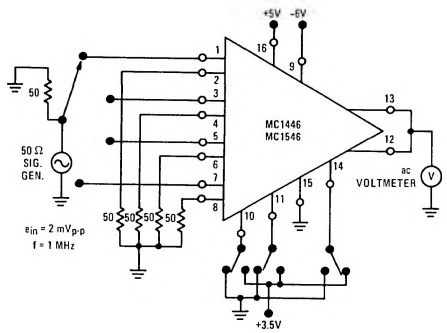


FIGURE 2 – OUTPUT DC LEVELS

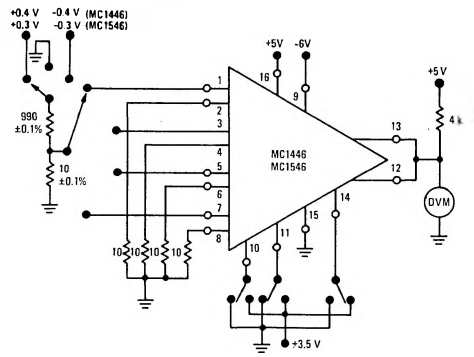


FIGURE 3 – INPUT CURRENTS

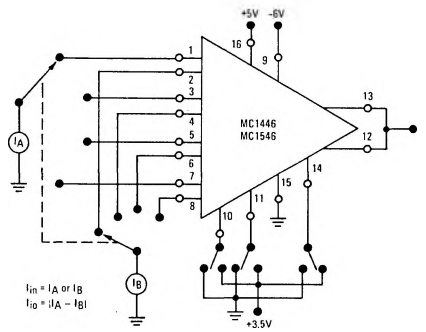


FIGURE 4 – CHANNEL SELECT AND STROBE INPUT CURRENTS

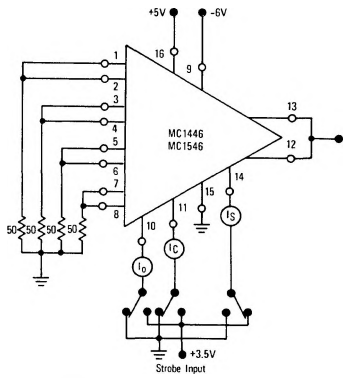


FIGURE 5 – CHANNEL SELECT TRANSFER CHARACTERISTICS

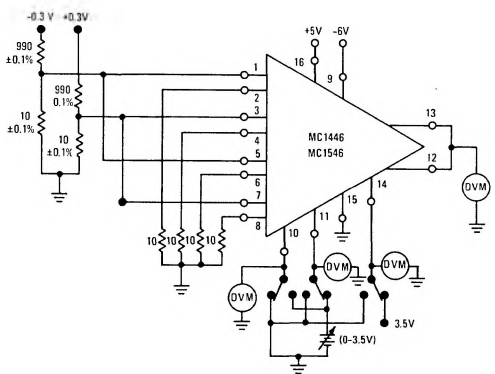


FIGURE 6 – OUTPUT CURRENTS

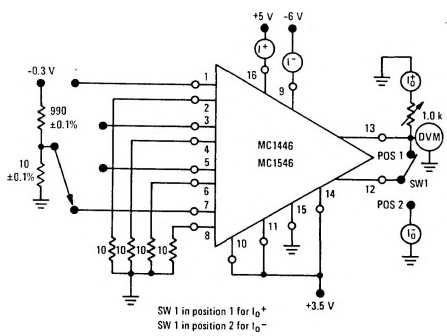


FIGURE 7 – INPUT COMMON-MODE CHARACTERISTICS

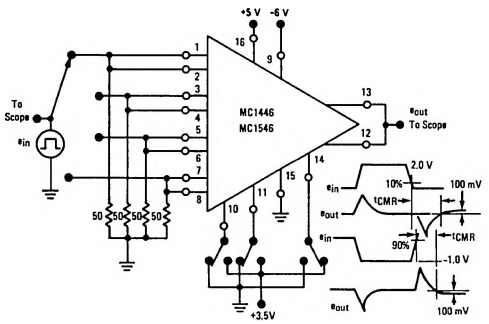


FIGURE 8 – CIRCUIT PROPAGATION DELAY, OUTPUT RISE AND FALL TIMES, AND DIFFERENTIAL-MODE RECOVERY TIME

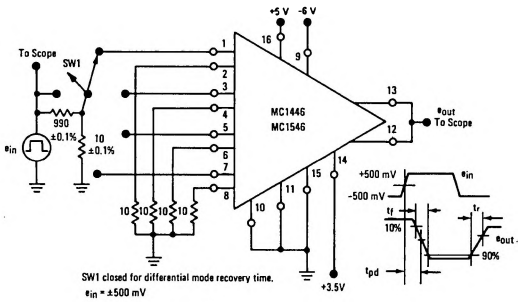


FIGURE 9 – STROBE CHARACTERISTICS

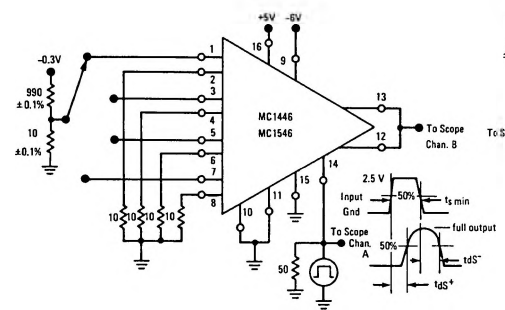
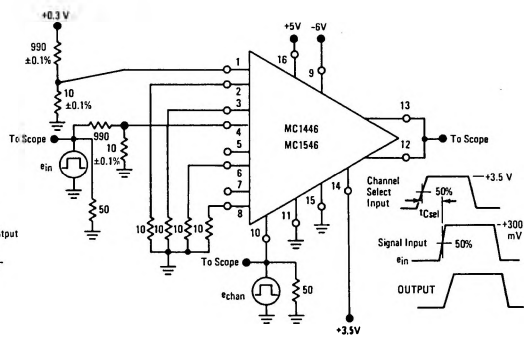


FIGURE 10 – CHANNEL SELECT TIME



TYPICAL RECOVERY TIME WAVEFORMS

FIGURE 11 – COMMON-MODE RECOVERY TIME

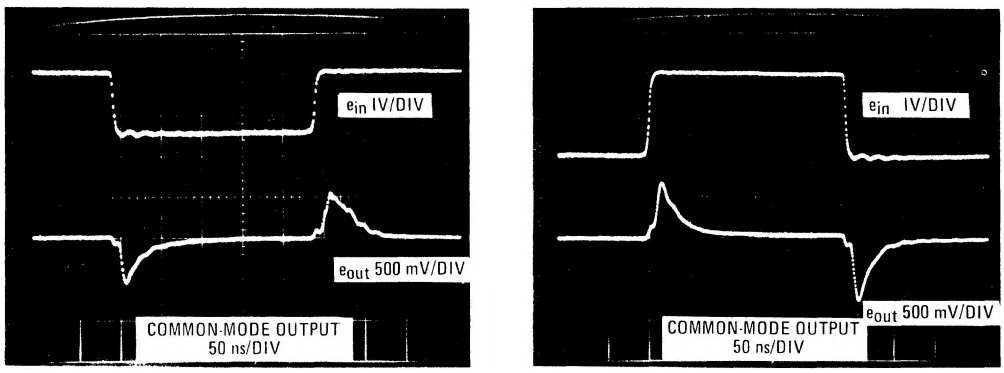
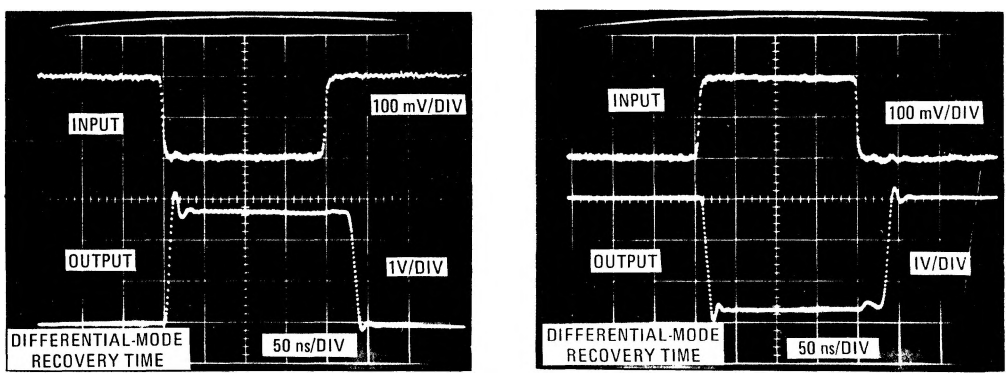


FIGURE 12 – DIFFERENTIAL-MODE RECOVERY TIME



TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted)

FIGURE 13 – VOLTAGE GAIN versus TEMPERATURE

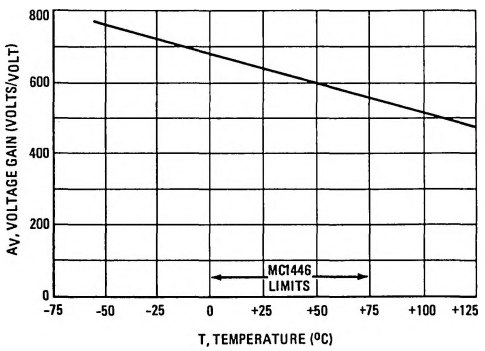


FIGURE 14 – DC OUTPUT VOLTAGE LEVEL versus TEMPERATURE (All Inputs Grounded)

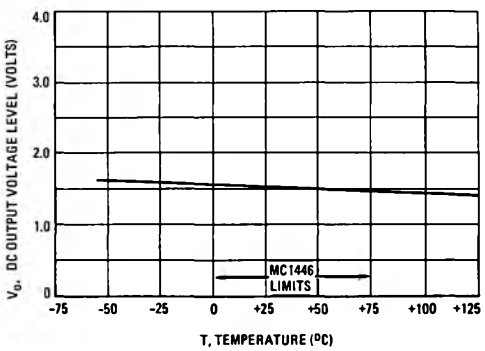


FIGURE 15 – AMPLIFIER TRANSFER CHARACTERISTICS

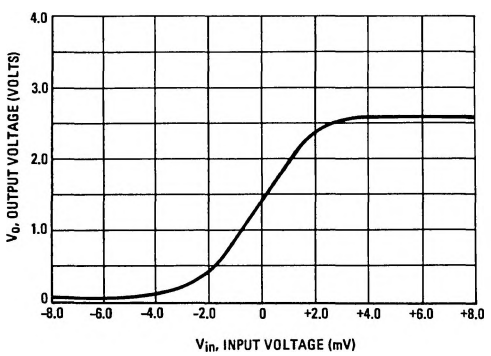


FIGURE 16 – CHANNEL SELECT versus OUTPUT TRANSFER CHARACTERISTICS

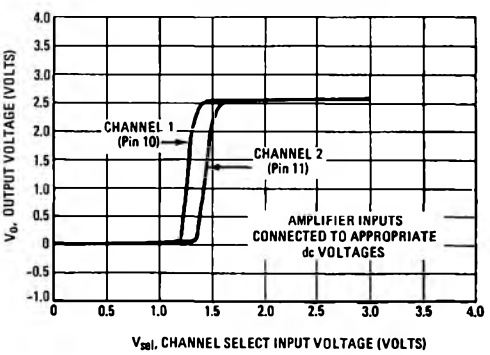


FIGURE 17 – STROBE INPUT TRANSFER CHARACTERISTICS (Input High)

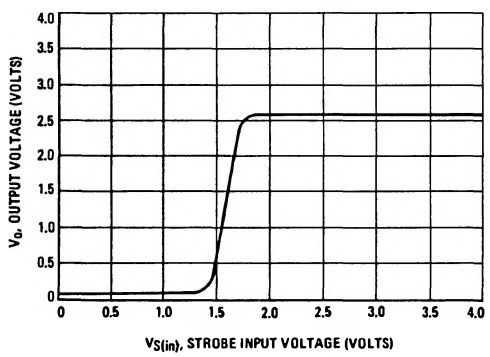
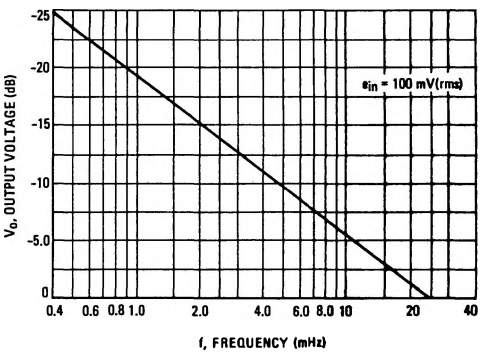


FIGURE 18 – COMMON-MODE GAIN versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 19 – VOLTAGE GAIN versus FREQUENCY

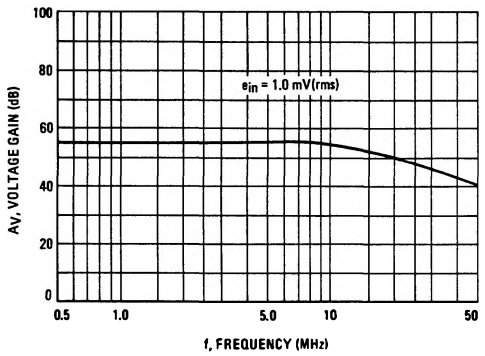
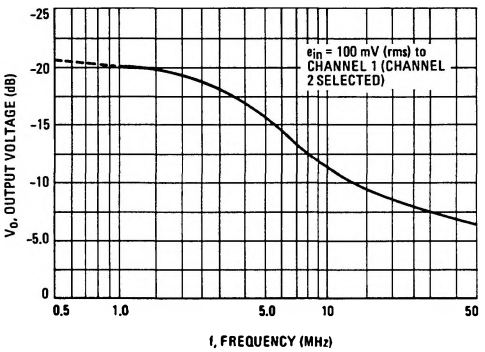


FIGURE 20 – ADJACENT CHANNEL ISOLATION versus FREQUENCY



CIRCUIT DESCRIPTION OF THE MC1546L/MC1446L

The MC1546L/MC1446L was designed to translate a positive 3.0 mV signal from a plated wire memory to an MTTL "1" level, or a negative 3.0 mV to an MTTL "0" level. This sense amplifier also eliminates the requirement for a bipolar switch in series with the plated wire because the bit selection is done inside the sense amplifier.

The circuit operation can be described in sections as follows:

1. All channels have been designed for low input offsets – 0.5 V typical.
2. Channel "ORing" is accomplished by using common collector load resistors for four differential amplifier pairs.
3. Channel selection is accomplished by current steering through the four differential pairs. The circuit below the four differential pairs forms a matrix tree which can be thought of as a 2-by-4 decode matrix. The bottom transistor is the current source for the first stage of gain.
4. DC translation between the first and second stages of gain is done through an emitter-follower stage, two diodes and another emitter follower for each side of the differential amplifier. The currents in these translator legs are combined and run through diodes to the negative supply. These diodes are used to bias both the first and second gain stages. This also gives the appropriate gain versus temperature and dc output level versus temperature characteristics.
5. The top of the second stage amplifier is regulated at a voltage equal to five diode drops above ground. It can be seen that if the 700 ohm resistor in the regulator has one diode (or V_{BE}) across it then the 2.8 k ohm resistor will have four diode drops across it. This makes a five diode drop voltage above ground that is fairly independent of the positive supply.
6. The current in the second stage of the amplifier is set by the 180-ohm resistor in the emitter of the current source. It can be seen that this resistor has one diode drop (approximately 750 mV) across it. Therefore, an analysis will show that the voltage drop across the 775-ohm load resistor in the second stage will be approximately two diodes when the differential amplifier is balanced. Accounting for the additional diode voltage drop of the emitter-follower output transistor will set the output dc level at two diodes above ground or very near the center of MTTL threshold.
7. The strobe circuit works by steering current in the second stage. When the strobe is low, the entire current of the second stage current source is steered through the 775-ohm load resistor. This clamps the output to a low state so that an input signal cannot cause an output. When the strobe is high, the current is steered through the second stage differential amplifier pair and the output will go to a level dictated by the presence of an input signal.
8. The output circuit of the sense amplifier may be thought of as a push-pull type. The emitter of the push transistor is brought out to a separate pin from the collector of the pull transistor. This will facilitate "Wire ORing" the outputs of several sense amplifiers. Several emitter outputs can be wired together along with only one collector pull-down transistor. The unused collectors of the pulldown transistor must be grounded. An example of the use of "Wire ORing" is to have four MC1546 devices wired-OR into a 16-channel sense amplifier in which a channel may be selected by selecting channels in parallel at the amplifier inputs and strobing the proper sense amplifier.

APPLICATIONS INFORMATION

The MC1546/MC1446 devices are designed to convert signals from plated-wire memories as small as positive or negative 3 mV to MTTL logic levels. The output level of the sense amplifier with no input signal present and with the strobe high is typically 1.4 volts (typical input threshold of MTTL logic). Hence, if the strobe goes high during the absence of an input signal from the plated-wire memory, the sense amplifier output will rise to 1.4 volts. This condition could cause false outputs; therefore careful considerations must be given to strobe timing. Figure 21 illustrates a typical timing sequence of the MC1546/MC1446 device as recommended for proper operation.

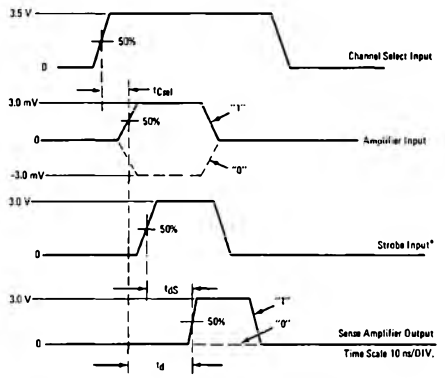
Figure 22 shows how these sense amplifiers are used in an N-word-line-by-32-bit basic memory plane organized as 4-N words of 8 bits each. During a read cycle, the read current is pulsed through a selected word-line and thus generates outputs to all of the 32-bit positions in the line. The internal one-of-four decoder selects the desired channels of the eight sense amplifiers for a particular system word. When the strobe goes high, the sense amplifier outputs switch according to the data present at the amplifier inputs. The data readout on the other 24-bit lines is not lost due to the Non-Destructive Read-Out properties of a plated-wire memory. On the next read cycle the decoder of the sense amplifier in combination with the selected word-line determines the 8-bits of data to read.

APPLICATIONS INFORMATION (continued)

Memory organizations that have more than four words per word-line require that the sense amplifier outputs be wired-OR. To wire-OR the outputs of several sense amplifiers all of the emitters of the output-pullup transistors are tied together. Only one collector of the pulldown transistors is tied to the wired-OR emitters of the pullup transistors. The remaining pulldown transistors must be grounded as noted in Figure 23. Ten or more sense amplifiers may be wired-OR together.without any reduction in usable logic levels since only one sense amplifier per bit is on at any given time. Variations in propagation delay time (t_{pd}), versus the number of wired-OR sense amplifiers and the output capacitance are given in Figure 24.

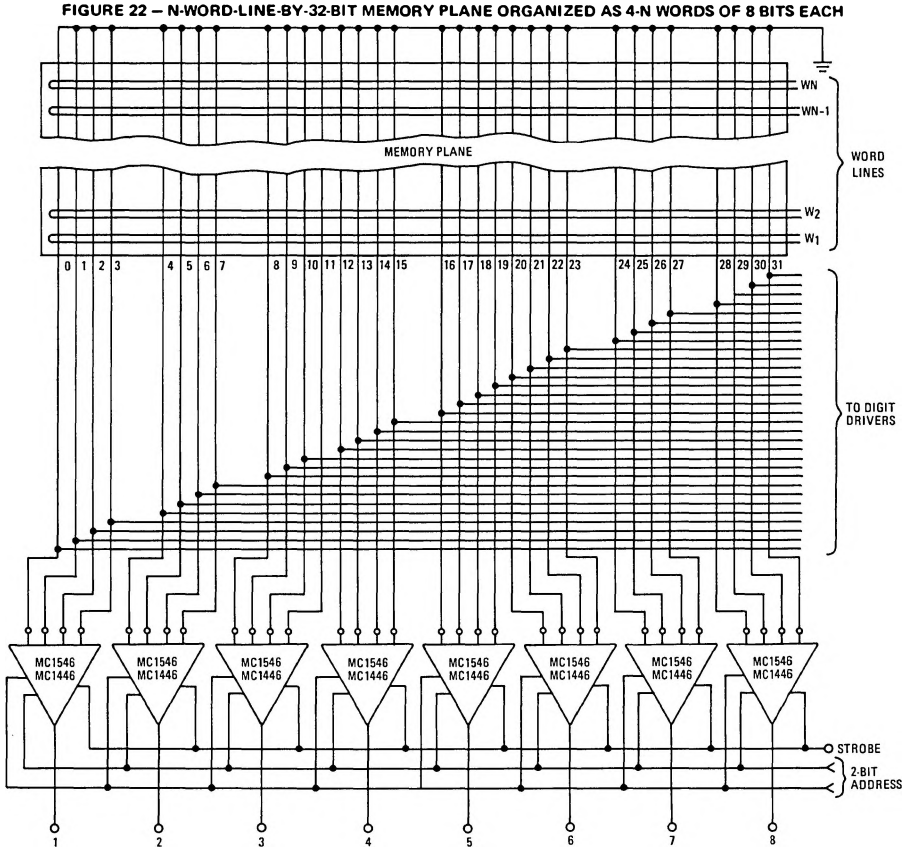
In Figure 25, eight are required for each bit of a 32-word/word-line memory. For those sense amplifiers that have wired-OR outputs, the strobe is used for decoding by attaching each strobe to a 3-bit-binary-to-1-of-8-bit decoder (MC4006). Thus only one sense amplifier per bit can be strobed at a given time. High fan-out gates are required on the channel select lines since a high current must be supplied to the select lines to drive them to the logic "1" level. The strobe current is low, thereby allowing many strobe lines to be driven with only one gate.

FIGURE 21 – TYPICAL TIMING SEQUENCE OF THE MC1546/MC1446



*The strobe pulse width is smaller than the amplifier input pulse width.

FIGURE 22 – N-WORD-LINE-BY-32-BIT MEMORY PLANE ORGANIZED AS 4-N WORDS OF 8 BITS EACH



APPLICATIONS INFORMATION (continued)

FIGURE 23 – WIRED "OR" MC1546/MC1446 DEVICES

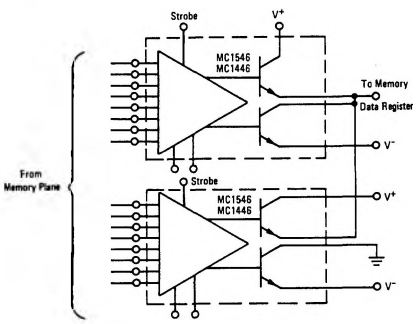


FIGURE 24 – TYPICAL PROPAGATION DELAY TIME VARIATION
(per number of devices at stated capacitance)

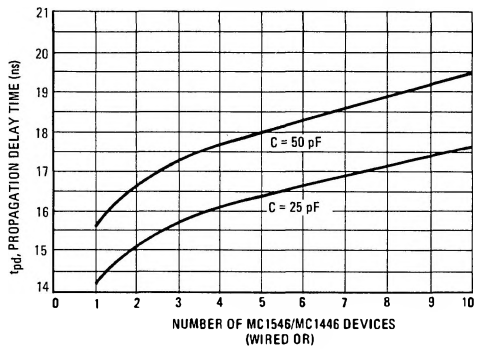
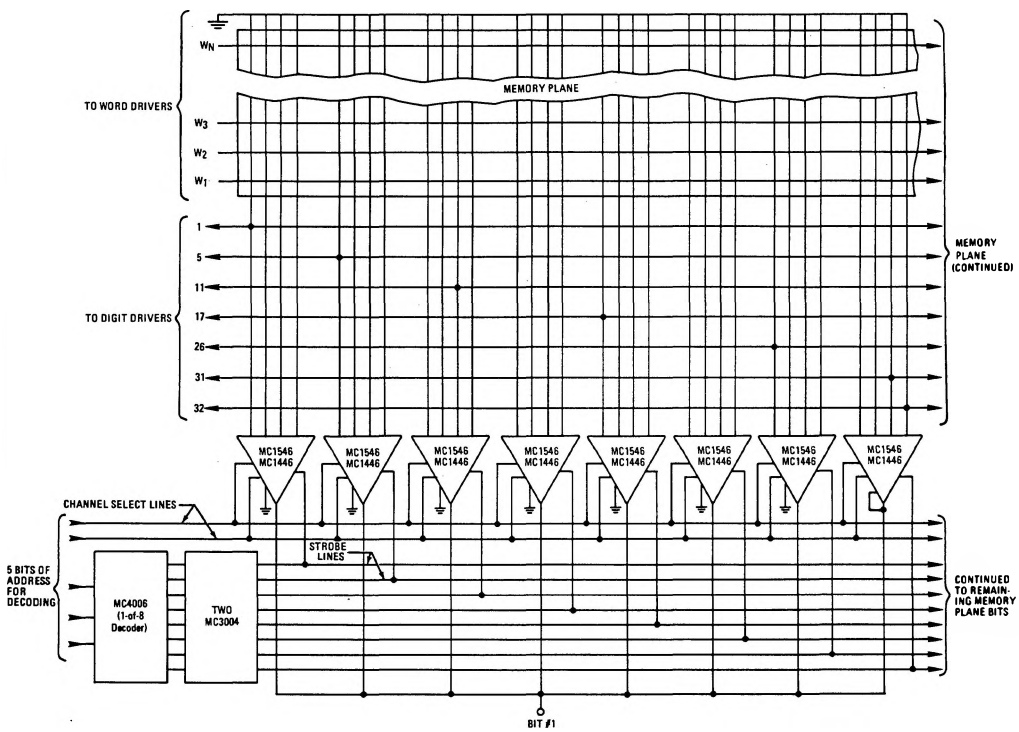


FIGURE 25 – 32 WORDS/WORD - LINE ORGANIZED MEMORY



DEFINITIONS

A_V the voltage gain from a channel input to amplifier output (input signal is 2 mV peak-to-peak and the strobe is high)

CMV_{in} maximum input common-mode voltage on any channel that will not cause the amplifier to saturate

DMV_{in} maximum input differential-mode voltage on any channel signal that will not saturate the amplifier

I^+ current from the positive supply with no load (pin 12 shorted to pin 13)

I^- current into the negative supply with both channel select pins at +3.5 volts

I_b input current into the base of any input transistor when the opposite transistor of the differential pair is at the same voltage

I_{CH} input current at channel select pin when the channel select voltage is at V_{CH}

I_{CL} input current at channel select pin when the channel select voltage is at V_{CL}

I_{io} difference between base currents of any input differential pair of transistors

I_{o+} output source current to a load with the output remaining above 2.4 volts, excluding the amplifier's own sink current

I_{o-} the current that the amplifier will sink into pin 12

t_{CMR} time required for the amplifier to recover from the maximum specified common-mode input, (recovery – output within 10% of its quiescent state)

$t_{C\,sel}$ time between the 50% point of the channel gate input and the 50% point of the signal input that still allows a full width signal at the amplifier output

t_{DMR} time required for the amplifier to recover from maximum specified differential-mode input, (recovery – output within 10% of its quiescent state)

t_{dS} delay time from the 50% point of the strobe input leading or trailing edge to the corresponding 50% point of the output

t_f time rise (and time fall) of the input signal must be less than 10 ns

t_{pd} the delay time from the 50% point of a 5.0 mV input leading or trailing edge to the corresponding 50% point of the amplifier output

t_r time from 10% to 90% of the rise and fall times respectively of the output signal with a 5.0 mV input signal

t_{Smin} minimum pulse width at 50% points at strobe input allows a full output (pulse rise times of less than 10 ns, amplifier differential input equal to 3 mV)

V_{CH} minimum voltage required at the channel select pin to cause a given channel to give 99% of the maximum gain through the amplifier

V_{CL} maximum voltage allowable at the channel select pin to cause a given channel to give 1% or less of the gain when channel is fully selected

V_o output dc level with inputs grounded and strobe high

V_{oH} minimum output high level

V_{oL} maximum output low level

V_{SH} the minimum voltage required at the strobe pin to allow 99% of a full output

V_{SL} the maximum voltage allowable at the strobe pin to allow 1% or less of a full output