MC145149

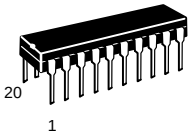
Dual PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

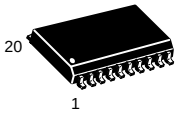
The MC145149 contains two PLL Frequency Synthesizers which share a common serial data port and common reference oscillator. The device contains two 14–stage R counters, two 10–stage N counters, and two 7–stage A counters. All six counters are fully programmable through a serial port. The divide ratios are latched into the appropriate counter latch according to the last data bits (control bits) entered.

When combined with external low–pass filters and voltage controlled oscillators (VCOs), the MC145149 can provide all the remaining functions for two PLL frequency synthesizers operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or dual–modulus prescaler can be used between the VCO and the synthesizer IC.

- Low Power Consumption Through Use of CMOS Technology
- Wide Operating Voltage Range: 3 to 9 V
- Operating Temperature Range: – 40 to + 85°C
- ÷ R Range = 3 to 16,383
- ÷ N Range = 3 to 1023
- ÷ A Range = 0 to 127
- Two "Linearized" Three–State Digital Phase Detectors with No Dead Zone
- Two Lock Detect Signals (LD1 and LD2)
- Two Open–Drain Port Expander Outputs (SW1 and SW2)
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs



P SUFFIX
PLASTIC DIP
CASE 738

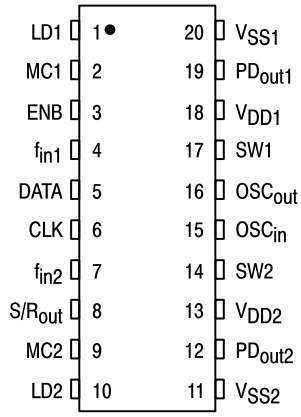


DW SUFFIX
SOG PACKAGE
CASE 751D

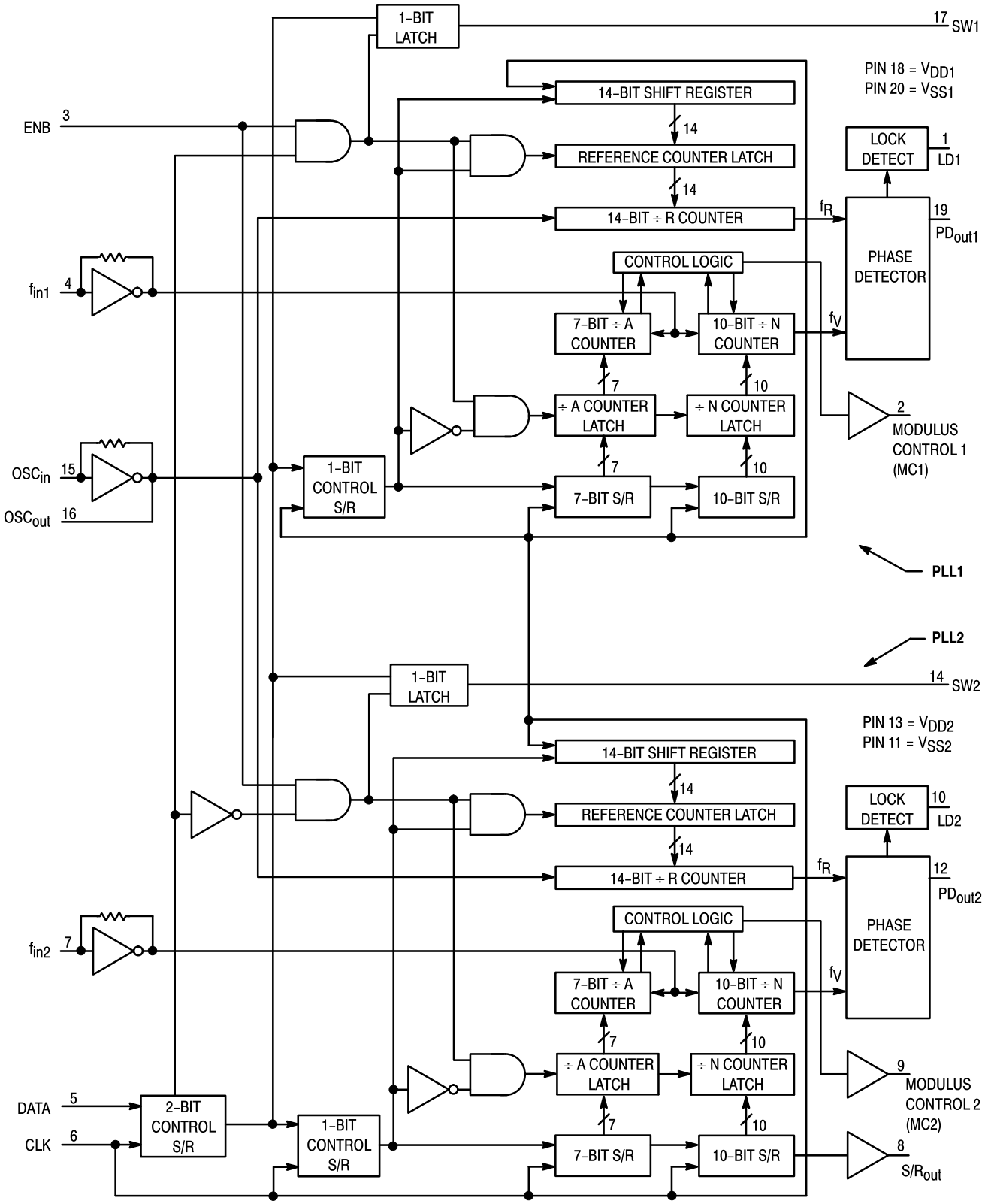
ORDERING INFORMATION

MC145149P	Plastic DIP
MC145149DW	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient) — SW1, SW2	– 0.5 to 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except SW1 and SW2 which may range up to 15 V.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs should be left floating.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	– 40°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range	—	3	9	3	9	3	9	V
V_{OL}	Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 µA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	1 Level	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
V_{IL}	Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} – 0.5 V (All Outputs Except OSC_{out})	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	1 Level	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
I_{OH}	Output Current — MC1, MC2 V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
I_{OL}	Output Current — SW1, SW2 V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.50	— — —	mA
I_{OH}	Output Current — Other Outputs V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OL}	V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
I_{in}	Input Current — DATA, CLK, ENB	9	—	± 0.3	—	± 0.1	—	± 1.0	µA
I_{in}	Input Current — f_{in}, OSC_{in}	9	—	± 50	—	± 25	—	± 22	µA

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	V_{DD} V	– 40°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
C_{in}	Input Capacitance	—	—	10	—	10	—	10	pF
C_{out}	Three–State Output Capacitance — PD_{out}	—	—	10	—	10	—	10	pF
I_{DD}	Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	—	1600 2400 3200	μA
I_{OZ}	Three–State Leakage Current — PD_{out} V_{out} = 0 V or 9 V	9	—	± 0.3	—	± 0.1	—	± 3.0	μA
I_{OZ}	Off–State Leakage Current — SW1, SW2 V_{out} = 9 V	9	—	0.3	—	0.1	—	3.0	μA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure No.	V_{DD} V	Min	Max	Unit
t_{TLH}	Output Rise Time, MC1 and MC2	1, 6	3 5 9	— — —	115 60 40	ns
t_{THL}	Output Fall Time, MC1 and MC2	1, 6	3 5 9	— — —	60 34 30	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time, LD and S/R_{out}	1, 6	3 5 9	— — —	140 80 60	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, f_{in} to MC1 or MC2	2, 6	3 5 9	— — —	125 80 50	ns
t_{su}	Setup Time, DATA to CLK	3	3 5 9	30 20 18	— — —	ns
t_{su}	Setup Time, CLK to ENB	3	3 5 9	70 32 25	— — —	ns
t_h	Hold Time, CLK to DATA	3	3 5 9	12 12 15	— — —	ns
t_{rec}	Recovery Time, ENB to CLK	3	3 5 9	5 10 20	— — —	ns
t_r, t_f	Input Rise and Fall Times, Any Input	4	3 5 9	— — —	5 2 0.5	μs
t_w	Input Pulse Width, ENB and CLK	5	3 5 9	40 35 25	— — —	ns

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz

SWITCHING WAVEFORMS

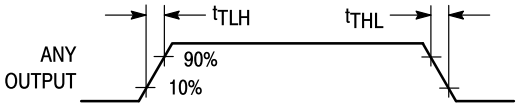


Figure 1.

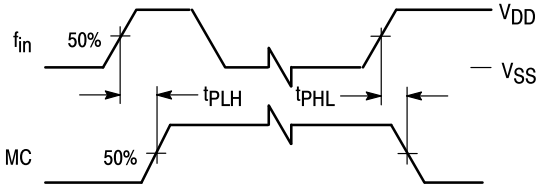


Figure 2.

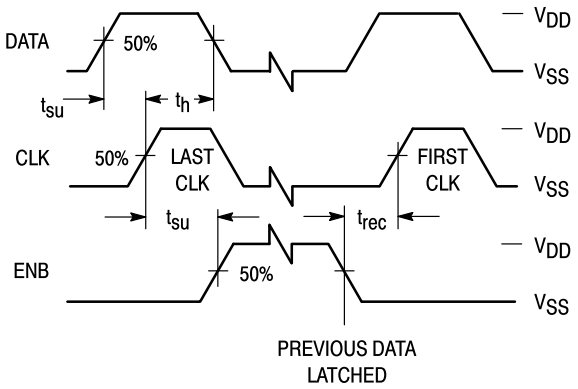


Figure 3.

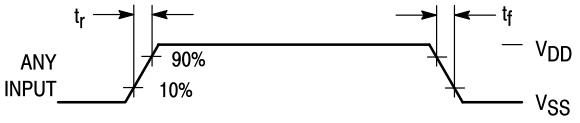


Figure 4.

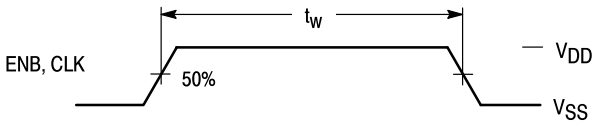
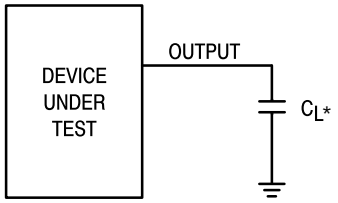


Figure 5.



* Includes all probe and fixture capacitance.

Figure 6.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 15, 16)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate value must be connected from OSC_{in} and OSC_{out} to ground.

OSC_{in} may also serve as input for an externally–generated reference signal. The signal is typically ac coupled to OSC_{in}, but for signals with CMOS logic levels, dc coupling may be used. When used with an external reference, OSC_{out} should be left open.

f_{in1}, f_{in2}
Frequency Inputs (Pins 4, 7)

Input frequency from an external VCO output. Each rising–edge signal on f_{in1} decrements the N counter, and when appropriate, the A counter of PLL 1. Similarly, f_{in2} decrements the counters of PLL 2.

These inputs have inverters biased on the linear region which allows ac coupling for signals as low as 500 mV p–p. With square wave signals which swing from V_{SS} to V_{DD}, dc coupling may be used.

DATA, CLK
Data, Clock Inputs (Pins 5, 6)

Shift register data and clock inputs. Each low–to–high transition on the clock pin shifts one bit of data into the on–chip shift registers. Refer to Figure 7 for the following discussion.

The last bit entered is a steering bit that determines which set of latches are activated. A logic high selects the latches for PLL 1. A logic low selects PLL 2.

The second–to–last bit controls the appropriate port expander output, SW1 or SW2. A logic low forces the output low. A logic high forces the output to the high–impedance state.

The third–to–last bit determines which storage latch is activated. A logic low selects the ÷ A and ÷ N counter latches. A logic high selects the reference counter latch.

When writing to either set of ÷ A and ÷ N counter latches, 20 clock cycles are typically used. However, if a byte–oriented MCU is utilized, 24 clock cycles may be used with the first 4 bits being “Don’t Care.”

When writing to either reference counter latch, 17 clock cycles are typically used. However, if a byte–oriented MCU is utilized, 24 clock cycles may be used with the first 7 bits being “Don’t Care”.

ENB
Latch Enable Input (Pin 3)

A positive pulse on this input transfers data from the shift registers to the selected latches, as determined by the control and steering data bits. A logic low level on this pin allows the user to shift data into the shift registers without affecting the data in the latches or counters. Enable is normally held low and is pulsed high to transfer data into the latches.

OUTPUT PINS

PD_{out1}, PD_{out2}
Single–Ended Phase Detector Outputs (Pins 19, 12)

Each single–ended (three–state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO (see Figure 8).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

S/R_{out}
Shift Register Output (Pin 8)

This output can be connected to an external shift register to provide band switching or control information. S/R_{out} may also be used to check the counter programming bit stream.

MC1, MC2
Modulus Control Outputs (Pins 2, 9)

Each output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N–A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters are preset to their respective programmed values, and the above sequence is repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

LD1, LD2
Lock Detect Signals (Pins 1, 10)

Each output is essentially at a high logic level when the corresponding loop is locked (f_R and f_V of the same phase and frequency). Each output pulses low when the corresponding loop is out of lock (see Figure 8).

SW1, SW2
Latched Open–Drain Switch Outputs (Pins 17, 14)

The state of each output is controlled by the “SW STATE” bit shown in Figure 7. If the bit is a logic high, the corresponding SW output assumes the high–impedance state. If the bit is low, the SW output goes low.

To control output SW1, steering bit PLL 1/PLL 2 shown in Figure 7 must be high. To control SW2, bit PLL 1/PLL 2 must be low.

These outputs have an output voltage range of V_{SS} to 15 V.

POWER SUPPLY PINS

V_{DD1}, V_{DD2}
Positive Power Supply (Pins 18, 13)

The most positive power supply potentials. Both of these pins are connected to the substrate of the chip. Therefore, both must be tied to the same voltage potential. This potential may range from 3 to 9 V with respect to the V_{SS} pins.

For optimum performance, V_{DD1} should be bypassed to V_{SS1} and V_{DD2} bypassed to V_{SS2}. That is, two separate bypass capacitors should be utilized.

V_{SS1}, V_{SS2}
Negative Power Supply (Pins 20, 11)

The most negative power supply potentials. Both of these pins should be tied to ground.

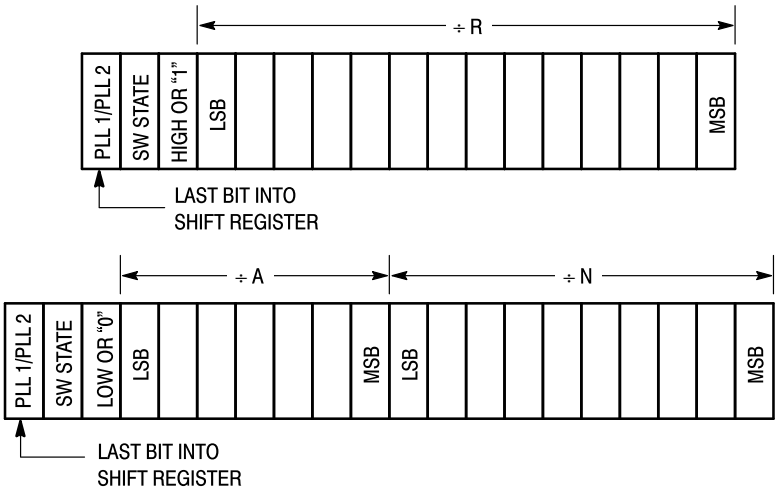
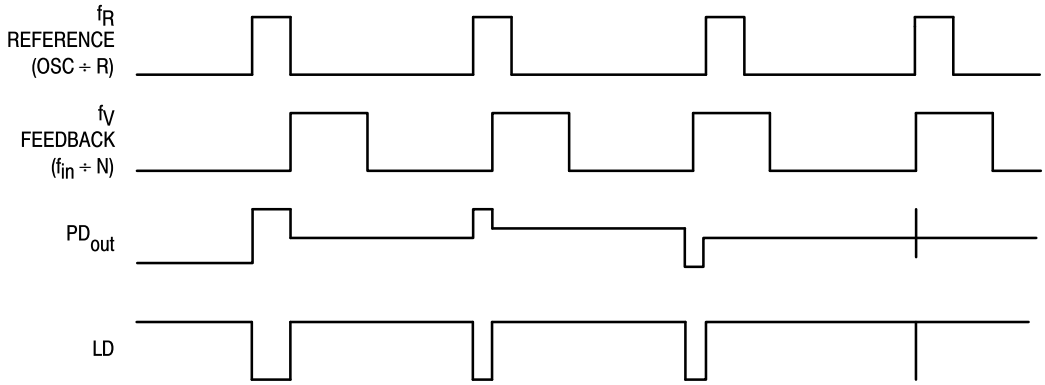


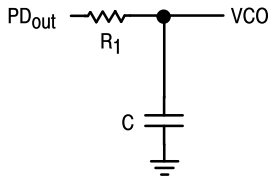
Figure 7. Bit Stream Formats



NOTE: The PD output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 8. Phase Detector/Lock Detector Output Waveforms

A)

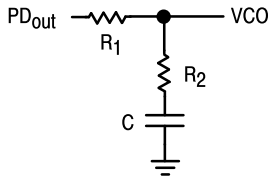


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design ω_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

Figure 9. Phase–Locked Loop Low–Pass Filter Design

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensate crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at

the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1 + C2}$$

where

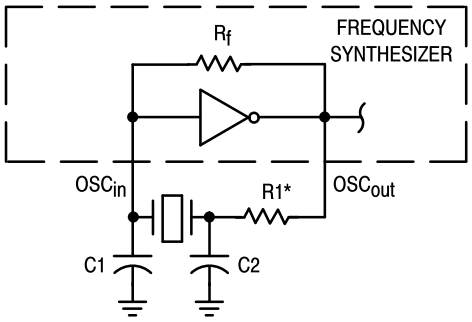
C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

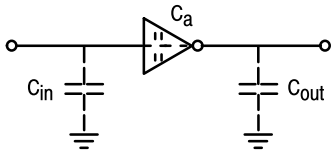
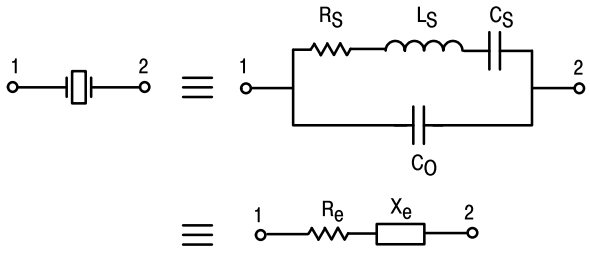


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity, and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145149 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.,

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from 0 through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1) P + A$ or $(P - 1) P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

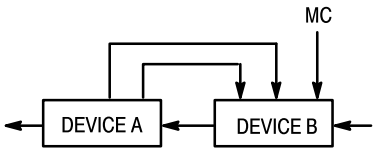
For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable.

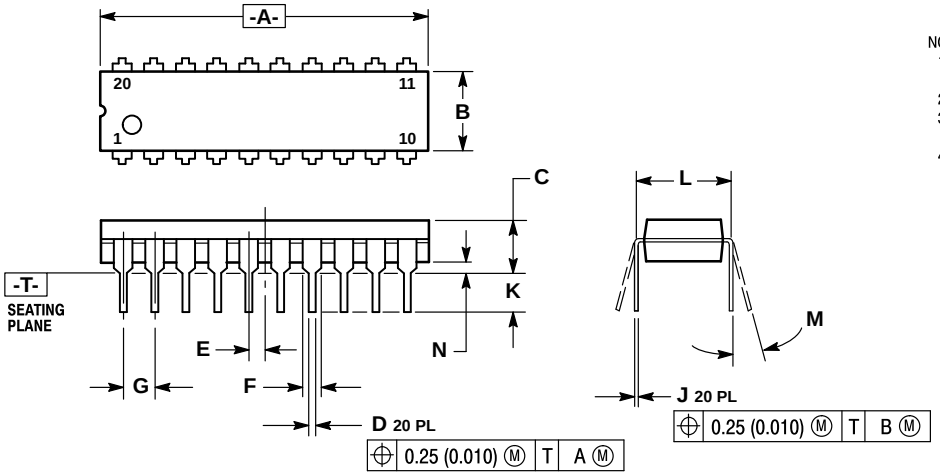


DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 OR ÷ 80/÷ 81	÷ 64/÷ 65 OR ÷ 128/÷ 129	÷ 80/÷ 81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

PACKAGE DIMENSIONS

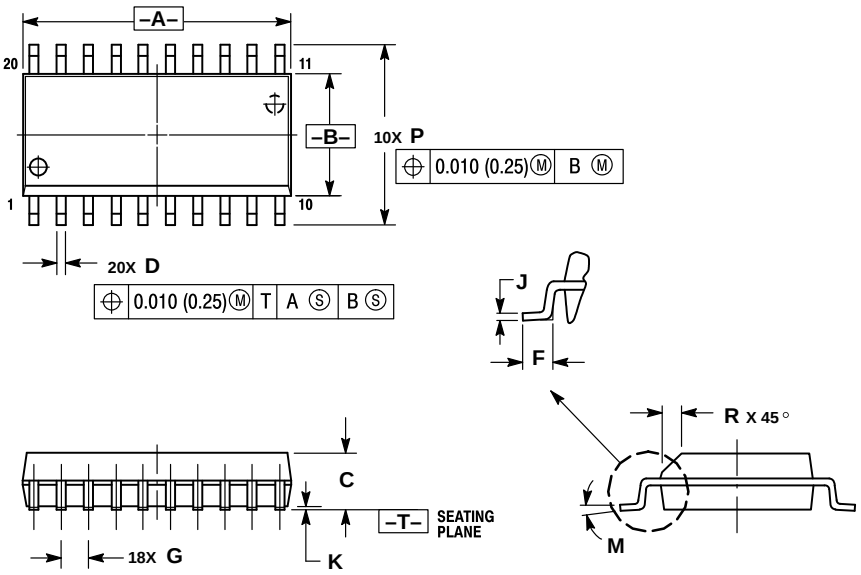
P SUFFIX
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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