

# MC145444

## Advance Information Single-Chip 300-Baud Modem

MC145444 is a silicon gate CMOS frequency shift keying (FSK) modem intended for use with telemetry systems or remote control systems over the telephone network.

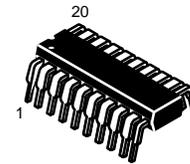
This device is compatible with CCITT V.21 and contains the entire circuit that provides a full-duplex or half-duplex 300-baud data communication over a pair of telephone lines. This device also includes the DTMF generator and call progress tone detector (CPTD).

The differential line driver has the capability of driving 0 dBm into a 600 Ω load with a single +5 V power supply.

The transmit level is controlled by the programmable attenuator in 1 dB steps.

Devices functions are controlled through a 3-wire serial interface.

- Capable of Driving 0 dBm into a 600 Ω Load
- DTMF Generator On-Chip
- Imprecise Call Progress Detector On-Chip
- A Transmit Attenuator Programmable in 1 dB Steps
- 3-Wire Serial Interface
- Compatible with CCITT V.21
- 2100 Hz Answer Tone Generator On-Chip
- Analog Loopback Configuration for Self Test
- Simplex, Half-Duplex, and Full-Duplex Operation



**H SUFFIX**  
PLASTIC DIP  
CASE 804



**DW SUFFIX**  
SOG PACKAGE  
CASE 751D

### ORDERING INFORMATION

MC145444P Plastic DIP  
MC145444DW SOG Package

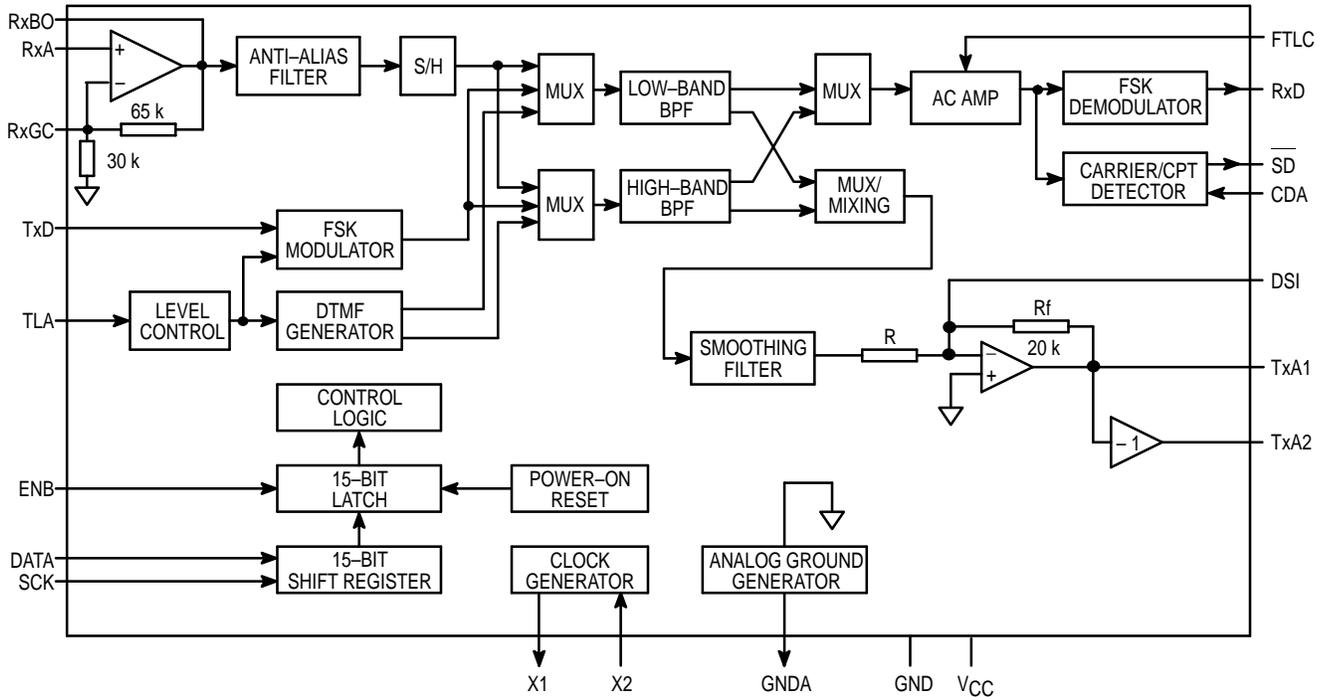
### PIN ASSIGNMENT

RxB0	1	20	RxGC
FTLC	2	19	RxA
GNDA	3	18	TxA1
CDA	4	17	TxA2
GND	5	16	DSI
TLA	6	15	V <sub>CC</sub>
X1	7	14	ENB
X2	8	13	SCK
SD	9	12	DATA
RxD	10	11	TxD

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0  
8/95

## BLOCK DIAGRAM



### MAXIMUM RATINGS\* (Voltages Referenced to $V_{SS}$ )

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage	$V_{in}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage	$V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Clamp Diode Current per Pin	$I_{IK}, I_{OK}$	$\pm 20$	mA
DC Current per Pin	$I_{out}$	$\pm 25$	mA
Power Dissipation	$P_D$	500	mW
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{CC}$	4.5	5	5.5	V
DC Input Voltage	$V_{in}$	0	—	$V_{CC}$	V
DC Output Voltage	$V_{out}$	0	—	$V_{CC}$	V
Input Rise Time	$t_r$	0	—	500	ns
Input Fall Time	$t_f$	0	—	500	ns
Crystal Frequency	$f_{osc}$	—	3.579545	—	MHz
Operating Temperature Range	$T_A$	-20	25	70	$^{\circ}C$

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	H Level	$V_{IH}$		3.15	—	—	V
	L Level	$V_{IL}$		—	—	1.1	
Output Voltage	H Level	$V_{OH}$	$I_{OH} = 20\ \mu\text{A}$	$V_{CC} - 0.1$	$V_{CC} - 0.01$	—	V
	L Level	$V_{OL}$	$I_{OL} = 20\ \mu\text{A}$ $I_{OL} = 2\ \text{mA}$	—	0.01	0.1 0.4	
Input Current DATA, SCK, E, TxD		$I_{in}$	$V_{in} = V_{CC}$ or GND	—	$\pm 1.0$	$\pm 10.0$	$\mu\text{A}$
Quiescent Supply Current		$I_{CC}$	FSK Mode	—	8	—	mA
Power-Down Supply Current		$I_{CC}$	Power-Down Mode 1	—	—	300	$\mu\text{A}$
		$I_{CC}$	Power-Down Mode 2	—	—	1	$\mu\text{A}$

**TRANSMIT CARRIER CHARACTERISTICS** ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Carrier Frequency Channel 1	Mark "1"	$f_{1M}$	Crystal Frequency 3.579545 MHz	974	980	986	Hz
	Space "0"	$f_{1S}$		1174	1180	1186	
Carrier Frequency Channel 2	Mark "1"	$f_{2M}$		1644	1650	1656	
	Space "0"	$f_{2S}$		1844	1850	1856	
Answer Tone		$f_{ans}$		2094	2100	2106	
Transmit Carrier Level		$V_{O^*}$		Attenuator = 0 dB RTLA = $\infty$	—	6	
Second Harmonic Energy		$V_{2h^*}$	—		-46	—	dBm
Out-of-Band Energy		$V_{OE^*}$	Figure 1			dBm	

\*  $V_{TXA1} - V_{TXA2}$ ,  $R_L = 1.2\ \text{k}\Omega$

**TRANSMIT ATTENUATOR CHARACTERISTICS** ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Attenuator Range	$A_{RNG}$		0	—	15	dB
Attenuator Accuracy	$A_{ACC}$		-0.5	—	+0.5	dB

**RECEIVER CHARACTERISTICS (Includes Hybrid, Demodulator and Carrier Detector)**

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance		$R_{IRX}$	RxA Pin (Pin 19)	50	—	—	$\text{k}\Omega$
Receiver Carrier Amplitude		$V_{IRX}$		-48	—	-12	dBm
Carrier Detect	OFF to ON	$V_{CDON}$	$CDA = 1.2\ \text{V}$ $f_{in} = 1.0\ \text{kHz}$	—	-44	—	dBm
Threshold	ON to OFF	$V_{CDOF}$		—	-47	—	
Hysteresis ( $V_{CDON} - V_{CDOF}$ )		$H_{VS}$		2	—	—	
Carrier Detect Timing	OFF to ON	$T_{CDON}$	CD1 = 0, CD0 = 0	—	450	—	ms
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	80	—	
	ON to OFF	$T_{CDOFF}$	CD1 = 0, CD0 = 0	—	30	—	
			CD1 = 0, CD0 = 1	—	30	—	
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	10	—	

**BAND-PASS FILTER CHARACTERISTICS (RxA to FTLC) ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )**

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
FTLC Output Impedance	ROFT		10	—	50	k $\Omega$
Adjacent Channel Rejection	REJ	$V_{RxA} = -12\text{ dBm}$	—	50	—	dB
Pass-Band Gain	GPAS		—	10	—	dB
Group Delay		Low-Band Filter 930 – 1230 Hz	—	700	—	$\mu\text{s}$
		High-Band Filter 1600 – 1900 Hz	—	800	—	

**DTMF CHARACTERISTICS ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )**

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Tone Output Level	Low Group		—	3	—	dBm
	High Group		—	4	—	
High Group Pre Emphasis	$P_E$	Attenuator = 0 dB $RTLA = \infty$ Crystal Frequency 3.579545 MHz	0	—	3	dB
DTMF Distortion	DIST		—	5	—	%
DTMF Frequency Variation	$\Delta f_V$		-1	—	1	%
Out-of-Band Energy	$V_{OE}^*$		Figure 1		—	dB
Setup Time	$t_{osc}$		—	4	—	ms

\*  $V_{TXA1} - V_{TXA2}$ ,  $R_L = 1.2\text{ k}\Omega$

**CPTD CHARACTERISTICS ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )**

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit	
Band-Pass Filter Center Frequency	$f_c$		—	400	—	Hz	
Band-Pass Filter – 3 dB Band Width	$\Delta BW$		—	140	—	Hz	
Tone Detect Level	OFF to ON	$CDA = 1.2\text{ V}$ $f_{in} = 400\text{ Hz}$	—	-44	—	dBm	
	ON to OFF		—	-47	—		
Tone Detect Timing	OFF to ON		$T_{TDON}$	—	10	—	ms
	ON to OFF		$T_{TDOF}$	—	25	—	

**DEMODULATOR CHARACTERISTICS ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )**

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Bit Bias	ID	Input Level = -24 dBm	—	5	—	%
Bit Error Rate	BER	Input Level = -24 dBm CCITT Line Simulation 511 Bit Pattern S/N = 5 dB	—	0.00001	—	—

**SWITCHING CHARACTERISTICS ( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $T_A = -20$  to  $+70^\circ\text{C}$ )**

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Setup Times	DATA to SCK		50	—	—	ns
	SCK to ENB		50	—	—	
Hold Time	SCK to DATA		50	—	—	ns
Recovery Time	ENB to SCK		50	—	—	ns
Input Rise Time	$t_r$		—	—	2	$\mu\text{s}$
Input Fall Time	$t_f$		—	—	2	$\mu\text{s}$
Input Pulse Width	ENB, SCK		50	—	—	ns

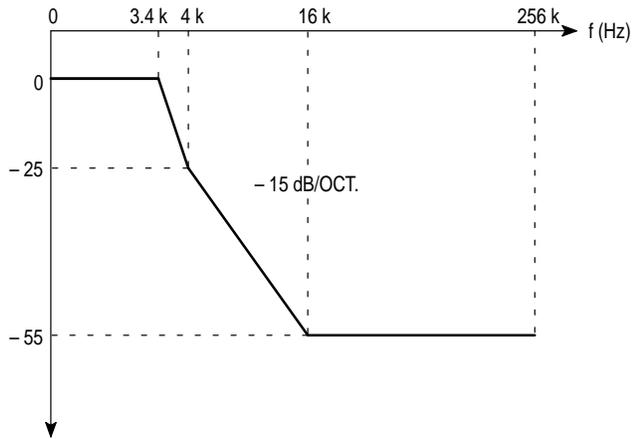


Figure 1. Out-of-Band Energy

## PIN DESCRIPTION

### VCC

#### Positive Power Supply (Pin 15)

This pin is normally tied to the + 5.0 V. A 0.1  $\mu$ F decoupling capacitor should be used.

### GND

#### Ground Pin (Pin 5)

This pin is normally tied to 0 V.

### GNDA

#### Analog Ground (Pin 3)

Analog ground is internally biased to  $(V_{CC} - V_{SS})/2$ . It should be tied to ground through a 0.1  $\mu$ F and 100  $\mu$ F capacitor.

### X1

#### Crystal Oscillator Output (Pin 7)

Connecting a 3.579545 MHz  $\pm$  0.1% crystal between X1 and X2 will cause the transmit frequencies to be within  $\pm$  64 MHz of nominal. X1 is capable of driving several CMOS gates. An external clock may be applied to X2. X1 should then be left open.

### X2

#### Crystal Oscillator Input (Pin 8)

Refer to X1.

### SCK

#### Shift Register Clock Input (Pin 13)

This pin is the clock input for the 15-bit shift register. Serial data is loaded into the shift register on the rising edge of this clock.

### DATA

#### Serial Data Input (Pin 12)

This pin is the 15-bit serial data input. This data determines the mode, DTMF signal, transmit attenuation, carrier detect time, channel, and transmit squelch.

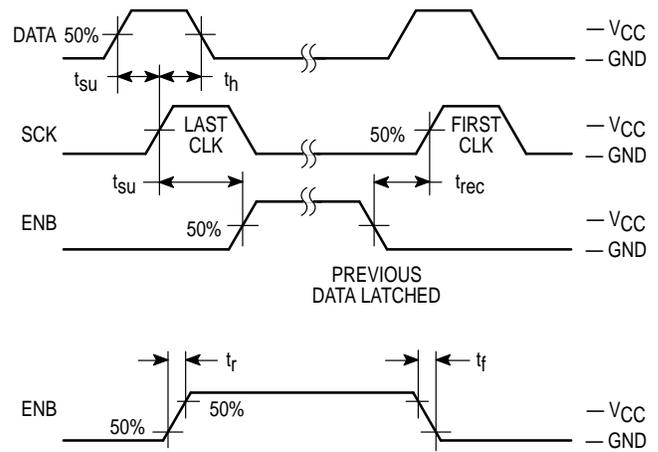


Figure 2. Switching Characteristics

### ENB

#### Enable Input (Pin 14)

Data is loaded into the 15-bit shift register when this pin is at a logic low. When this pin transitions from a logic high to low, the data is transferred to the internal latch on the falling edge of ENB. New data loaded into the shift register will not affect the device operation until this pin transitions from high to low. (See Figure 2.)

### TxD

#### Transmit Data Input (Pin 11)

This pin is the transmit data input. The mark frequency is generated when this pin is at the logic high level. The space frequency is generated when the pin is at a logic low.

### RxD

#### Receive Data Output (Pin 10)

This pin is the receive data output. A high logic level of this pin indicates that the mark carrier frequency has been received, and a low logic level indicates the space carrier frequency has been received.

### SD

#### Carrier/Call Progress Tone Detect (Pin 9)

This pin is the output from the carrier detector or call progress tone detector. This pin works as a carrier detector in the FSK mode and as the call progress tone detector in the CPTD mode. The output goes to a logic low level when the input signal reaches the minimum threshold of the detect level that is adjusted by the CDA voltage. When SD = H, the receive data output (RxD) is clamped high to avoid errors that may occur with loop noise. The SD pin is also clamped high in the other modes except during the power-down mode.

### TxA1

#### Non-Inverting Transmit Analog Carrier Output (Pin 18)

This pin is the line driver non-inverting output of the FSK and tone transmit analog signals. A + 6 dBm (max) differential output voltage can be obtained by connecting a 1.2 k $\Omega$  load resistor between Tx1 and Tx2. Attention must be set so as not to exceed this level when an external input is added to the DSI pin. A telephone line (600  $\Omega$ ) is driven through an external 600  $\Omega$  resistor. In this case, the output level becomes about half of differential output.

**TxA2**  
**Inverting Transmit Analog Carrier Output (Pin 17)**

This pin is the line driver inverting output. The signal is equal in magnitude, but 180° out of phase with the TxA1 (refer to TxA1).

**RxA**  
**Receive Signal Input (Pin 19)**

This pin is the receive signal input. The pin has an input impedance of 50 kΩ (min).

**RxGC**  
**Receive Gain Adjust (Pin 20)**

This pin is used to adjust the receive buffer gain. To adjust the gain, the signal from the RxBO through a divider is added as a feedback. This pin may be held open when the gain adjustment is not needed.

**RxBO**  
**Receiver Buffer Output (Pin 1)**

This pin is the receive buffer output.

**DSI**  
**Driver Summing Input (Pin 16)**

This pin is the inverting input of the line driver. An external signal is transmitted through an external series resistor R<sub>DSI</sub>. The differential gain  $G_{DSI} = (V_{TXA1} - V_{TXA2})/V_{DSI}$  is determined by the following equation.

$$G_{DSI} = -2R_f / R_{DSI}, R_f \approx 20 \text{ k}\Omega$$

DSI should be left open when not used.

**CDA**  
**Carrier Detect Level/CPTD Level Control (Pin 4)**

The carrier/call progress tone detect level is programmed with a CDA pin voltage.

When this pin is held open, the CDA voltage is set to 1.2 V with an internal divider. The detect level is set at -44 dBm (typ) for off to on, and -47 dBm (typ) for on to off. The minimum hysteresis is 2 dB. This pin has a very high input impedance so it should be connected to GND with a 0.1 μF capacitor to keep it well regulated. An external voltage may be applied to this pin to adjust the carrier detect threshold. The following equations may be used to find the CDA voltage required for a given threshold voltage.

$$V_{CDA} = 245 \times V_{On}$$

$$V_{CDA} = 347 \times V_{Off}$$

**FTLC**  
**Filter Test (Pin 2)**

This pin is a high-impedance filter output. It may be used to check the receive filter. This pin also may be used as a demodulator input. In normal operation, this pin is connected to the GNDA through a 0.1 μF bypass capacitor. This pin handles very small signals so care must be used with the capacitor's wiring.

**TLA**  
**Transmit Carrier Level Adjust (Pin 6)**

This pin is used to adjust the transmit carrier level that is determined by the value of the resistor (RTLA) connected

between this pin and GND. The maximum transmit level is obtained when this pin is connected to GND (RTLA = 0).

**SERIAL INTERFACE**

The following six functions are set up with the 15-bit serial data.

FUNCTION MODE	:	M2	M1	M0	
TRANSMIT ATTENUATOR	:	A3	A2	A1	A0
TRANSMIT SQUELCH	:	SQ			
TONE FREQUENCY	:	T3	T2	T1	T0
CHANNEL	:	CH			
CARRIER DETECT TIME	:	CD1	CD0		

Figure 3 presents the 15-bit serial data timing, starting with the carrier detect time, CD1, followed by the channel, the tone frequency, the transmit squelch, the transmit attenuator, and the function mode. This data is loaded into the internal shift register at the rising edge of the SCK signal and latched at the falling edge of the ENB signal.

**FUNCTION MODE**

Modes are selected from the following 3-bit data (M2 – M0, see Table 1).

**Table 1. Function Mode Truth Table**

M2	M1	M0	Function Mode
0	0	0	FSK
0	0	1	Analog Loopback
0	1	0	CPTD
0	1	1	Answer Tone
1	0	0	DTMF
1	0	1	Single Tone
1	1	0	Power-Down 1
1	1	1	Power-Down 2

The following paragraphs describe each function. Table 2 presents each output status.

**FSK Mode**

The transmitter and the receiver work as a FSK modulator/demodulator. The SD pin output is the carrier's detect signal.

**Analog Loopback Mode**

TxA1 connects to the receiver internally and FSK signals are demodulated. The frequency of the receiver is set up with the same frequency as the transmitter. The SD pin output is the carrier detect signal. An IC self test is supported with this function.

**CPTD Mode**

The receiver detects a 400 Hz call progress tone. The detect signal comes from the SD pin. The transmitter is disabled.

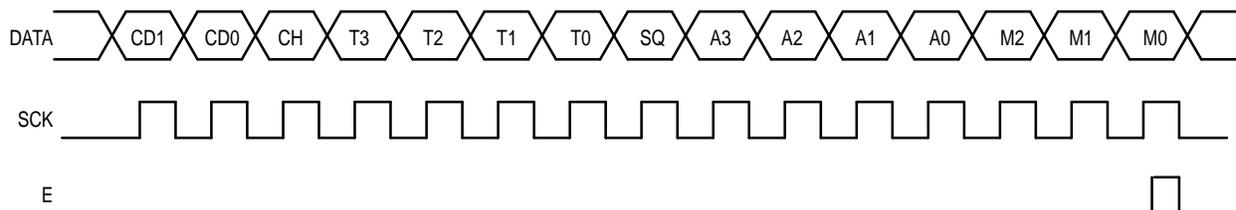


Figure 3. Serial Data Timing

Table 2. Output Status

Function Mode	Output		
	RxD	SD	TxA1, TxA2
FSK	Received Digital Data	Carrier Detect	FSK
Analog Loopback			
CPTD	H	CPTD	$V_{CC}/2$
Answer Tone	H	H	Answer Tone
DTMF	H	H	DTMF Tone
Single Tone	H	H	Single Tone
Power-Down 1, 2	High-Z	High-Z	High-Z

#### Answer Tone Mode

The transmitter works as 2100 Hz answer tone generator. The receiver is disabled.

#### DTMF Mode

The transmitter works as a DTMF tone generator. The receiver is disabled.

#### Single Tone Mode

The transmitter output is one of the DTMF eight frequencies. The receiver is disabled.

#### Power-Down Mode 1

Internal circuits except the oscillator are disabled, and all outputs except the X1 pin go to the high impedance state. The supply current decreases to 300  $\mu$ A (max).

#### Power-Down Mode 2

All circuits including the oscillator stop working and all outputs go to the high impedance state. The supply current decreases to 1.0  $\mu$ A (max).

#### Transmit Attenuator

Four-bit serial data (A3 – A0) sets up the analog transmit level in the FSK, answer tone, DTMF, analog loopback, and single tone mode. The range of the transmit attenuator is 0 – 15 dB in 1 dB steps. The external signal (DSI) is not affected by this attenuator.

#### tone FREQUENCY

The DTMF tones or the single tone mode is selected by the 4-bit serial data (T3 – T0).

**Table 3. Transmit Attenuator Truth Table**

A3	A2	A1	A0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

**Table 4. Tone Frequency Truth Table**

T3	T2	T1	T0	Tone Frequency (Hz)			
				DTMF Mode			Single Tone Mode
				Low Group	High Group	Keyboard Equivalent	
0	0	0	0	941	1633	D	941
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633
1	1	1	1	852	1633	C	1633

## TRANSMIT SQUELCH

The 1-bit serial data (SQ) controls the transmit analog signal. The FSK signal, DTMF tones, single tone, and answer tone are disabled. The external signal to the DSI will be transmitted at that time. The internal line driver works at all times except during the power-down mode.

SQ	Squelch
1	Enable
0	Disable

## CHANNEL

The transmit and receive channel is set up with a 1-bit serial data (CH) when the function mode is either in FSK or analog loopback.

When the function mode is either on the FSK or analog loopback mode, the transmit and receive channel is set up with a 1-bit serial data (CH).

CH	Channel
1	1 (Originate)
0	2 (Answer)

## CARRIER DETECT TIME

The carrier detect time (see Figure 4 and Table 5) is set by 2-bit serial data (CD1, CD0).  $t_{on}$  indicates the amount of time the carrier is greater than  $V_{on}$  threshold must be present before SD goes low.

$t_{off}$ , on the other hand, indicates the amount of delay time SD goes high after the carrier level becomes lower than  $V_{off}$  threshold.

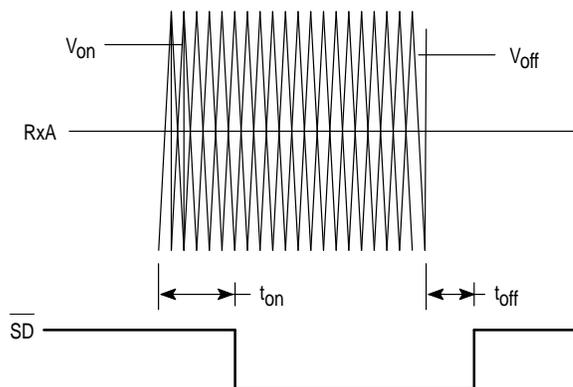


Figure 4. Carrier Detect Timing

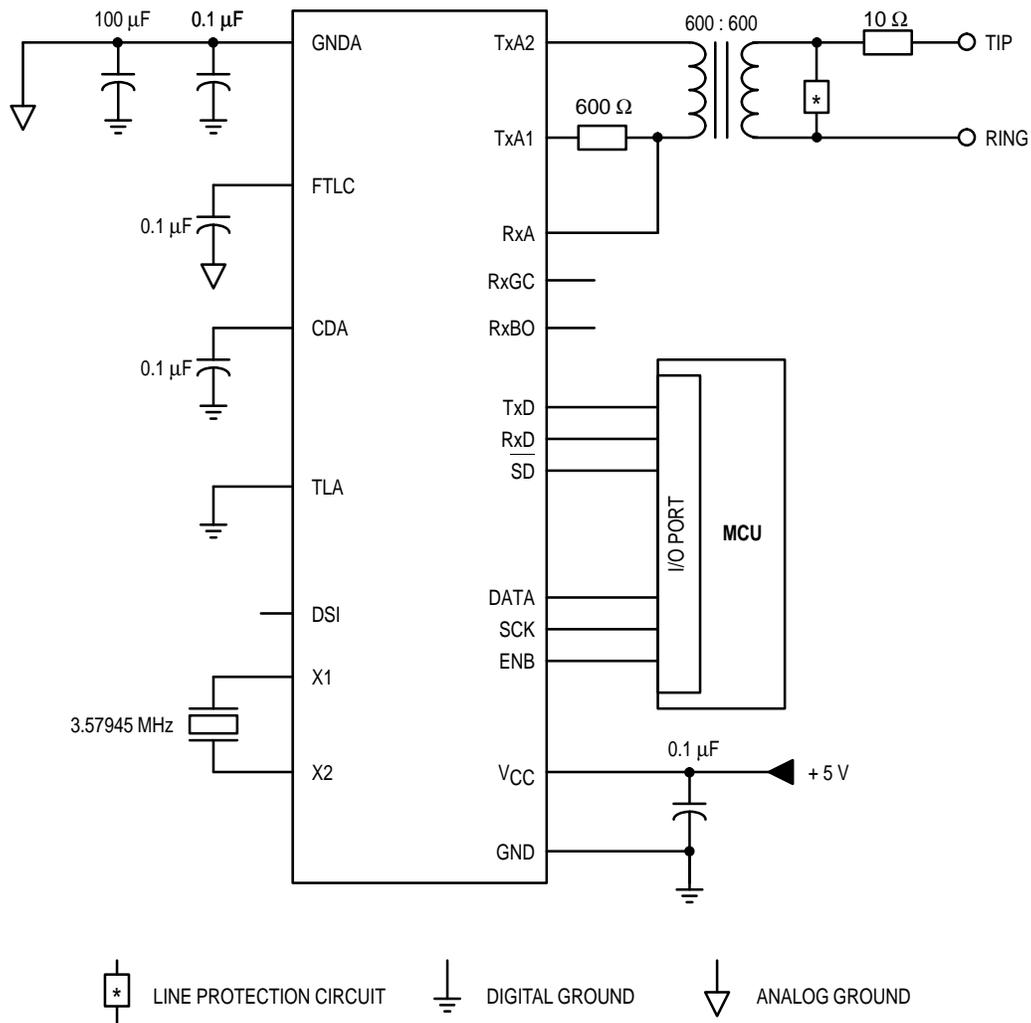
Table 5. Carrier Detect Time Truth Table

CD1	CD0	Carrier Detect Time (Typ)	
		$t_{on}$ (ms)	$t_{off}$ (ms)
0	0	450	30
0	1	15	30
1	0	15	15
1	1	80	10

## POWER-ON RESET

When the power is switched on, this device has the following conditions.

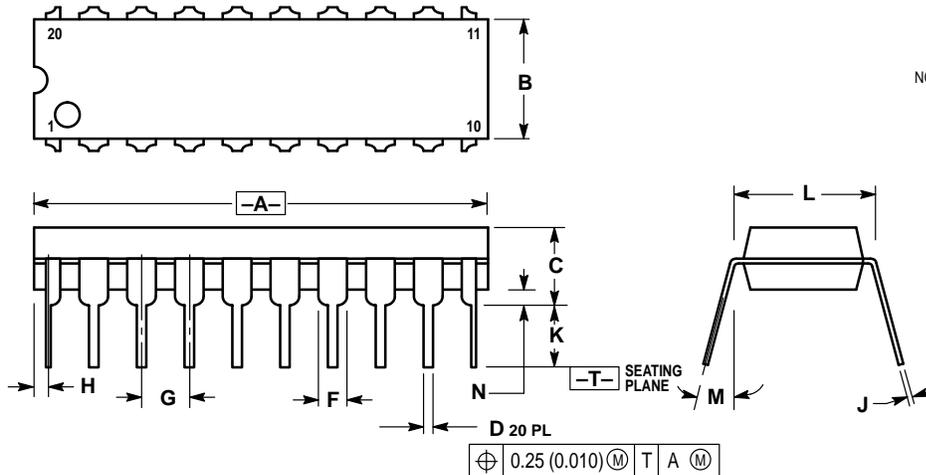
Function Mode	FSK
Transmit Attenuator	0 dB
Transmit Squelch	Enable
Channel	1 (Originate)



**Figure 5. Application Circuit**

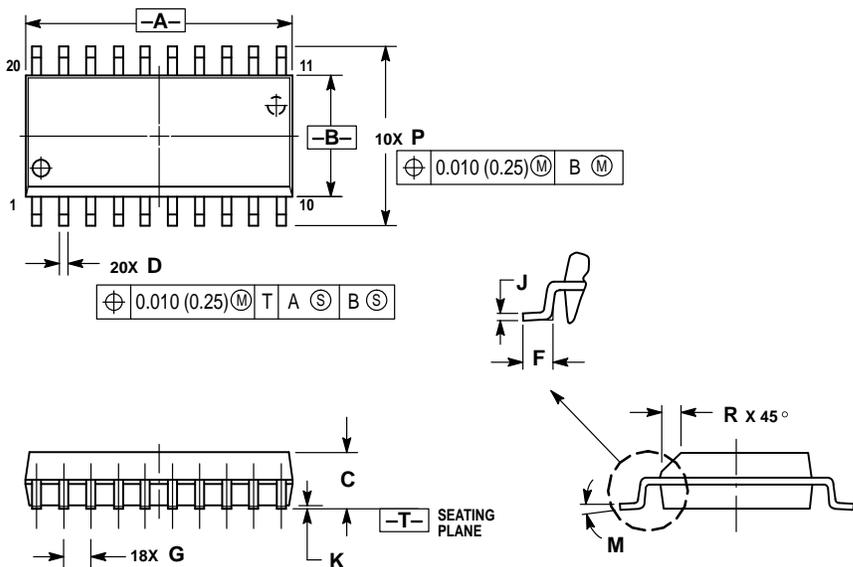
# PACKAGE DIMENSIONS

## H SUFFIX PLASTIC DIP CASE 804-01



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. CONTROLLING DIMENSION: INCH.

## DW SUFFIX SOG PACKAGE CASE 751D-04



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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