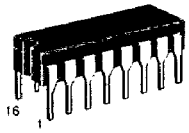
MOTOROLA

MC14583B

DUAL SCHMITT TRIGGER

The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels



L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

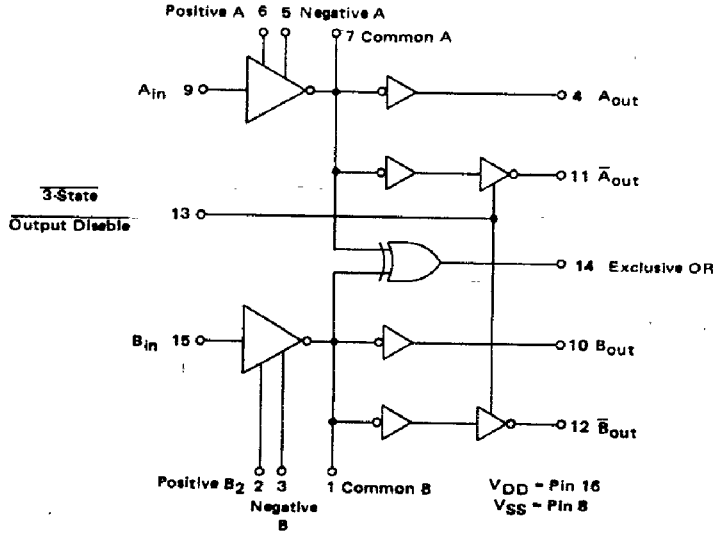
T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

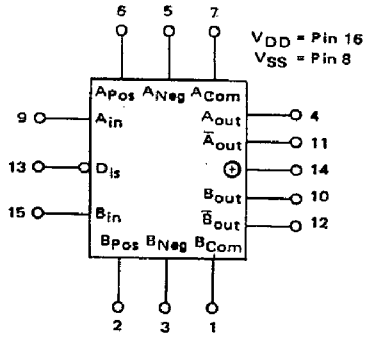
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\bar{A}_{out}$	B_{out}	$\bar{B}_{out}$	⊕
0	0	0	0	Z	0	Z	0
0	0	1	0	1	0	1	0
0	1	0	0	Z	1	Z	1
0	1	1	0	1	1	0	1
1	0	0	1	Z	0	Z	1
1	0	1	1	0	0	1	1
1	1	0	1	Z	1	Z	0
1	1	1	1	0	1	0	0

Z = High impedance at output

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage A and B "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−1.2	—	−1.0	−1.7	—	−0.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.25	—	−0.2	−0.36	—	−0.14	—	
(V_{OH} = 9.5 Vdc)		10	−1.62	—	−0.5	−0.9	—	−0.35	—	
(V_{OH} = 13.5 Vdc)		15	−1.8	—	−1.5	−3.5	—	−1.1	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.33 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.65 μA/kHz) f + I_{DD}							
		15	I_T = (3.98 μA/kHz) f + I_{DD}							
Three-State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

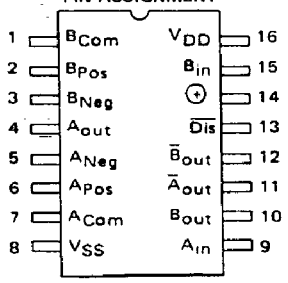
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A_{in}, B_{in} to A_{out}, B_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
A_{in}, B_{in} to A_{out}, B_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1015 ns		5.0	–	1100	2200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 347 ns		10	–	380	760	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 235 ns		15	–	260	520	
A_{in}, B_{in} to Exclusive OR	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns		10	–	280	560	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
3-State Enable, Disable Delay Time (see figure 5)	t_{on}, t_{off}					ns
t_{on}, t_{off} = (1.7 ns/pF) C_L + 140 ns		5.0	–	225	450	
t_{on}, t_{off} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{on}, t_{off} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	
Positive Threshold Voltage (R1, R2 = 5.0 kΩ)	V_{T+}	5.0	–	3.30	–	Vdc
		10	–	5.70	–	
		15	–	8.20	–	
Negative Threshold Voltage (R1, R2 = 5.0 kΩ)	V_{T-}	5.0	–	1.70	–	Vdc
		10	–	4.30	–	
		15	–	6.80	–	
Hysteresis Voltage (R1, R2 = 5.0 kΩ)	V_H	5.0	0.85	1.70	3.40	Vdc
		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	
Threshold Voltage Variation, A to B (R1, R2 = 5.0 kΩ)	ΔV_T	5.0	–	0.1	–	Vdc
		10	–	0.15	–	
		15	–	0.20	–	

*The formulas given are for the typical characteristics only at 25°C.

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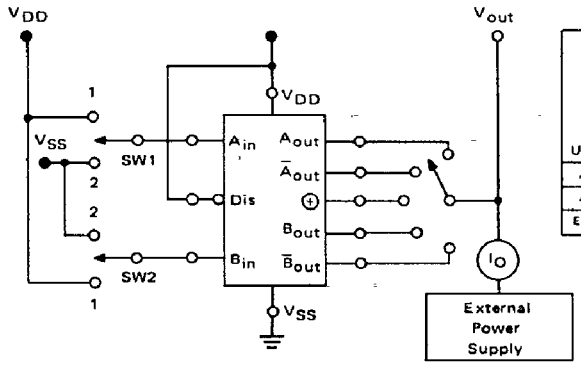
FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

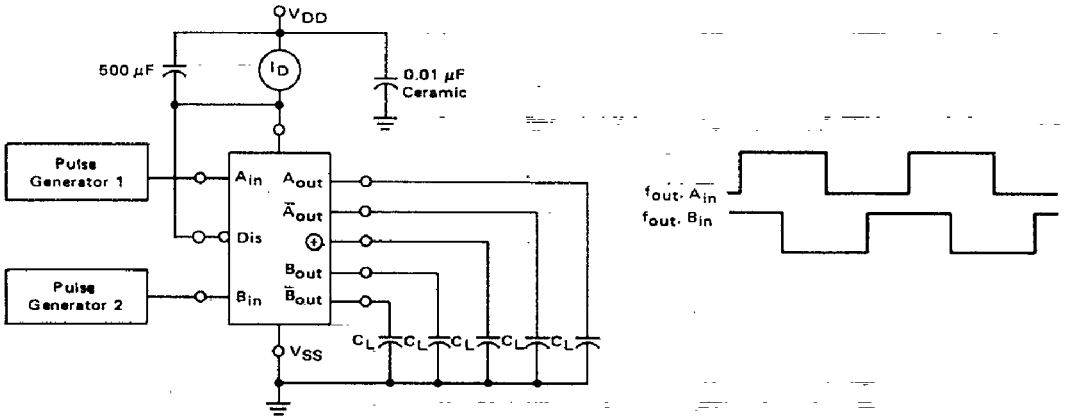
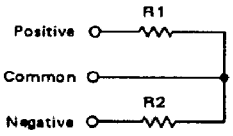
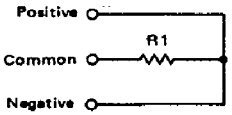


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



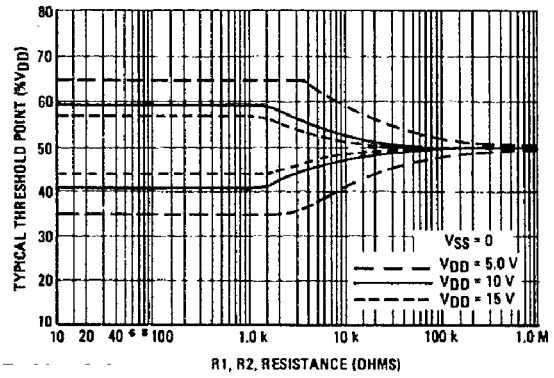
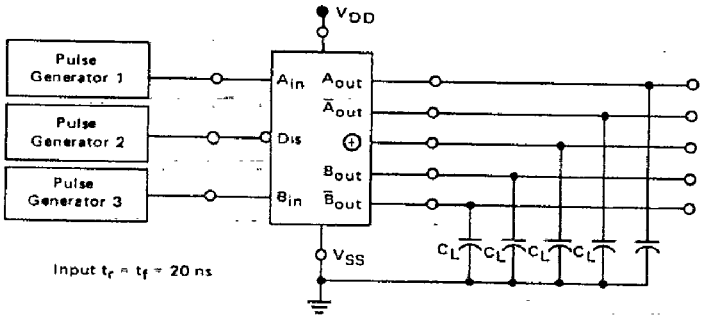
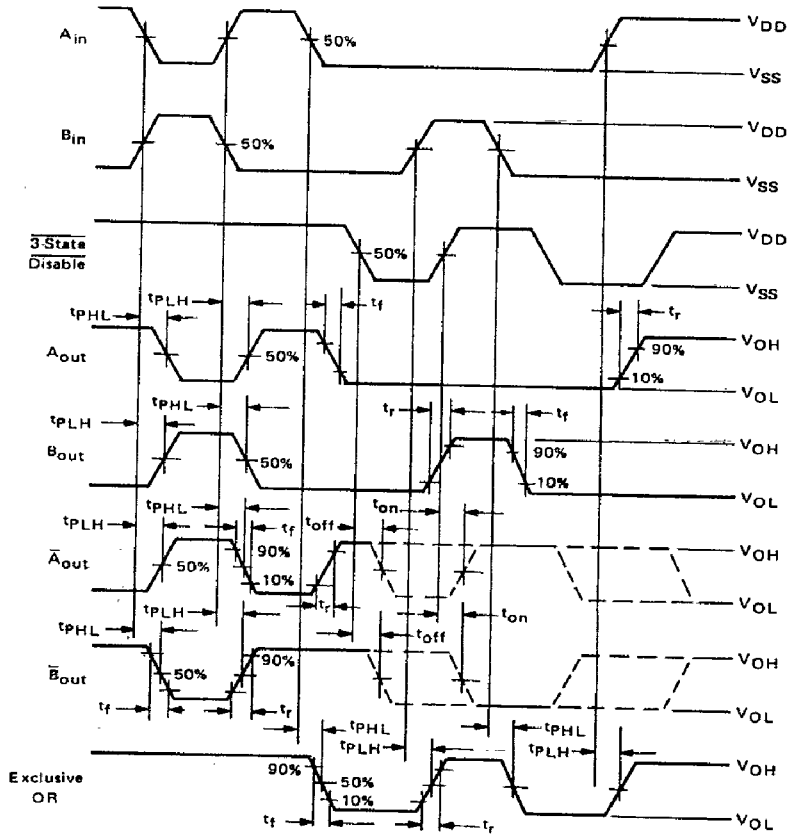


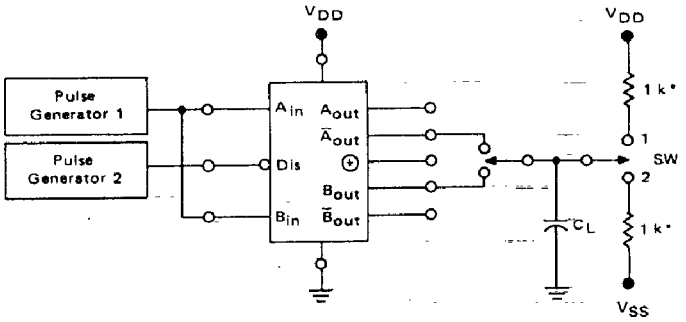
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





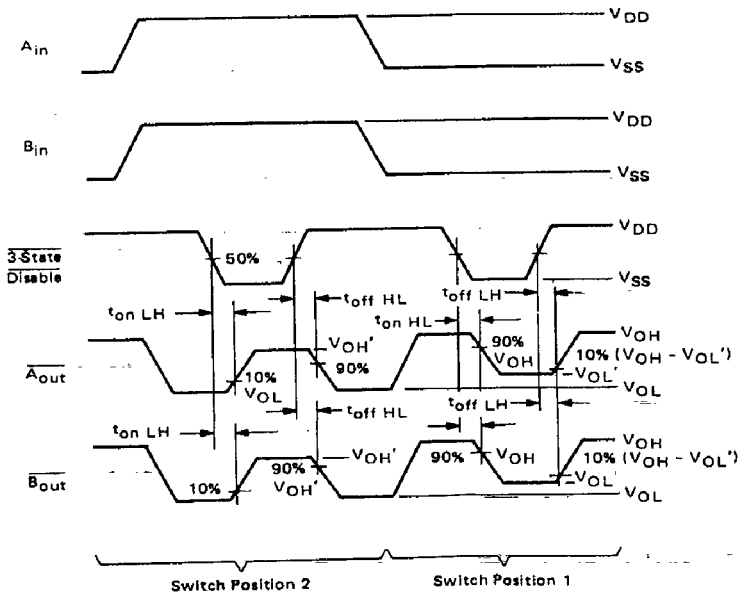
Note: Dashed lines indicate high output resistance

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
$t_{on\ HL}$	1
$t_{on\ LH}$	2
$t_{off\ HL}$	2
$t_{off\ LH}$	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.