MC1519

. . . featuring NPN inputs and PNP outputs. Two monolithic compatible* chips are used to provide a versatile and extremely stable amplifier.

*Compatible — a process utilizing thin film resistors deposited on a silicon monolithic integrated circuit.

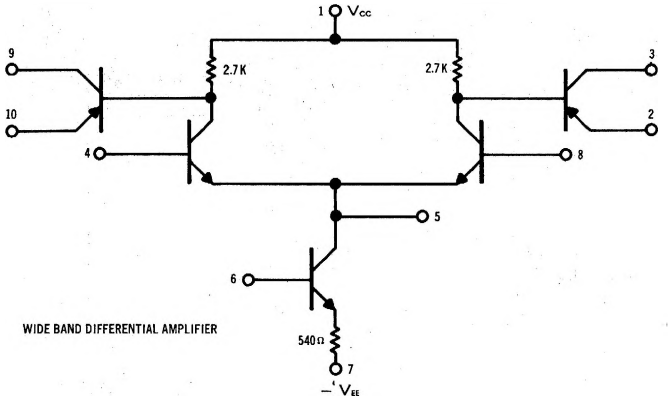
CASE 71

All pins electrically isolated from package

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	Vdc
Power Supply Voltage	V_{EE}	-14	Vdc
Differential Input Signal	V_{in}	±5	Vdc
Total Power Dissipation Derate above 25°C	P_D	300 2.0	mW mW/°C
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

CIRCUIT SCHEMATIC

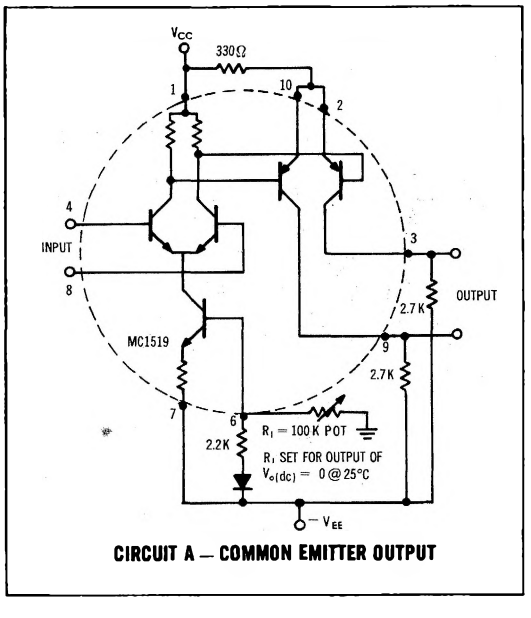


WIDE BAND DIFFERENTIAL AMPLIFIER

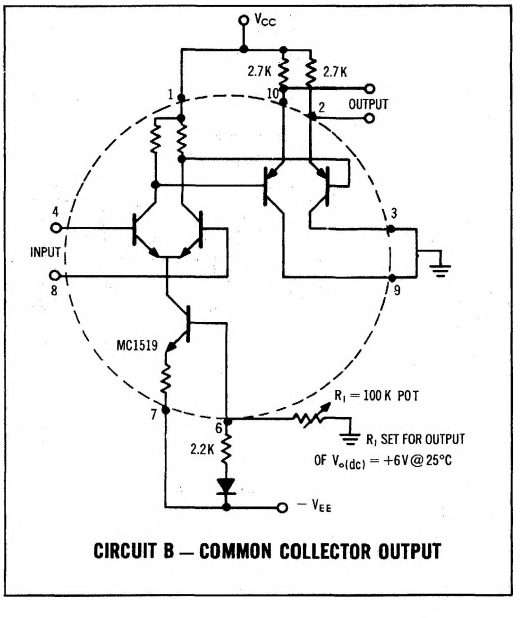
ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = −12 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain Circuit A (CE) Circuit B (CC)	3, 8	A_{dd}	 67 40	 73 45	 79 50	db
Single Ended Voltage Gain Circuit A (CE) Circuit B (CC)	3	A_V	 — —	 67 38	 — —	db
Maximum Output Swing Circuit A (CE) Circuit B (CC)	4	V_O	 12.0 8.0	 14.0 10.0	 — —	$V_{(p-p)}$
Input Offset Voltage Circuit A (CE) Circuit B (CC)	5, 9	V_{IO}	 — —	 2.0 2.0	 6.0 6.0	mVdc
Input Offset Voltage Drift Circuit A (CE) Circuit B (CC)	5, 9	V_{IOD}	 — —	 5.0 5.0	 — —	$\mu V/^oC$
Input Offset Current Circuit A (CE) Circuit B (CC)	6, 10	I_{IO}	 — —	 1.0 2.0	 4.0 8.0	μAdc
Input Current Circuit A (CE) Circuit B (CC)	6, 11	I_i	 — —	 40.0 60.0	 70.0 90.0	μAdc
Common Mode Rejection Circuit A (CE) Circuit B (CC)	7	CM_{Rej}	 — —	 89.0 86.0	 — —	db
Bandwidth - 3 db Circuit A (CE) Circuit B (CC)	3, 12	BW	 0.70 5.0	 1.0 8.0	 — —	mc
Differential Input Impedance Circuit A (CE) Circuit B (CC)	2	Z_{in}	 1.8 —	 2.6 1.2	 — —	kohms
Single Ended Output Impedance Circuit A (CE) Circuit B (CC)	2	Z_{out}	 — —	 2.7 0.048	 — 0.120	kohms

FIGURE 1



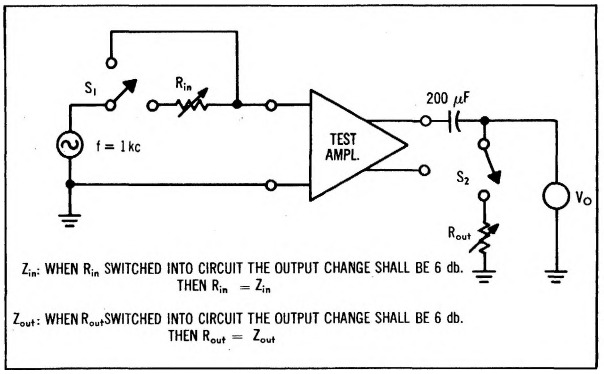
CIRCUIT A — COMMON EMITTER OUTPUT



CIRCUIT B — COMMON COLLECTOR OUTPUT

TEST CIRCUITS

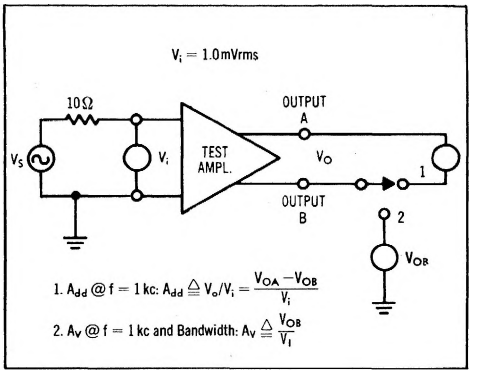
FIGURE 2 — DIFFERENTIAL INPUT IMPEDANCE AND SINGLE-ENDED OUTPUT IMPEDANCE



Z_{in}: WHEN R_{in} SWITCHED INTO CIRCUIT THE OUTPUT CHANGE SHALL BE 6 db. THEN $R_{in} = Z_{in}$

Z_{out}: WHEN R_{out} SWITCHED INTO CIRCUIT THE OUTPUT CHANGE SHALL BE 6 db. THEN $R_{out} = Z_{out}$

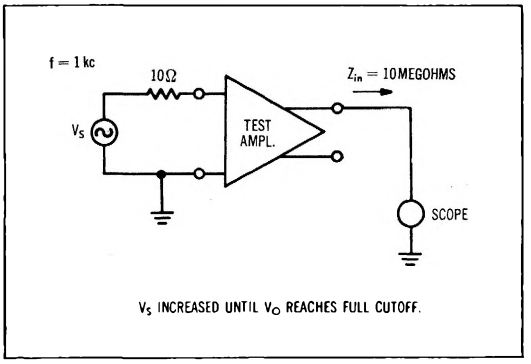
FIGURE 3 — DIFFERENTIAL VOLTAGE GAIN, SINGLE-ENDED VOLTAGE GAIN, and BANDWIDTH



1. A_{dd} @ f = 1 kc: $A_{dd} \triangleq V_o/V_i = \frac{V_{OA} - V_{OB}}{V_i}$

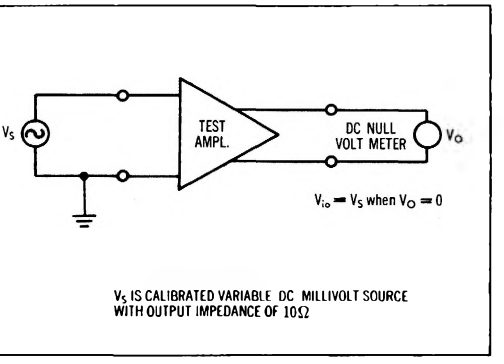
2. A_V @ f = 1 kc and Bandwidth: $A_V \triangleq \frac{V_{OB}}{V_I}$

FIGURE 4 — MAXIMUM OUTPUT SWING



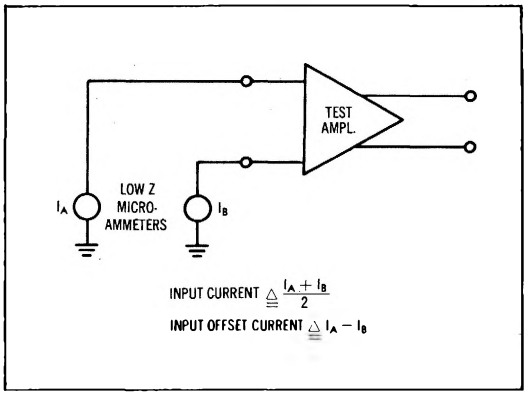
V_S INCREASED UNTIL V_O REACHES FULL CUTOFF.

FIGURE 5 — INPUT OFFSET VOLTAGE



V_S IS CALIBRATED VARIABLE DC MILLIVOLT SOURCE WITH OUTPUT IMPEDANCE OF 10Ω

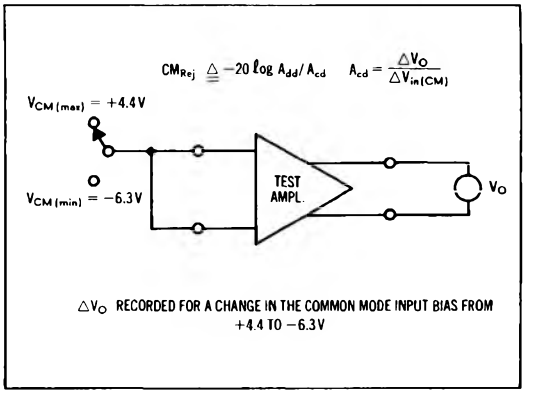
FIGURE 6 — INPUT OFFSET CURRENT and INPUT CURRENT



INPUT CURRENT $\triangleq \frac{I_A + I_B}{2}$

INPUT OFFSET CURRENT $\triangleq I_A - I_B$

FIGURE 7 — COMMON MODE REJECTION



ΔV_O RECORDED FOR A CHANGE IN THE COMMON MODE INPUT BIAS FROM +4.4 TO −6.3 V

EFFECT OF TEMPERATURE ON CIRCUIT B CHARACTERISTICS

R, SET FOR $V_{O(CM)} = +6V$ AT +25°C

FIGURE 8 — DIFFERENTIAL MODE GAIN

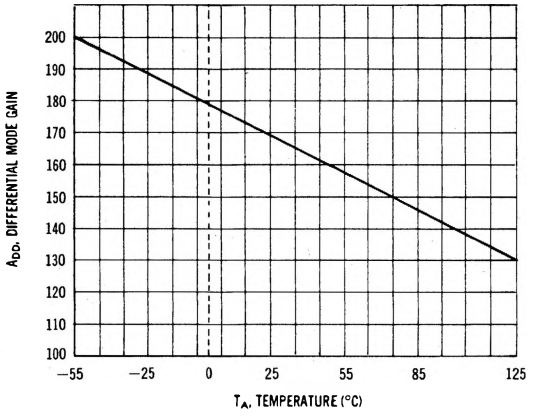


FIGURE 9 — INPUT OFFSET VOLTAGE

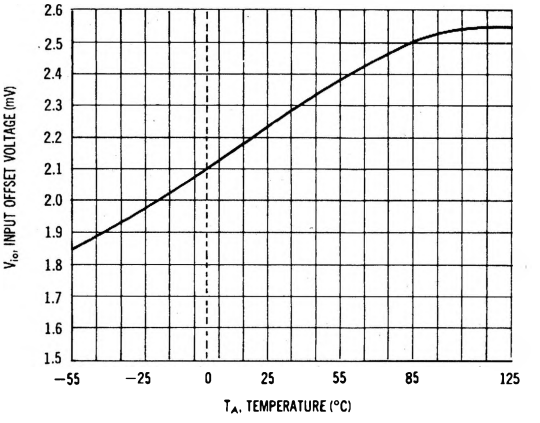


FIGURE 10 — INPUT OFFSET CURRENT

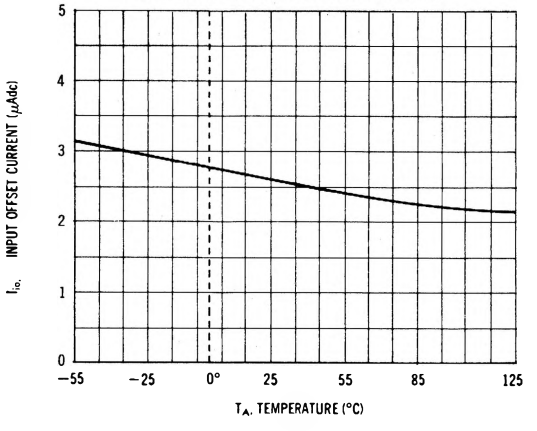


FIGURE 11 — INPUT CURRENT

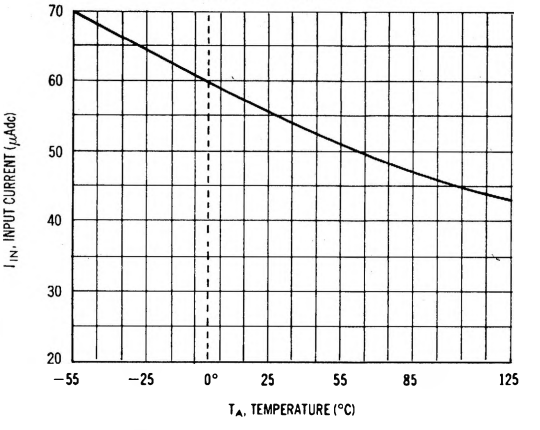


FIGURE 12 — CIRCUIT A BANDWIDTH

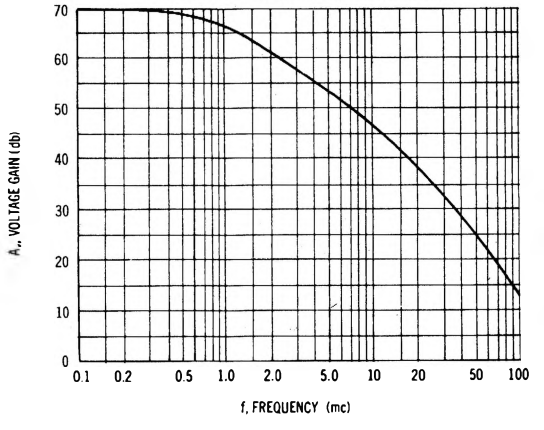


FIGURE 13 — CURRENT SOURCE BIASING