MC1595L
MC1495L

MONOLITHIC FOUR-QUADRANT MULTIPLIER

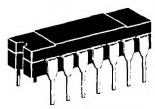
. . . designed for uses where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier

- Excellent Linearity – 1% max error on X-Input, 2% max error on Y-Input – MC1595L
- Excellent Linearity – 2% max error on X-Input, 4% max error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ±10 Volts

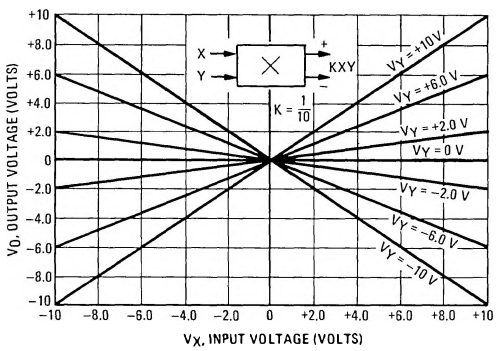
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

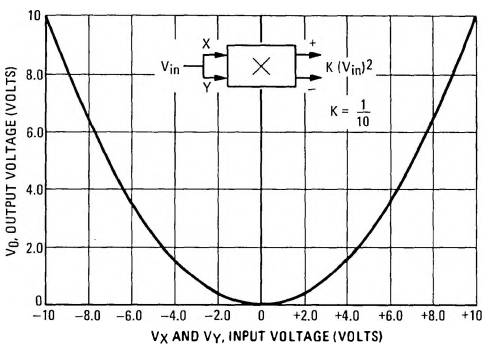


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

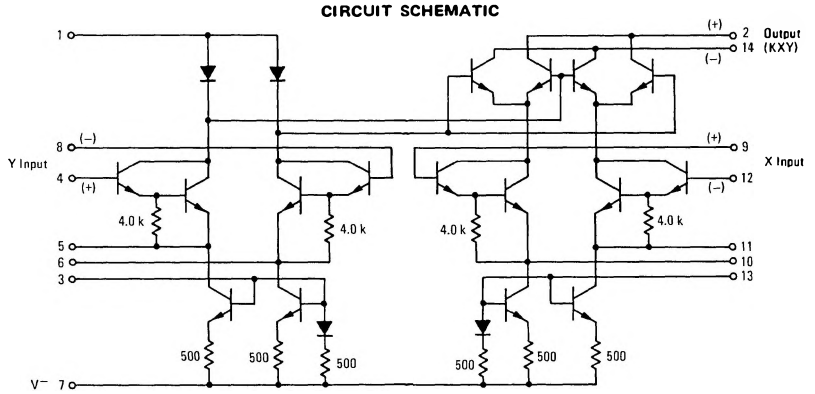
FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



SQUARING MODE TRANSFER CHARACTERISTIC



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

See current MCC1595/1495 data sheet for standard linear chip information.

ELECTRICAL CHARACTERISTICS (V^+ = +32 V, V^- = -15 V, T_A = 25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Figure	Note	Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale: T_A = 25°C		1	4,6					%
-10 < V_X < +10 (V_Y = ±10 V)	MC1495			E_{RX}	–	1.0	2.0	
	MC1595				–	0.5	1.0	
-10 < V_Y < +10 (V_X = ±10 V)	MC1495			E_{RY}	–	2.0	4.0	
	MC1595				–	1.0	2.0	
T_A = 0 to +70°C	MC1495							
-10 < V_X < +10 (V_Y = ±10 V)				E_{RX}	–	1.5	–	
-10 < V_Y < +10 (V_X = ±10 V)				E_{RY}	–	3.0	–	
T_A = -55°C to +125°C	MC1595							
-10 < V_X < +10 (V_Y = ±10 V)				E_{RX}	–	0.75	–	
-10 < V_Y < +10 (V_X = ±10 V)				E_{RY}	–	1.50	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		1	1,5,6,7	E_{SQ}				%
T_A = 25°C	MC1495				–	0.75	–	
	MC1595				–	0.5	–	
T_A = 0 to +70°C	MC1495				–	1.0	–	
T_A = -55°C to +125°C	MC1595				–	0.75	–	
Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$		1	2,7	K	–	0.1	–	–
Input Resistance (f = 20 Hz)	MC1495	2	–	R_{INX}	–	20	–	MegOhms
	MC1595				–	35	–	
	MC1495			R_{INY}	–	20	–	
	MC1595				–	35	–	
Differential Output Resistance (f = 20 Hz)		3	–	R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	4	–	I_{bx}	–	2.0	12	μA
	MC1595				–	2.0	8.0	
	MC1495			I_{by}	–	2.0	12	
	MC1595				–	2.0	8.0	
Input Offset Current $\lvert I_9 - I_{12}\rvert$	MC1495	4	–	$\lvert I_{iox}\rvert$	–	0.4	2.0	μA
	MC1595				–	0.2	1.0	
$\lvert I_4 - I_8\rvert$	MC1495			$\lvert I_{ioy}\rvert$	–	0.4	2.0	
	MC1595				–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		4	–	$\lvert TC_{Iio}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495				–	2.0	–	
(T_A = -55°C to +125°C)	MC1595				–	2.0	–	
Output Offset Current $\lvert I_{14} - I_2\rvert$	MC1495	4	–	$\lvert I_{oo}\rvert$	–	20	100	μA
	MC1595				–	10	50	
Average Temperature Coefficient of Output Offset Current		4	–	$\lvert TC_{Ioo}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495				–	20	–	
(T_A = -55°C to +125°C)	MC1595				–	20	–	
Frequency Response								
3.0 dB Bandwidth		5	9	BW_{3dB}	–	3.0	–	MHz
3° Relative Phase Shift Between V_X and V_Y				f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift				f_θ	–	30	–	kHz
Common Mode Input Swing (Either Input)	MC1495	6	–	CMV	±10.5	±12	–	Vdc
	MC1595				±11.5	±13	–	
Common Mode Gain (Either Input)	MC1495	6	–	A_{CM}	-40	-50	–	dB
	MC1595				-50	-60	–	
Common Mode Quiescent Output Voltage		1	1,7	V_{o1}	–	21	–	Vdc
				V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		1	7	V_{out}	–	±14	–	V_{peak}
Power Supply Sensitivity		7	3	S^+	–	5.0	–	mV/V
				S^-	–	10	–	
Power Supply Current		1	–	I_7	–	6.0	7.0	mA
DC Power Dissipation		1	8	P_D	–	135	170	mW

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3 R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above 25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	 °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Typical Multiplier Operation

For most applications, the multiplier must be nulled as described in Note 7. If this is not done, dc errors will result which make the multiplier unusable for most applications.

Depending on the maximum input voltage desired and the external circuitry used with this multiplier, several different positive supply voltages are possible as indicated below.

The multiplier is normally used with external circuitry which is designed to remove the common mode output voltage. Four recommended circuits for doing this are shown in Figures 1, 10, 11 and 12. In Figure 1, the multiplier differential output is connected to an XY plotter that provides the common-mode rejection. This circuit is useful for measuring accuracy and linearity and is representative of applications where a differential load can be used. The circuits of Figures 10 and 11 both provide output dc level translation which removes the common-mode voltage and produces a single ended output. An operational amplifier is used in Figures 10 and 11 for level shifting and is more accurate than the discrete circuit of Figure 12. Figure 10 allows operation with maximum inputs of ±10 volts with a +32 V supply and ±5 V maximum inputs with a ±15 V supply. The op-amp circuit has the advantage of being rather simple and relatively temperature insensitive. It has the disadvantage of being frequency limited to about 50 kHz for large signal swings due to the slew rate of the operational amplifier. The circuit of Figure 11 has the full ±10 volt input – yet operates from ±15 V supplies. Figure 12 uses discrete components to perform the level shifting, which makes it very inexpensive, simple, and permits operation at higher frequencies (limited by the 7.5 k ohm resistor and stray capacitance associated with the output). The circuit of Figure 12 has the additional advantage of being able to handle larger input voltages (±10 V) while still operating from ±15 V supplies. This circuit has the disadvantage, however, of being temperature sensitive if the base-emitter junctions of the NPN and the PNP are not matched to track with temperature. This problem can be greatly reduced by using complementary-pair transistors mounted in the same package such as the Motorola MD6100. A second problem with this level shifting circuit is a high output impedance with little current drive capabilities. This problem can be solved by placing an operational amplifier at the output as shown or, if high frequency operation is desired, an emitter follower using a discrete transistor can be used to replace the op-amp.

NOTE 2: Scale Factor Calculation

The differential output voltage of the multiplier is given by:

$$V_{out} = V_{o1} - V_{o2} = \frac{2V_X V_Y R_L}{I_3\left(R_X + \frac{2kT}{qI_{13}}\right)\left(R_Y + \frac{2kT}{qI_3}\right)}$$

$$= K V_X V_Y \qquad \text{(See Figure 1)}$$

where $\frac{kT}{q}$ = 26 mV at 25°C. The scale factor, K, (usually $\frac{1}{10}$) can be adjusted with a suitable choice of I_3, R_X, R_Y and R_L as described in Note 11.

Note that the value given for R_3 in Figures 10 to 13 is approximate; it should be adjusted to set the I_3 which will provide the exact gain (K-factor) desired. Note that I_3 not only controls the K-factor, but also controls the signal handling capability of the Y input and the voltage at pin 1 (relating to output swing capability). Its range should therefore be limited to small adjustments about the quiescent current value. For larger adjustments see Note 10 on R_L selection.

NOTE 3: Power Supply Sensitivity

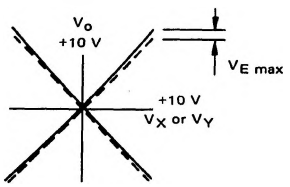
In some cases, it may be desirable to provide separate power supply regulation for I_3, since the multiplier gain is directly dependent on this current.

NOTE 4: Linearity

Linearity is measured for V_X and V_Y separately using an X-Y plotter with the circuit as shown in Figure 1. It is defined to be the maximum deviation of output voltage from a straight line transfer function expressed as error in percent of full scale; see figure below. For example, if the maximum deviation, $V_{E(max)}$, is 100 mV and the full scale output is 10 V, then the error is:

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10\ V} \times 100 = 1\%$$

To measure this, the X-Y plotter is set up first to plot V_{out} versus V_X in all four quadrants ($V_Y = \pm 10$ V, -10 V $\leq V_X \leq +10$ V) then V_{out} versus V_Y ($V_X = \pm 10$ V, -10 V $\leq V_Y \leq +10$ V). The maximum deviations for X and Y are then determined as shown below. It is desirable, but not necessary, to "zero out" the multiplier static error (see Note 7) before making this test.



NOTE 5: Squaring Mode Accuracy is defined as the maximum absolute deviation from a square law curve expressed as a percent of full scale output. This deviation may be measured by connecting the X and Y inputs together (squaring mode) and plotting output versus input, -10 V $\leq V_X = V_Y \leq +10$ V, using an X-Y plotter as shown in Figure 1. Before performing this test, the multiplier static error must be "zeroed out" as in Note 7.

NOTE 6: Sources of Multiplier Error

a. The major source of error in the multiplier arises from voltage offsets and ohmic base resistances in the four output transistors and the base diodes. The static error adjustment procedure described in Note 7 removes as much of this error as possible by offsetting the input differential amplifiers to compensate for the output unbalance.

b. A second and usually small source of error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figure 8 shows the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

c. Care must also be taken to avoid aging and temperature drift in the external components used with the multiplier. This is especially important in the level translation circuitry of Figures 10, 11, and 12.

d. At high frequencies, relative phase differences between the X and Y channels will cause errors in the output product as discussed in Note 9.

NOTE 7: Static Error and Scale Factor Adjustment Procedure

To obtain usable absolute output accuracy, several adjustments must be made in the external multiplier circuitry. For small inputs, the differential output voltage for a typical unadjusted multiplier may be written as:

$$V_{out} = K(V_X \pm \phi X \pm V_{X\ offset})(V_Y \pm \phi Y \pm V_{Y\ offset}) \pm V_{o\ offset}$$

Where ϕX is an equivalent X input offset term

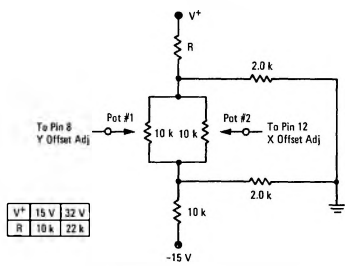
ϕY is an equivalent Y input offset term

$V_{o\ offset}$ is an output offset that remains after the inputs are zeroed.

Following are three different adjustment procedures requiring:

1. an ac voltmeter or oscilloscope (Procedure I)
2. a digital voltmeter (Procedure II)
3. an X-Y plotter (Procedure III)

Each procedure allows the X and Y inputs to be "zeroed" first by setting $V_{X\ offset} = -\phi X$ and $V_{Y\ offset} = -\phi Y$. Next $V_{o\ offset}$ is removed by an output adjustment and K is adjusted for the correct gain. For these procedures the X, Y offset adjust circuitry shown below should be used.



Procedure I (AC Voltmeter or Oscilloscope)

A. X-Y Offset Adjust

1. Connect an ac voltmeter or oscilloscope to the output.
2. Connect 1.0 kHz, 1.0 V_{p-p} oscillator to Y input, ground X input, adjust X offset for an output null.
3. Connect 1.0 kHz, 1.0 V_{p-p} oscillator to X input, ground Y input, adjust Y offset for an output null.

B. Output Offset Adjust

1. For the circuits of Figures 10, 11, and 12, adjust "output offset adjust" potentiometers for zero output.

C. Scale Factor Adjust

1. Set $V_X = +5.0$ Vdc, $V_Y = +5.0$ Vdc and adjust gain potentiometer (I_3) for +2.5 Vdc out.
2. To check, let $V_X = -5.0$ Vdc, $V_Y = -5.0$ Vdc and check for +2.5 Vdc out — if error occurs repeat steps A, B and C.

Procedure II (Digital Voltmeter)

A. X-Y Offset Adjust

1. Set $V_X = V_Y = 0$ volts. Adjust output offset potentiometer until the output reads zero volts.
2. Set $V_X = 5.000$ volts, $V_Y = 0.000$ volts and ad-

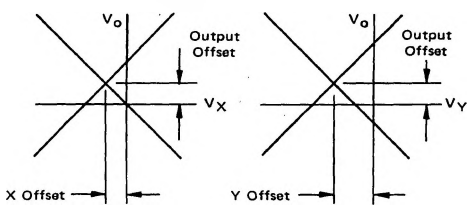
just the Y input offset potentiometer until output reads zero volts.

3. Set V_Y = 5.000 volts, V_X = 0.000 volts and adjust the X input offset potentiometer until output reads zero volts.
4. Repeat step 1.
5. Set $V_X = V_Y$ = 5.000 volts and adjust the K factor potentiometer until output reads +2.500 volts ($K = \frac{1}{10}$).
6. Set $V_X = V_Y$ = -5.000 volts and note the output. The output should again be +2.500 volts. If the error is appreciable (greater than 1 or 2 percent), repeat steps 1 thru 6.

Procedure III (X-Y Plotter)

A. X-Y Offset Adjust

1. Connect X-Y plotter to multiplier.
2. Plot V_{out} versus V_Y (V_X = ±10 V, $-10 \leq V_Y \leq +10$ V) and V_{out} versus V_X (V_Y = ±10 V, $-10\ V \leq V_X \leq +10$ V).
3. See example curves below for X offset, Y offset and output offset.



4. Adjust X and Y offset to bring the above values to zero.

B. Output Offset — See Procedure I-B for methods to bring output offset to zero

C. See Procedure I-C.

When a high degree of accuracy is unnecessary, the adjustment procedure can be simplified by eliminating the V_o offset adjust. This normally results in a small (percentage) error for large output voltages, but a larger (percentage) error near zero.

NOTE 8: Power Dissipation

Because this circuit has no direct positive power supply connections, power dissipation, (P_D), within the actual IC package should be calculated as the sum of the voltage-current products at each port (ignore base current).

Under normal operating conditions, it is valid to assume:

$I_2 = I_{14} = I_{13}$, $I_1 = 2I_3$, and $V_2 = V_{14}$

then

$$P_D = 2(V_2 - V_7)I_{13} + 2(V_1 - V_7)I_3 + (V_{13} - V_7)I_{13} + (V_3 - V_7)I_3$$

For the circuit in Figure 1, calculate:

$$P_D = 2(36)(10^{-3}) + 2(29)(10^{-3}) + (1.2)(10^{-3}) + (1.2)(10^{-3}) = 133\ mW$$

NOTE 9: Bandwidth and Phase

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband op-amp should be used.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

NOTE 10: General Design Procedure

The method used to calculate the element values for the first entry in the table in Figure 10 is given below. This will illustrate a general design procedure. For this example, the inputs, outputs and scale factor are:

$$V_{out} = V_X V_Y/10,\ -10\ V \leq V_X \leq +10\ V$$

$$-10\ V \leq V_Y \leq +10\ V,\ K = 1/10$$

Design Procedure (See Figure 1):

a. Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

$$V_{X(max)} < I_{13} R_X$$

$$V_{Y(max)} < I_3 R_Y$$

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega$$

In order to insure that $R_X >> \frac{kT}{qI_{13}}$ and $R_Y >> \frac{kT}{qI_3}$ even with maximum input voltage, let $R_X = R_Y$ = 15 kΩ (see Note 6b and Figure 8).

b. Then from Note 2 the scale factor is approximately:

$$K \approx \frac{2R_L}{I_3 R_X R_Y}$$

and R_L is established for K = 1/10:

$$R_L = \frac{K I_3 R_X R_Y}{2} = \frac{(10^{-3})(15 \times 10^3)(15 \times 10^3)}{(10)(2)}$$

$$= 11.25\ k\Omega$$

Select R_L = 11 kΩ.

c. The supply voltages are now selected. From the curve in Figure 9, for an input swing of ±10 V, voltage V_1 may have a minimum value of +12 volts. (This minimum V_1 is approximately two forward diode drops above $V_{X\ max}$ and one diode drop above $V_{Y\ max}$.) With a 1.5 volt safety margin, V_1 becomes 13.5 V. This voltage can be supplied by a separate power supply or obtained by a dropping resistor, R_1, from the positive supply according to the equation:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

The positive supply is determined from:

$$V^+ = V_1 + \left[\frac{K V_{X\ max} V_{Y\ max}}{2}\right] + I_{13} R_L + 2\ V\ \text{(safety margin)}$$

$$= 13.5 + 5 + 11 + 2\ V$$

$$= 31.5\ \text{(select nominal +32 V supply)}$$

Now R_1 can be found:

$$R_1 = \frac{V^+ - V_1}{2I_3} = \frac{32 - 13.5}{(2)(1.0\ mA)} = 9.25\ k\Omega$$

Select R_1 = 9.1 kΩ.

The negative supply should be selected so that with maximum positive input voltage applied, the maximum voltage between the input and the negative supply does not exceed the 30 V breakdown limit. In addition, the negative supply should be at least two volts more negative than the most negative input voltage. For V_{in} max (negative) = -10 V, select V^- = -15 V.

d. The currents I_{13} and I_3 are set by means of dropping resistors from ground to pins 13 and 3 respectively, according to the equations.

$$R_{13} = \frac{V_7 - \phi}{I_{13}} - 500\Omega$$

where $\phi = V_{BE} = 0.75$ at 25°C.

$$\text{Similarly: } R_3 = \frac{V_7 - \phi}{I_3} - 500\Omega$$

for $I_{13} = I_3$, $R_3 = R_{13} = 13.75\ k\Omega$

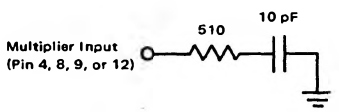
e. The common-mode voltage, V_{CM}, may be calculated from:

$$V_{CM} = V^+ - R_L I_{13} = 32 - 11 = 21\ V.$$

NOTE 11: Parasitic Oscillation

When long leads are used on the input, oscillation may occur. In this event, an R-C parasitic suppression network similar to the one shown below should be connected directly to each input using short leads. The purpose of the network is to reduce the Q of source-tuned circuits which cause the oscillation.

Another technique which is also adequate in most applications is to insert a 510Ω resistor in series with the multiplier inputs, pins 4, 8, 9, and 12.



TEST CIRCUITS

FIGURE 1 – TEST CIRCUIT FOR LINEARITY AND ACCURACY MEASUREMENT USING X-Y PLOTTER

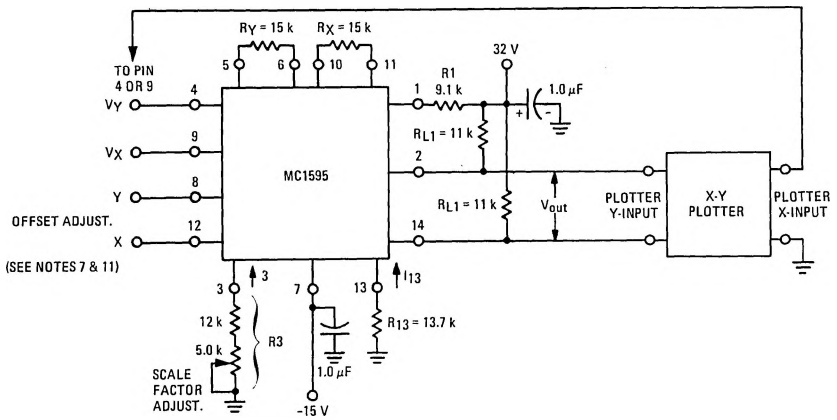


FIGURE 2 – INPUT RESISTANCE MEASUREMENT

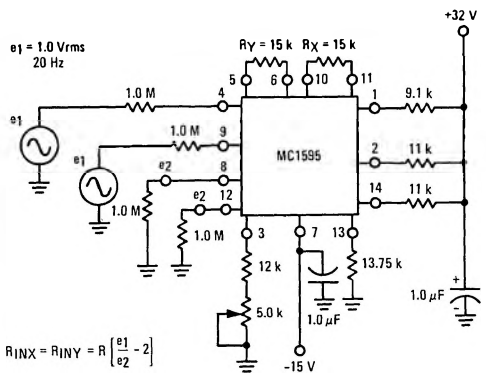


FIGURE 3 – OUTPUT RESISTANCE MEASUREMENT

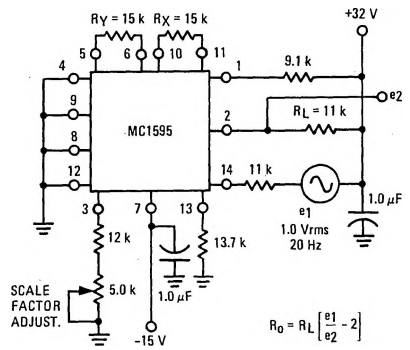


FIGURE 4 – INPUT AND OUTPUT CURRENT MEASUREMENT

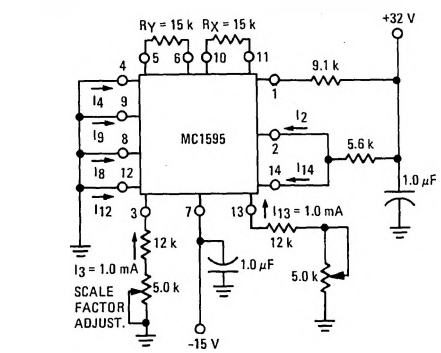
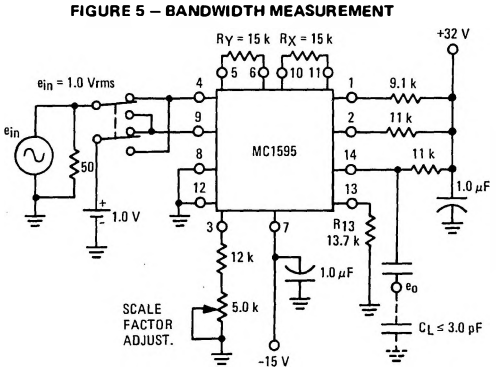


FIGURE 5 – BANDWIDTH MEASUREMENT



TEST CIRCUITS (Continued)

FIGURE 6 – COMMON MODE INPUT VOLTAGE AND GAIN MEASUREMENT

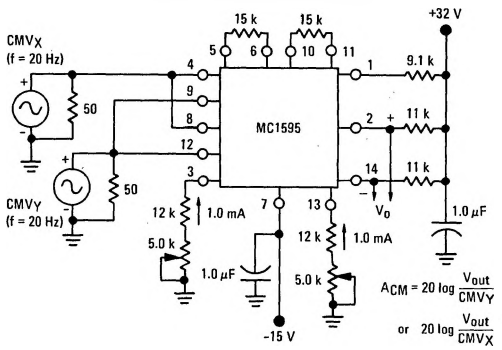
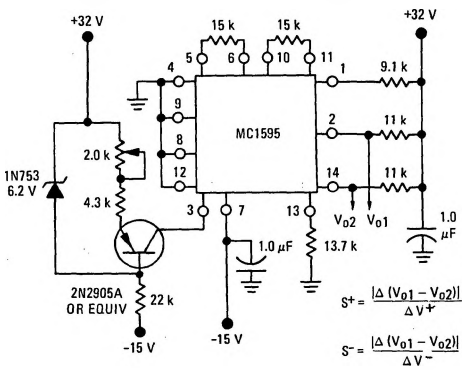


FIGURE 7 – POWER SUPPLY SENSITIVITY



TYPICAL CHARACTERISTICS

FIGURE 8A – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

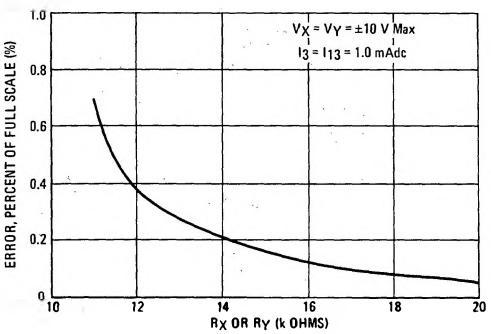


FIGURE 8B – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

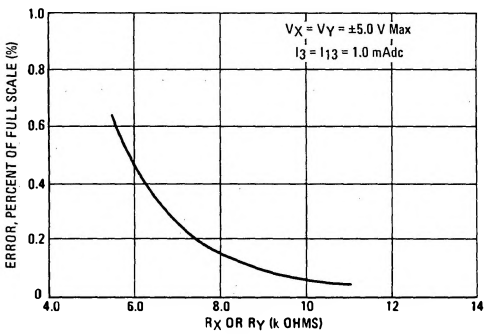
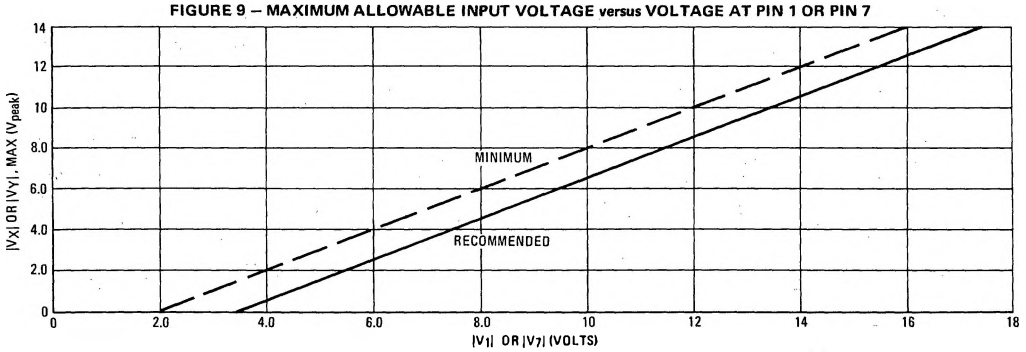
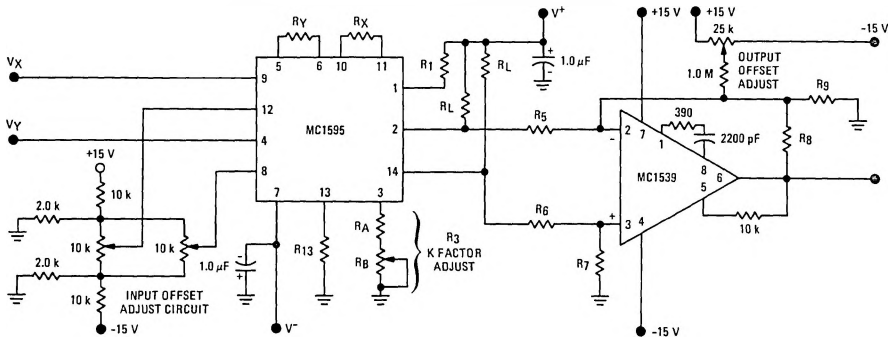


FIGURE 9 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



TYPICAL APPLICATIONS

FIGURE 10 – MULTIPLY WITH OP-AMP LEVEL SHIFT



RESISTOR	R_1	R_5	R_6	R_7	R_8	R_9	R_{13}	R_A	R_B	R_L	R_X	R_Y
UNIT	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ
TOLERANCE	5%	1%	1%	1%	1%	1%	1%	5%	20%	0.5%	5%	5%
V^+ = +32 Vdc, V^- = -15 Vdc -10 V ≤ V_X ≤ +10 V, 10 V ≤ V_Y ≤ +10 V	9.1	121	100	11	121	15	13.7	12	5.0	12	15	15
V^+ = +15 Vdc, V^- = -15 Vdc -5 V ≤ V_X ≤ +5 V, -5 V ≤ V_Y ≤ +5 V	3.0	300	100	100	300	∞	13.7	12	5.0	3.4	8.2	8.2

FIGURE 11 – MULTIPLY WITH OP-AMP LEVEL SHIFT

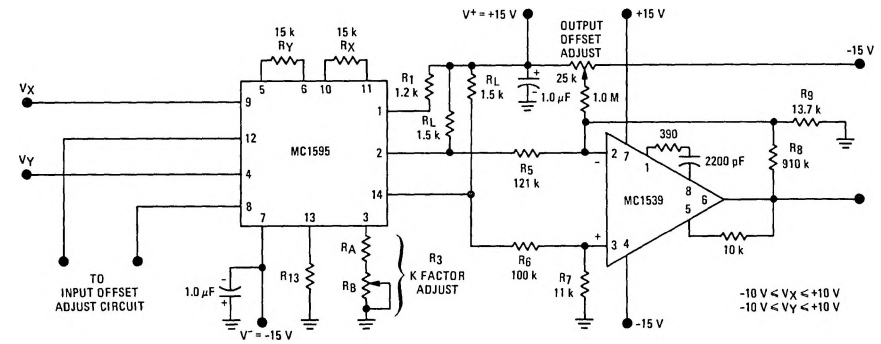
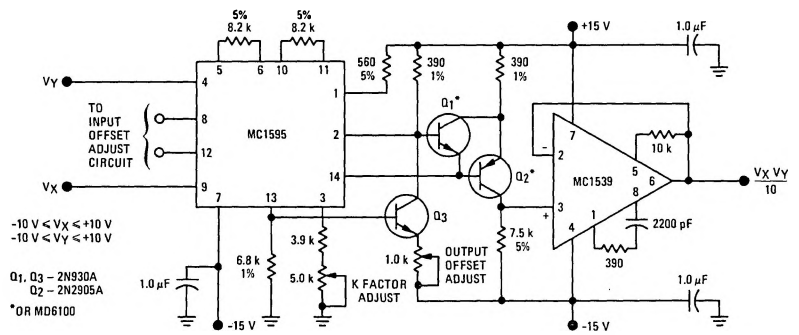


FIGURE 12 – MULTIPLY WITH DISCRETE LEVEL SHIFT



TYPICAL APPLICATIONS (continued)

FIGURE 13 – DIVIDE AND SQUARE ROOT

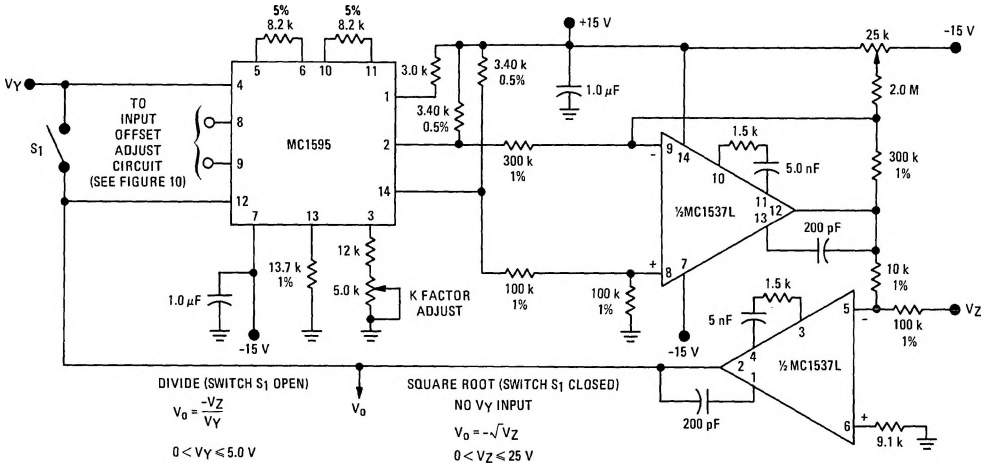


FIGURE 14 – FREQUENCY DOUBLER

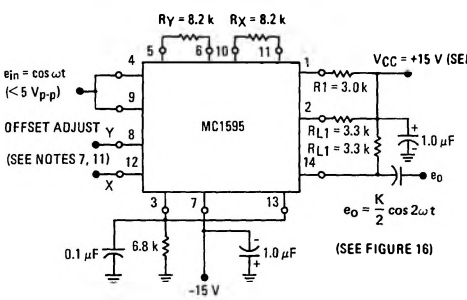


FIGURE 15 – BALANCED OR AMPLITUDE MODULATOR

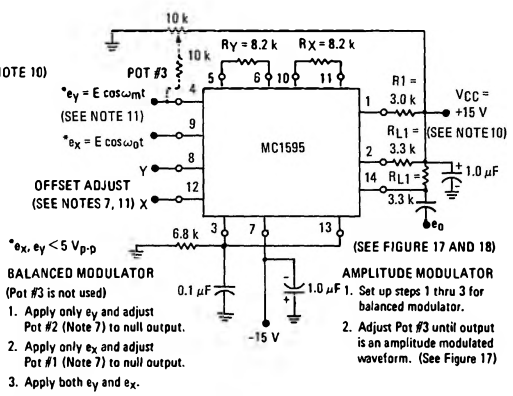


FIGURE 16 – FREQUENCY DOUBLER (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 14)

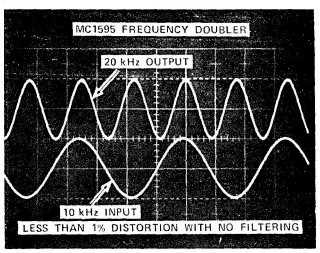


FIGURE 17 – AMPLITUDE MODULATOR (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 15)

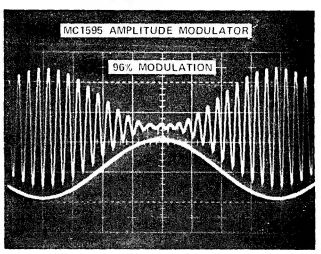


FIGURE 18 – BALANCED MODULATOR (OUTPUT WAVEFORM OF CIRCUIT SHOWN IN FIGURE 15)