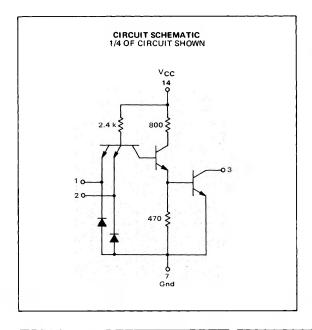
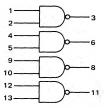
QUAD 2-INPUT "NAND" GATE (Open Collector)

MC3100/MC3000 series

MC3104F • MC3004F MC3104L • MC3004L,P



This device consists of four 2-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR-function is required or for driving discrete components.



Positive Logic: $3 = 1 \cdot 2$ Negative Logic: 3 = 1 + 2

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 88 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

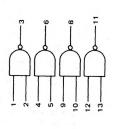
Pin numbers for the 54H01F/74H01F device are shown in the chart. These devices are available on special request.

DEVICE		PIN NUMBERS													
MC3104F,L/3004F,L,P		2	3	4	5	6	7	8	9	10	11	12	13	14	
54H01F/74H01F		2	3	6	7	5	11	œ	9	10	14	12	13	4	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS 2.5 Vdc 9 Vcc TPout t+ 7.0 ns t-7.0 ns € 280 10% PULSE -tod+ GENERATOR ≥2.4 V PRF = 1.0 MHz typ PW = 50% Duty Cycle 木 CT 50 ≤0.4 V t+ = 7.0 ns Gnd t- = 7.0 ns CT = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



TEST CURRENT / VOLTAGE VALUES

Volts

μA

@ Test

V _{IHX}		2.5			2.5				V _{IHX} Gnd	- 7*	2,7*	2,7*	* 4	*4	*4	1, 2, 4, 5, 7, 9, 10, 12, 13	7	- 1, 2, 4, 5, 7, 9, 10, 12, 13		2 7*	2 7*
V _{ссн} V	5.5	5.5	5.5	5.25	5.25 2	5.25		-	V _{CCH} V	-	14	14			,		14	14	-		
Vccı	4.5	4.5	4.5	4.75	4.75	4.75		+	V _{CCL}	14		1	14	14	14					,	-
V _{CC}	5.0	5.0	5.0	5.0	5.0	5.0	. A		V _{CC}	-	,	,		1,		1	,	,		4	1.4
V		7.0			7.0		STED BE		V _{max}	,	,					14					
Vcex	5.5	5.5	5.5	5.5	5.5	5.5	PINS	VULIAGE APPLIED TO PINS LIS	VCEX		,		-	-	8	,		,			
VRH	4.0	4.0	4.0	4.0	4.0	4.0	EST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW		V _{RH}	23				2	1.	1	1, 2, 4, 5, 9, 10, 12, 13	1			
>	2.4	2.4	2.4	2.5	2.5	2.5			>"		-		-	- (,	,		,			
>"	0.4	0.4	0.4	0.4	9.0	9.0	URRENT		>"	7		1			,	,	ı	i			
>=	2.0	1.8	1.8	2.0	1.8	1.8	TEST		>=		'			-	63	,	,	, .		,	
>=	1.1	1.1	9.0	1.1	1.1	0.9		-	>=	<u>'</u>	'				-	,	'	'		'	-
_0	'	-10	'	,	-10	,		-	-	<u> </u>	-	1	-	'	'	'	-	1		'	-
_5	_	1.0	'	'	1.0			1	_5		'	-	'	'	1	'	'	'	Pulse	m	1
_ <u>ō</u>	20	20	20	20	20	20			_6					m	,	,	,	,	Pulse In	-	
Temperature	−55°C	+25°C	+125°C	0 0	+25°C	+75°C			Unit	mAde	μAdc	Vdc	Vdc	Vdc	μAdc	mAdc	mAdc	mAdc		su	
Temp	•	MC3104	_	_	MC3004 {			+75°C	Max	-2.0	20		i	4.0	250	1	36	10		•	
		WC			W		nits	+	Win		1.		,	,	٠.	,	1			1	
							MC3004 Test Limits	+25°C	Max	-2.0	20		-1.5	9.0	250	25	36	10		14	
							C3004	+2	Min	1	'	5.5		'		, .	'	'		1	
							ž	0,0	Max	-2.0	20		,	6.4	250		36	10		1	
						-		0	Min	'			,	,		1	'			1	
								+125°C	Max	-2.0	20	,		0.4	250	. 1	36	10		,	
							Limits	Ŧ	Min	,	,				•	1		. '		1	
								+25°C	Max	-2.0	20	1	-1.5	4.0	250	55	36	10		14	00
						MC3104 Test	+2	Win	- 1	'	5.5		2.						•		
							¥	−55°C	Max	-2.0	20			0.4	250	1	36	10		,	
					Ц.		Min		,	,	,	1	1.	'		-		1	L		
								Ilnder	Test	7	7	1	1	m	က	14	14	14		1,3	0.5
									Symbol	ď	I _R	BVin	ο _D	VOL	LCEX	Imax	нач	IPDL	10. A	-pd ₁	
									Characteristic	Input Forward Current	Leakage Current	Breakdown Voltage	Clamp Voltage	Output Output Voltage	Output Leakage Current	Power Requirements (Total Device) Maximum Power Supply Current	Power Supply Drain		Switching Parameters	Turn-On Delay	Turn-Off Dolou

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.