

## MC3100/MC3000 series

**MC3104F • MC3004F**  
**MC3104L • MC3004L,P**  
 (54H01J) (74H01J,N)

The circuit diagram shows three op-amp comparators arranged vertically. The top comparator has its non-inverting input (+) connected to VCC (pin 14) through an 800 Ω resistor and its inverting input (-) connected to pin 1 through a 2.4 kΩ resistor. Its output (pin 3) is connected to the inverting input of the middle comparator. The middle comparator has its non-inverting input (+) connected to VCC through an 800 Ω resistor and its inverting input (-) connected to pin 2 through a 2.4 kΩ resistor. Its output (pin 3) is connected to the inverting input of the bottom comparator. The bottom comparator has its non-inverting input (+) connected to VCC through an 800 Ω resistor and its inverting input (-) connected to pin 7 (Gnd). Its output (pin 3) is connected to the inverting input of the middle comparator. All comparators have their other inputs connected to Gnd (pin 7). Two LEDs are connected between pins 1 and 2 to ground.

The diagram shows four 2-input OR gates connected in parallel. The inputs are labeled 1, 2, 4, 5, 9, 10, 12, and 13. The outputs are labeled 3, 6, 8, and 11.

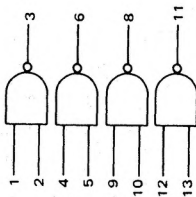
Input Loading Factor = 1  
Output Loading Factor = 10  
Total Power Dissipation = 88 mW typ/pkg  
Propagation Delay Time = 8.0 ns typ

DEVICE	PIN NUMBERS													
MC3104F,L/3004F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H01F/74H01F	1	2	3	6	7	5	11	8	9	10	14	12	13	4

PRF = 1.0 MHz typ  
 PW = 50% Duty Cycle  
 $t_r = 7.0$  ns  
 $t_f = 7.0$  ns

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

[illegible]

\* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.