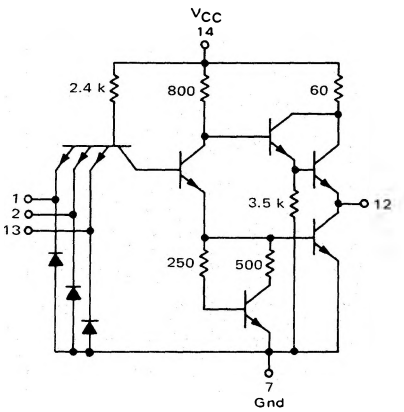
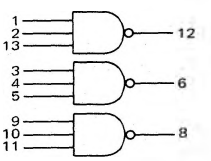
TRIPLE
3-INPUT "NAND" GATE

MC3105F • MC3005F
MC3105L • MC3005L,P
(54H10J) (74H10J,N)

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



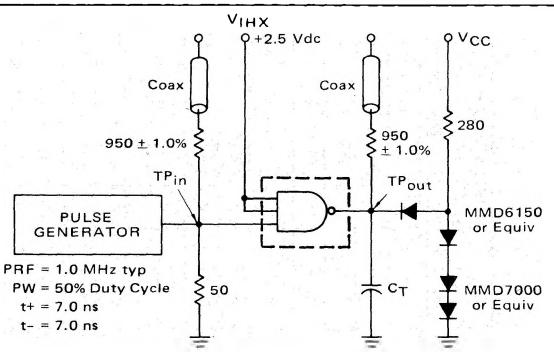
This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.

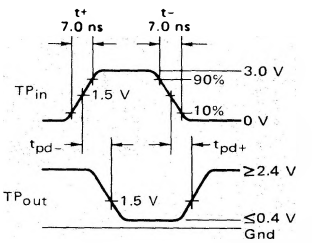


Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





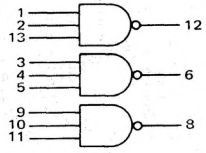
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		I_{OL} mA	I_{OH} mA	I_{in} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{RH} Volts	V_{max} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{IHX} Volts
MC3105	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3005	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3105 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	-	1	-	-	2, 13	-	-	14	-	-	7*
	V_{OH}	12	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	12	-	-	1	-	-	-	2, 13	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	12	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 7,* 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	14	-	30	-	30	-	30	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	-	-	14	-	7
	I_{PDL}	14	-	12.6	-	12.6	-	12.6	-	12.6	-	12.6	-	12.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters Turn-On Delay	t_{pd-}	1, 12	-	-	-	10	-	-	-	-	-	10	-	-	ns	Pulse In 1	Pulse Out 12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*
Turn-Off Delay	t_{pd+}	1, 12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.