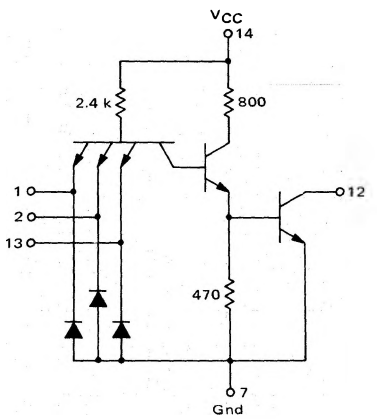
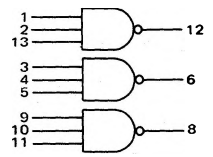
TRIPLE 3-INPUT "NAND" GATE
(Open Collector)

MC3107F • MC3007F
MC3107L • MC3007L,P

CIRCUIT SCHEMATIC
1/3 OF CIRCUIT SHOWN



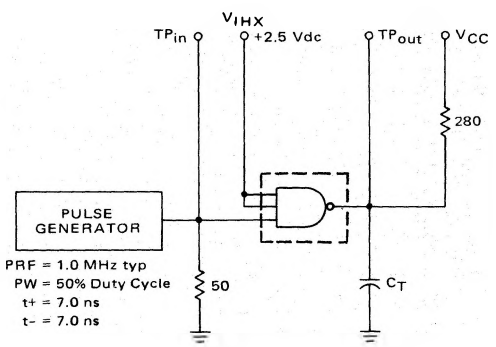
This device consists of three 3-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.

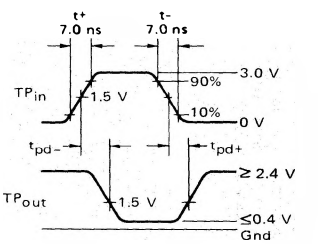


Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$
Negative Logic: $12 = \overline{1 + 2 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



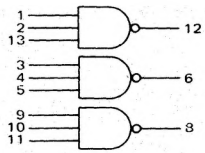


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES														
		mA			Volts											
		I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC3107	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-	
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5	
	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-	
MC3007	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5	
	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	

Characteristic	Symbol	Pin Under Test	MC3107 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3007 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	-	2, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL}	12	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	1	-	-	2, 13	-	-	-	14	-	-	7*
Output Leakage Current	I_{CEX}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2,13	-	-	-	12	-	-	14	-	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	14	-	28	-	28	-	28	-	28	-	28	-	28	mAdc	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	-	-	-	14	-	7
	I_{PDL}	14	-	13.5	-	13.5	-	13.5	-	13.5	-	13.5	-	13.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters Turn-On Delay	t_{pd-}	1, 12	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In 1	Pulse Out 12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*
Turn-Off Delay	t_{pd+}	1, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.