MC3100/MC3000 series

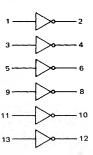
HEX INVERTER

MC3108F • MC3008F MC3108L • MC3008L,P

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN

VCC
14
2.8 k
760
4 k
760
7
Gnd

This device offers six independent inverting gates in a single package. Each gate consists of a single input driving an output inverter.



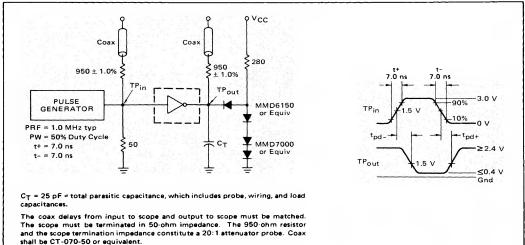
Positive Logic: 2 = 1

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 140 typ/pkg
Propagation Delay Time = 6 ns typ

Pin numbers for the 54H04F/74H04F device are shown in the chart. These devices are available on special request.

DEVICE		-				PIN	NU	MBE	RS					
MC3108F,L/3008F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H04F/74H04F	1	14	3	2	5	6	11	8	7	10	9	12	13	14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

Pin MC3108 Test Limits MC3008 Test Limits M			11	=	1	-10																TE	ST CUR	RENT / VC	TEST CURRENT / VOLTAGE VALUES	UES				
13					۷ ۷										(1		μM							>	olts				
Pin			72	2	1	-12							*		Temp	erature	_6	-F	_ <u>.</u> £	٥	>"	>	>"	>"	V _{RH}	Vmax		Vccı	V _{CCH}	r
Paris Pari															•	-55°C		-2.0		•	1.1	2.0	9.4	2.4	4.0	-	5.0	4.5	5.5	-
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $														W	~	+25°C		-2.0	_	_	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	
Paris Pari															ٺ	+125°C		-2.0	,		0.8	1.8	0.4	2.4	4.0	•	5.0	4.5	5.5	
															_	٥°C		-2.0	_		1.1	2.0	9.0	2.5	4.0		5.0	4.75	5.25	
Physical Pick Physical Pic														W	_	+25°C		-2.0	-	-	1.1	1.8	0.4	2.5	4.0	4.0	5.0	4.75	5.25	_
										-					_	+75°C	20	-2.0	_	,	6.0	1.8	9.0	2.5	4.0	-	5.0	4.75	5.25	
	. W		Pin		×	C3108		mits			2	103008	Test Lin	nits				,			TEST C	URREN	1/00/	AGE APP	LIED TO PIL	VS LISTEL	D BELO	. ×		
Symbol Test Min Max Min			Under	_	-55°C	+	25°C	+	125°C		٥ <u>.</u> 0	+	2°C	+	. 2°C			L				-	-				1	1		
I _R 1 -2.0 -	Characteristic	Symbol	Test	4	Max		-	-	Max	-	-	-	Max	-	Max	Unit	ا _و	_ĕ	_ <u>.</u> E	۵	>"	>=	>"	>"	> RH	> ×	۶	VccL	VCCH	Gnd
Harror H	nput Forward Current	4	-	3	-2.0		-2.0	-	-2. (_	-	_	-2.0	_	-2.0			-			1		-			-	1	Ŀ	14	1.
BV _{III} 1 - - 5.5 - - - 1.5 - - - 5.5 - - - Vdc - - 1 - - - 1 - - -	Leakage Current	IR	1	'	20	1	20	-	20	-	20	'	20	1.	20	μAdc							-			1.			14	*1
VD 1 -	Breakdown Voltage	BVin	-	'	-	5.5	_	1	1	1	-	5.5	-		1	Vdc			-	,			1				-		14	*-
VOL. 2 2.4 - 0.4 -	Clamp Voltage	v _D	1	1	.1 .		-1.5	-	'	1	'	'	-1.5			Vdc			-	-			1				-	14	1	**
VoH 2 2 2.4 - 2.4 - 2.5 - 2.5 - 2.5 - 0.4dc - 100 400 100 40 10 10 10 10 10 10 10 10 10 10 10 10 10	Output Output Voltage	vol.	23	-	0.4	-	0.4		0.4	 			0.4	,	0.4	Vdc	2	'		-	1	-	,	,		,	-	14		**
Secondary Fig. Secondary		МОЛ	2	2.4		2.4	_	2.4		2.5		2.5		2.5	-	Vdc		62			-			,				14	•	**
The control of the	Short-Circuit Current	I _{SC}	2	-40	-	-	-	-	_		1	-	-100		-100	mAdc			1	,		,	,	1 -		,		'	14	1,2,7*
Taylor 14 - 58 - 58 - 58 - 58 - 58 make - 6 - 7 - 7 - 7 - 7 - 7 - 7 - 7 - 7 - 7	ower Requirements (Total Device) Maximum Power Supply Current		14		2 1		37.5				,	,	37.5		,	mAdc	,		,		,	-1	,		,	14	,	,	,	1,3,5,7,9
IppL 14 26 27 2	Power Supply Drain		14	-	28	1	28	1	28	'	28	1	28		28	mAdc	1		1	•	,	1.	,		1,3,5,9,		.1	,	14	7
Police Pulse Pulse in a large and a large		IDDL	14	1	26	. 1	56	'	26	'	26	1	56	1	26	mAde	1	,	'	1			1	,		1		,	41	1,3,5,7,9
. 1.2	Switching Parameters Turn-On Delay	t pd+	1,2		1	- 1	10	r		1			01		1	su	Pulse In	Pulse Out					,				14	,		* 2
-pd,	Turn-Off Delay	t pd-	1,2			1	10	'	1	1	-	-	10	-	,	su	1	64	,	,		,	1	1		'	14			**
where the second section is a second section and the second second section is a second section to the second section s	* Since this is an inv.	erting gate,	power dra	ain is i	ninimize	d by gr	Suipuno.	the in	outs to	gates n	ot under	test.																		