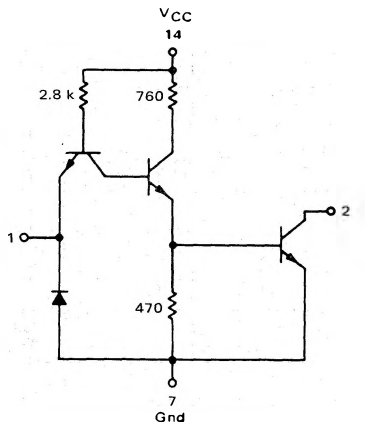
HEX INVERTER

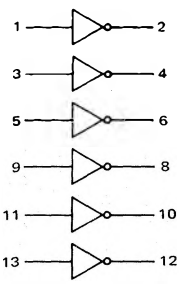
MC3109F • MC3009F
MC3109L • MC3009L,P

(54H05J) (74H05J,N)

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



This device consists of six independent inverting gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



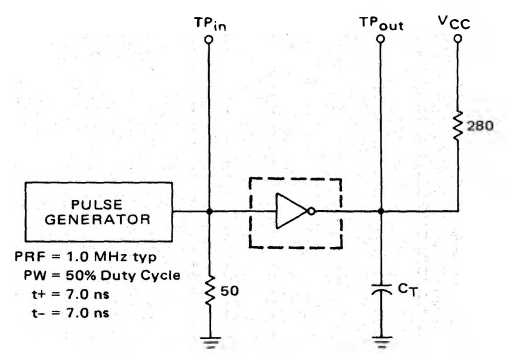
Positive Logic: $2 = \overline{1}$

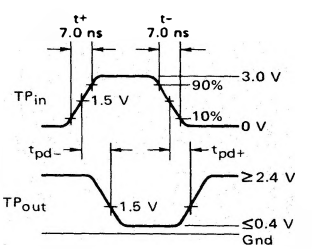
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 8 ns typ

Pin numbers for the 54H05F/74H05F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3109FL/3009F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H05F/74H05F	1	14	3	2	5	6	11	8	7	10	9	12	13	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



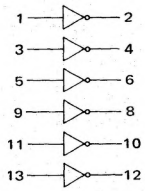


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES													
		mA			Volts										
		I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
MC3109	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	
	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	
MC3009	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	
	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3109 Test Limits						MC3009 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:													
			−55°C		+25°C		+125°C		0°C		+25°C		+75°C			I_{OL}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max															
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	-	-	-	-	-	14*	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	14	7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	7*
Output Output Voltage	V_{OL}	2	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	2	-	-	-	1	-	-	-	-	-	-	14	-	7*
Output Leakage Current	I_{CEX}	2	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	-	-	-	-	2	-	-	14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	37.5	-	-	-	-	-	37.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	1,3,5,7, 9,11,13
Power Supply Drain	I_{PDH}	14	-	58	-	58	-	58	-	58	-	58	-	58	mAdc	-	-	-	-	-	-	-	1,3,5,7, 9,11,13	-	-	-	-	14	7
	I_{PDL}	14	-	26	-	26	-	26	-	26	-	26	-	26	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7, 9,11,13
Switching Parameters Turn-On Delay	t_{pd-}	1,2	-	-	-	15	-	-	-	-	-	15	-	-	ns	Pulse In 1	Pulse Out 2	-	-	-	-	-	-	-	-	-	14	-	-	7*
Turn-Off Delay	t_{pd+}	1,2	-	-	-	18	-	-	-	-	-	18	-	-	ns	1	2	-	-	-	-	-	-	-	-	-	14	-	-	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.