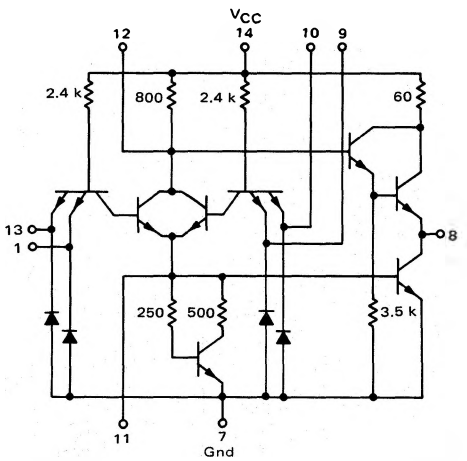
EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC3120F • MC3020F
MC3120L • MC3020L,P

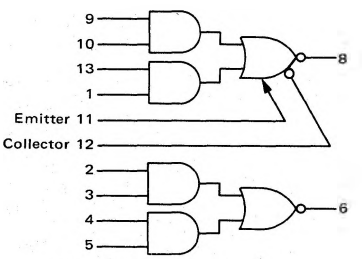
(54H50J) (74H50J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN†



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030/3130 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

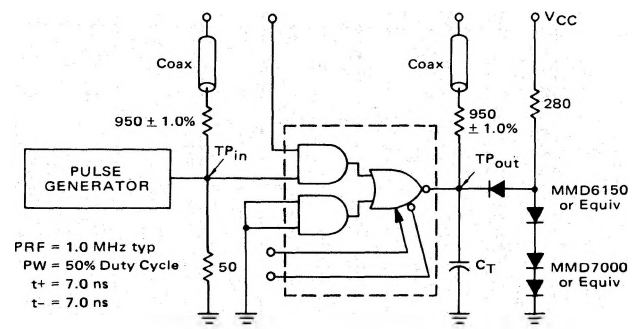
$$8 = \overline{(9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$$

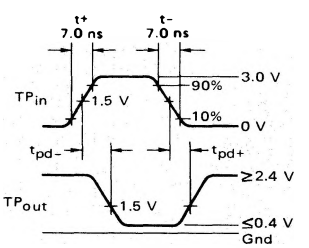
Negative Logic:

$$8 = \overline{(9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})}$$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 62.5 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Expander pins should be left open when measuring switching times.

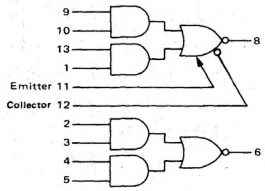
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	I_{OL} (mA)	I_{OH} (mA)	I_{in} (mA)	I_D (mA)	I_E (mA)	I_{EXE} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{IHX} (Volts)
TEST CURRENT/VOLTAGE VALUES	MC3120 −55°C	20	-2.0	-	-	0.3	0.55	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	MC3120 +25°C	20	-2.0	1.0	-10	0.3	0.71	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	MC3120 +125°C	20	-2.0	-	-	0.3	0.92	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	MC3020 0°C	20	-2.0	-	-	0.3	0.65	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	MC3020 +25°C	20	-2.0	1.0	-10	0.3	0.71	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	MC3020 +75°C	20	-2.0	-	-	0.3	0.82	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3120 Test Limits −55°C Min	MC3120 Test Limits −55°C Max	MC3120 Test Limits +25°C Min	MC3120 Test Limits +25°C Max	MC3120 Test Limits +125°C Min	MC3120 Test Limits +125°C Max	MC3020 Test Limits 0°C Min	MC3020 Test Limits 0°C Max	MC3020 Test Limits +25°C Min	MC3020 Test Limits +25°C Max	MC3020 Test Limits +75°C Min	MC3020 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	I_E	I_{EXE}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	7, 9, 10, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	14	-	-	7, 9, 10*
Output Output Voltage	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	-	1	-	-	13	-	-	-	14	-	-	7, 9, 10*
	V_{OL}	8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	-	14	-	-	1,7,9,10,13
	V_{OH}	8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	-	1	-	-	-	13	-	-	14	-	-	1, 7, 10*
Short-Circuit Current	I_{SC}	8	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 7, 8, 9, 10, 13*
Base-Emitter Voltage	$V_{BE\ max}$	11	-	1.10	-	-	-	-	-	1.00	-	-	-	-	Vdc	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 13*
	$V_{BE\ min}$	11	0.80	-	0.65	-	0.45	-	0.70	-	0.65	-	0.55	-	Vdc	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12, 13*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	24	-	-	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	-	-	14	-	7
	I_{PDL}	14	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	-	12.8	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 4, 5, 7, 9, 10, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	Pulse In: 1	Pulse Out: 8	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*
Turn-Off Delay	t_{pd+}	1, 8	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.