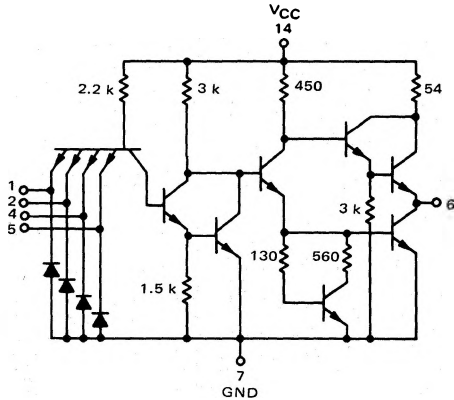


**DUAL 4-INPUT "AND"
POWER GATE**

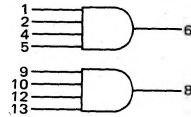
MC3100/MC3000 series

**MC3126F • MC3026F
MC3126L • MC3026L,P**

**CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN**



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).



Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$

Negative Logic: $6 = 1 + 2 + 4 + 5$

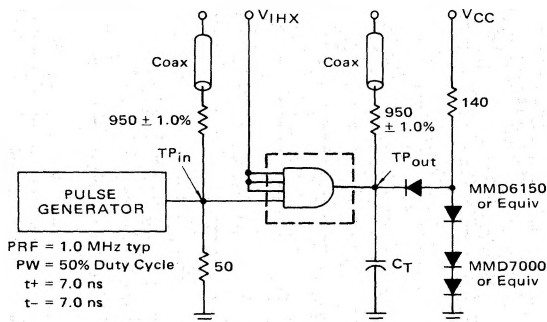
Input Loading Factor = 1.3

Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg

Propagation Delay Time = 9.0 ns typ

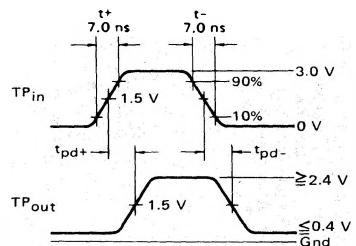
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PRF = 1.0 MHz typ
PW = 50% Duty Cycle
 $t^+ = 7.0$ ns
 $t^- = 7.0$ ns

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

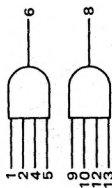
The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



MC3126, MC3026 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



			TEST CURRENT / VOLTAGE VALUES																											
			mA						Volts																					
			I _{OL}	I _{OH}	I _{IN}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{BE}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{HX}														
Characteristic	Symbol	Pin Under Test	MC3126 Test Limits						MC3026 Test Limits						TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C																	
Input			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I _{OL}	I _{OH}	I _{IN}	I _D	V _{IL}	V _{IH}	V _F	V _R	V _{BE}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{HX}	Gnd	
Forward Current	I _F	1	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-2.6	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	-	14	-	7
Leakage Current	I _R	1	-	50	-	50	-	50	-	50	-	50	-	50	-	-	-	-	-	-	-	1	*	-	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BV _{IN}	1	-	-	-	5.5	-	-	-	-	-	5.5	-	-	-	-	-	-	-	-	-	*	-	-	-	-	14	-	2, 4, 5, 7	
Clamp Voltage	V _D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	-	-	-	-	-	-	-	*	-	-	-	14	-	-	7	
Output																														
Output Voltage	V _{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	6	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	-	7
	V _{OH}	6	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	-	-	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	-	7
Short-Circuit Current	I _{SC}	6	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	-	6	-	-	-	-	-	-	1, 2, 4, 5 *	-	-	-	14	-	-	6, 7
Power Requirements																														
Maximum Power (Total Device)																														
Maximum Power Supply Current	I _{max}	14	-	-	-	22	-	-	-	-	-	22	-	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	-	-	-	-	7	
Power Supply Drain	I _{PDH}	14	-	15	-	15	-	15	-	15	-	15	-	15	-	-	-	-	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	-	-	14	-	-	7
	I _{PDL}	14	-	40	-	40	-	40	-	40	-	40	-	40	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters																														
Turn-On Delay	t _{pd+}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	-	7
Turn-Off Delay	t _{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	-	7

* Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{BE}.