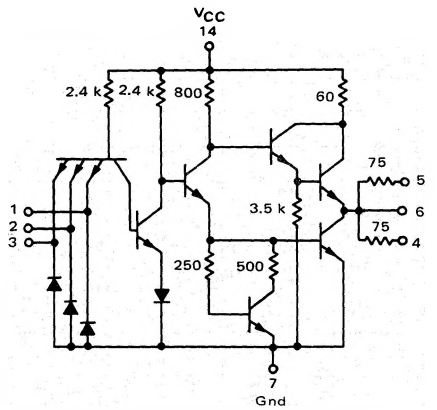
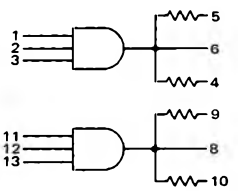
DUAL 3-INPUT 3-OUTPUT
"AND" SERIES TERMINATED
LINE DRIVER

MC3128F • MC3028F
MC3128L • MC3028L,P

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = 1 • 2 • 3
Negative Logic: 4, 5, 6, = 1 + 2 + 3

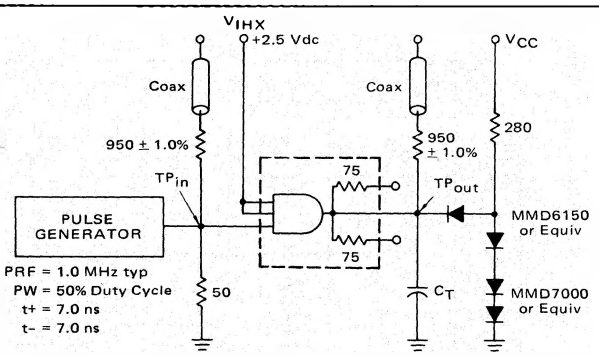
Input Loading Factor = 1

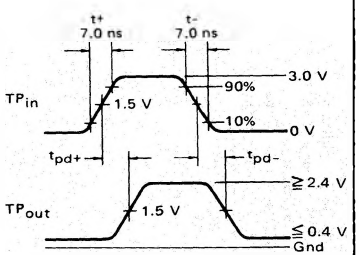
Output Loading Factor, Direct Output (Pins 6 & 8) = 8 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





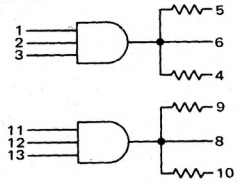
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES																		
		mA								Volts										
		$I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
MC3128	−55°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5	
	+125°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-	
MC3028	0°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-	
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5	
	+75°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-	

Characteristic	Symbol	Pin Under Test	MC3128 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3028 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL\,A}$	$I_{OL\,B}$	$I_{OL\,C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																																
Forward Current	$I_{F\,2}$	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	2, 3*	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 3, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 3, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output																																
Output Voltage	$V_{OL\,1}$	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	$V_{OL\,2}$	5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	6	5	4	-	-	-	1	-	-	2, 3*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3*	-	-	-	14	-	6, 7
Power Requirements (Total Device)																																
Maximum Power Supply Current	I_{max}	14	-	-	-	18	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7 11, 12, 13
Switching Parameters																Pulse In	Pulse Out															
Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.