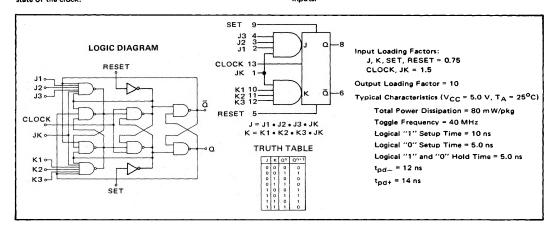
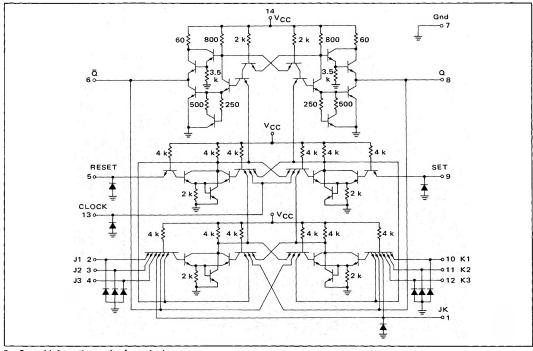
"AND" J-K FLIP-FLOP

## MC3150F · MC3050F MC3150L · MC3050L,P

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs  $\Omega$  and  $\bar{\Omega}$  respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.





See General Information section for packaging.

FIGURE 1 - IEX TEST CIRCUIT

FIGURE 3 – V<sub>OL</sub> TEST CIRCUIT

# MC3150, MC3050 (continued)

STICS		73		T	1		-																				
		75	က   ၂၂	П		_	0 8	~					@	@ Test		Αm		1	1		1	1	Volts		-	1	
	បី	CLOCK	-	깁	)								Temp	Temperature		_ĕ	<u>E</u>	٥	>=	>=		>~	>	> xem		V CCH	
		¥		+								2	_	25		-2.0	1	- [		2.0		4.2	1	+	+	5.5	
		7	10	5			-					3	OCIONI)	+25 C		-2.0	i.c	3		1.8	9	4.5	1	0.1		0.0	
		K2	1	П		×	9-0	"					٠.	+1257		-2.0	1		0.8	1.8	0.4	2.4	4.0	1		5.5	
		K3	_	1	)	1	7							0.0		-2.0	-	•	1.1	2.0	0.4	2.5	1			5.25	
	Œ	ESET	5			7						Ŭ M	MC3050	+25°C	20	-2.0	1.0	10	1.1	1.8	0.4 2.5	2.5	4.0	7.0 4	4.75 5.	5.25	
													_	+75°C	20	-2.0	ŀ	,	6.0	1.8	0.4 2.5	2.5	4.0	- 4	4.75 5.	5,25	
		Pi.		MC31	50 Te	MC3150 Test Limits	its	H	Z	C3050	MC3050 Test Limits	Limits					-	EST CU	RRENT	100/	AGEA	PPLIE	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:	ELOW.		Γ	
Characteristic	Combol	Under	—55°C	C Way	Min Max Min Max		+125°C	_	O°C Min May		+25°C		+75°C	.ta	_5	-2	-	_	>"	>	>"	>0	N N N N N N N N N N N N N N N N N N N	V V	1 5	7	Gnd
Characteristic	эушро	_	W I	MIGX	E I			_	Ě		PIA		MIGX	5	5	5	=	_	=	=		×		ž –	3	5	
Input Forward Current	<sup>1</sup> F.J	20 8 4	111	-1.5 	111	-1.5	7 -	-1.5 	-1.5	1 1 1		1.1.1	-1:5 	mAdc →	111	1.1.1	1.1.1	1 1 1		111	81 82 44	1 1 1	1,3,4,5 1,2,4,5 1,2,3,5	1 1 1		41 <del>-</del>	7,9,13
	<sup>L</sup> FK	11 12 12	1 1 1	-1.5	111	i	7 -	£. →	-1.5	111	-i.5	1.1.1	-1.5	mAdc	1 1 1	111		1 1 1			110	1 1 1	1,9,11,12 1,9,10,12 1,9,10,11	111		14	5,7,13
	1FC	13		-3.0	1	-3.0	٠,	-3.0	3.0	0	-3.0	-	-3.0	mAdc	,		1			,	13	1		,	,	14	1,5,7,9
	1FJK	-	-	-3.0	1	-3.0	· ?	-3.0	-3.	-3.0	-3.0	-	-3.0	mAdc	,				,			,	2,3,4,10,11,12	,		14	5,7,9,13
	FS	6	-	-1.5	1	-1.5	-	-1.5	-1	-1.5 -	-1.5		-1.5	mAdc	-					,	6	,	2		,	14	7
	IFR	2	-	-1.5	1	-1.5	7	-1.5	-1-	-1.5	-1.5	1	-1.5	mAdc	1		,	'		,	25	,	6	,	,	14	7
Leakage Current	<sup>I</sup> RJ	004	1 1 1	20	1 1;1	09 -		20 -	- 20	0 .	8-	1 1 1	20	μ Adc	1 1 1		111			111		004	<b>σ</b> →	1 1 1		41	1,3,4,5,7 1,2,4,5,7 1,2,3,5,7
	LRK	12 12		20	1 1 1	9. —	111	20 -	200		20	1 1 1	20	μAdc →	1 1 1	111	1 1 1		1.1.1	111		12 12	w <b>→</b>	111	111	41-	1,7,9,11,12 1,7,9,10,12 1,7,9,10,11
	<sup>1</sup> RC	13		100	-	100	- 11	100	- 100	- 0	100		100	μAdc	1			,	,	,	,	13 1,	,2,3,4,5,10,11,12	,	,	14	6,7
	LRJK	1		100	-	100	7	100	- 100	9	100	'	100	μAde	,		,	,	,			-	6		-	14 2,	2,3,4,5,7,10,11,12
	IRS	6	1.	20	,	20	ın.	20	- 20		20	'	20	μAde	,			,	,			o.		,		14	7
	IRR	2	,	20	1	20	10	20	- 20	-	20		20	μAde	,					-		2	!	,	,	14	7
Breakdown Voltage	BV <sub>in</sub>	2 4 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			· ·					ů.	111111111			v V dc	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	111111111	2 8 4 4 10 11 11 11 11 11 11 11 11 11 11 11 11					111111111	5 5 5 6,2,4,5,10,11,12			2,	1,3,4,5,7 1,2,4,5,7 1,2,3,5,7 1,7,9,11,112 1,7,9,10,11 7,9 2,3,4,5,7,10,11,12
Clamp Voltage	v <sub>D</sub>	2 4 4 3 2 1 1 1 1 1 1 1 2 1 1 1 2 1 1 1 2 1 1 1 2 1			7	i.					i.			Add.		1111111111	111111111	2 3 11 11 13 13 13 5							14		
Output Output Voltage	NOL.	9 8		4.0		0.4	0 0	0.4	- 0.4	4 4	0.4	1 1	0.4	Vdc	9		1 1	1 1	5 6	e 10	1 1					14	7,13
	VOH	9 80							2.5	2.5			1.1	Vdc		9 8	1 1	1 1	0.0	ശര	1.1	1 1			14		7,13
Short-Circuit Current	1 sc	98	-40	-100	-40 -1	100	-40 -1 -40 -1	-100	-40 -100 -40 -100	00 -40 00 -40	-100	-40	-100	mAdc				1.1		1.1	1.1	1 1	മ	7.1		14	6,7,9
Power Requirements (Total Device) Maximum Power Supply Current	Imax	14	,		,	35		<u> </u>	,	'	35		1	mAdc			-	-		1	r	,	,	14	ı		1,5,7,13
Power Supply Drain								-					1			-	1					1		į			

ELECTRICAL CHARACTERISTIC

#### **OPERATING CHARACTERISTICS**

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

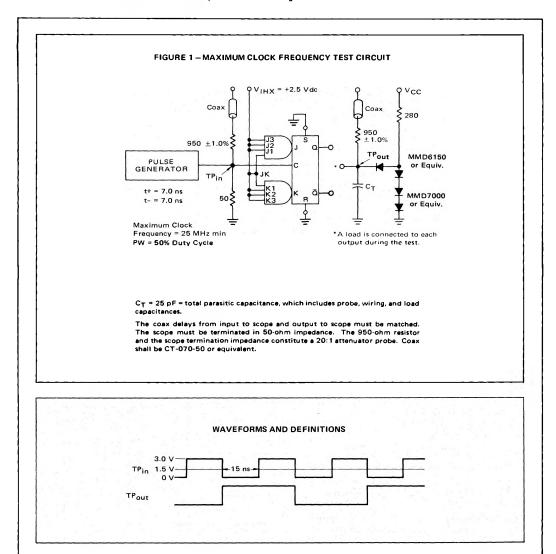
#### **Unused Inputs:**

JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and  $5.5\,\mathrm{Vdc}.$ 

Unused J inputs should be tied to used J inputs, the used JK input,  $\overline{\mathbf{Q}}$ , or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input,  $\mathbf{Q}$ , or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs MUST be tied to ground.

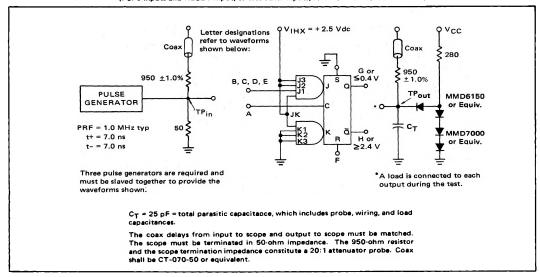


H 3.0 V

tpd-

### **OPERATING CHARACTERISTICS (continued)**

# FIGURE 2 – SWITCHING TIME TEST CIRCUIT (For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



#### A 3.0 V CLOCK (Must be used on all tests) -30 ns-TEST PROCEDURES CHART B 3.0 V INPUT LIMITS (ns) ã. - tSetup "1" a٠ 100 K\*\* TEST 30 ns C 3.0 V 8 17 01 С Gnd G н tHold "1" Setup "0" J ٥ Gnd Gnd < 0.4 V >2.4 V 5.0 D 3.0 V thold "O" Ε Gnd Gnd ≤0.4 V ≥2.4 V 0.1 1 5 V Setup "1" K Gnd F Gnd в н G 17 tSetup "0" thold "1" K Gnd 01 +tHold "O" E 3.0 V tSetup "O" K Gnd D ≥ 2.4 ∨ Gnd ≤0.4 V 5.0 <sup>t</sup>Hold "0" K Ε 01 Gnd ≥ 2.4 ∨ ≤0.4 ∨ +30 ns+ 8.0 30 500 ns Delay from clock to Q during tSetup "1" K test. F 3.0 V Delay from clock to 0 during t<sub>Setup</sub> "1" J test. Delay from clock to 0 during t<sub>Setup</sub> "1" K test. 1.5 V 8.0 30 Delay from SET to Q during tSetup "1" K test. Delay from RESET to $\overline{\mathbf{Q}}$ during tSetup "1" J test t<sub>sd+</sub> t<sub>sd</sub>-G 3.0 V 1.5 V Delay from SET to a during tSetup "1" K test. Delay from RESET to a during tSetup "1" J test ted-7.0 23

-1.5 V

\*\* Letters shown in these columns refer to waveforms at the left.  $t_{
m Hold}$  is typically a negative number.

**VOLTAGE WAVEFORMS AND DEFINITIONS**