

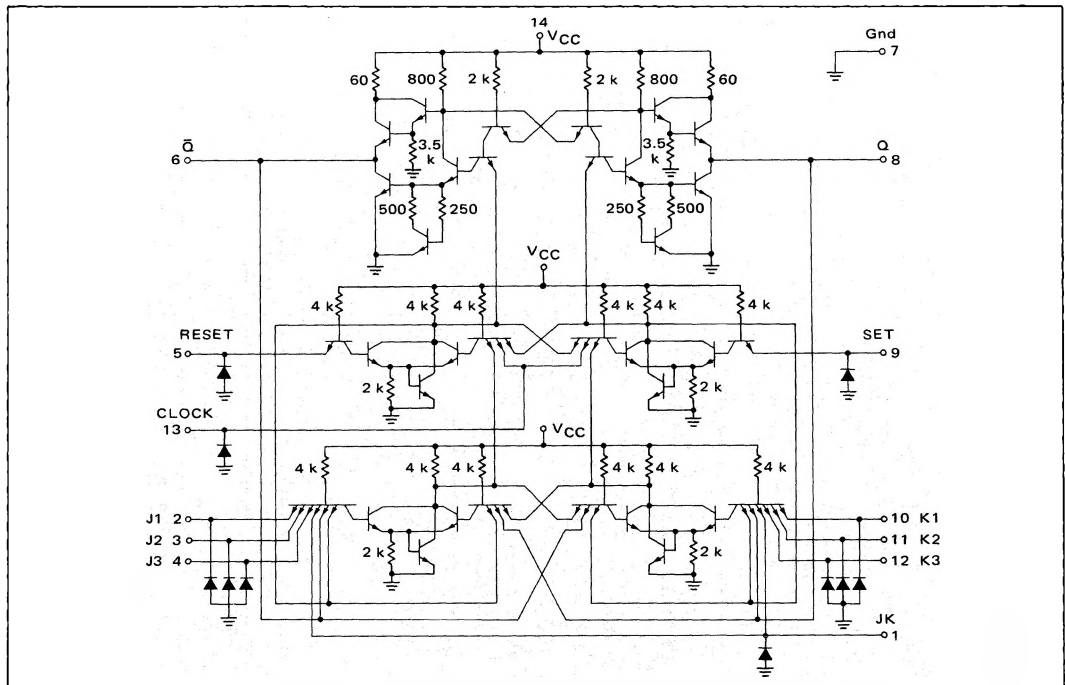
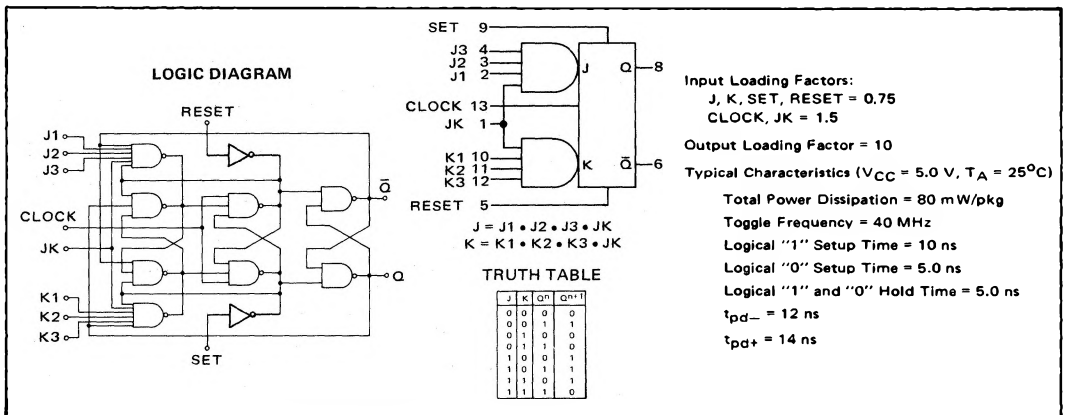
"AND" J-K FLIP-FLOP

MC3100/MC3000 series

MC3150F • MC3050F
MC3150L • MC3050L,P

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.



See General Information section for packaging.

FIGURE 1 – I_{EX} TEST CIRCUIT

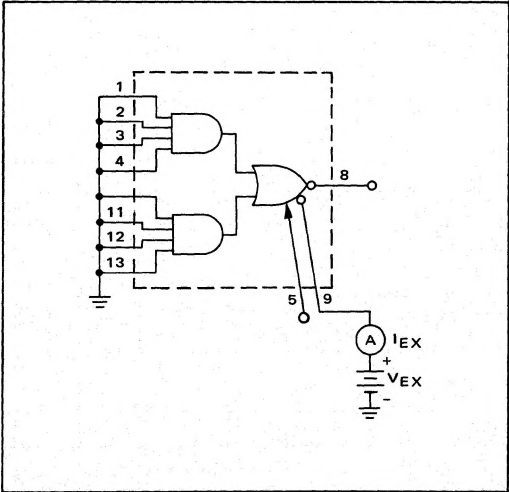


FIGURE 2 – V_{BE} TEST CIRCUIT

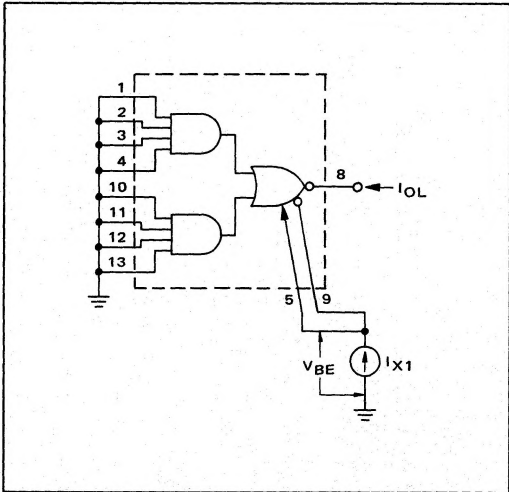
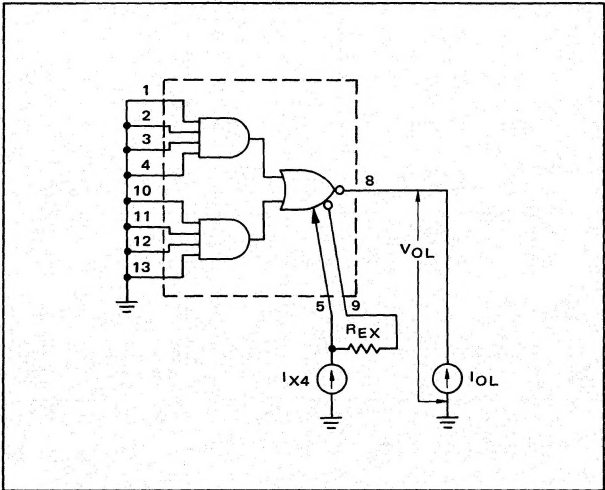
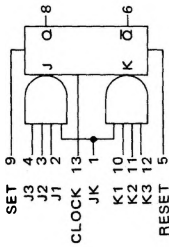


FIGURE 3 – V_{OL} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS



CS

Characteristic	Symbol	TEST CURRENT / VOLTAGE VALUES	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:	Unit																																																																																																																																																																																																									
Input	Pin	MC3150 Test Limits	Test	MC3050 Test Limits	Test	mA	V _{IL}	V _{IH}	V _F	V _R	V _{max}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}	V _{VCH}

OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

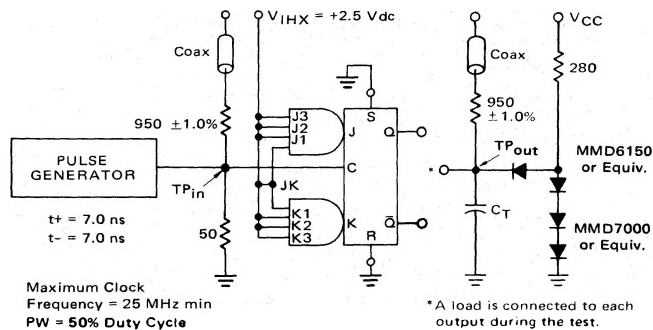
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, $\bar{Q}$, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs MUST be tied to ground.

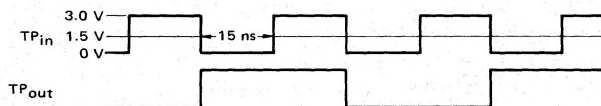
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

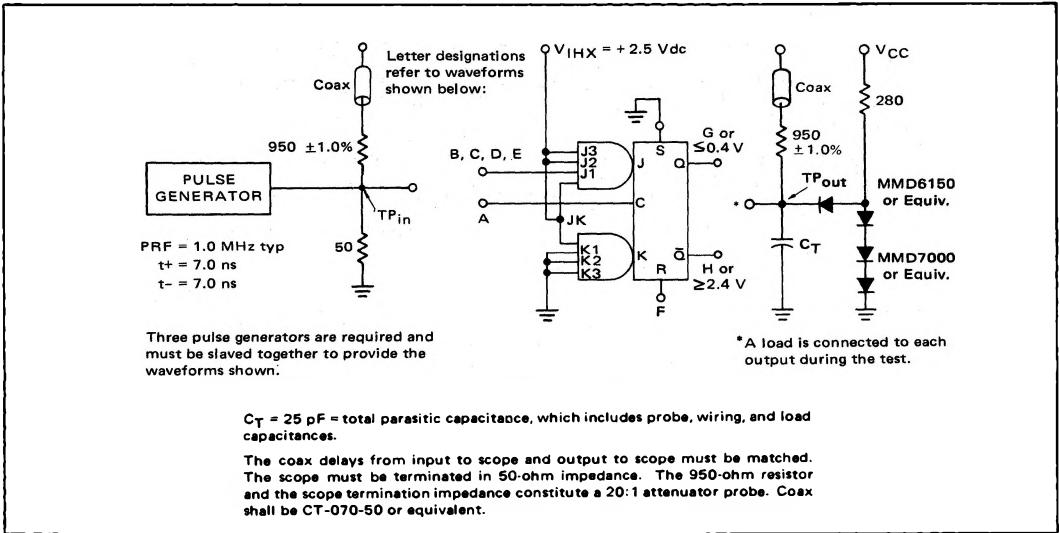
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS

