

"AND" J-K FLIP-FLOP

MC3100/MC3000 series

MC3151F • MC3051F
MC3151L • MC3051L,P

This J-K flip-flop triggers on the negative edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is low, data is entered into the input steering section of the flip-flop when the clock goes high. The input steering section of the flip-flop continually reflects the input state when the clock is high. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the negative edge of the clock and the outputs Q and \bar{Q} respond accordingly. The flip-flop can be set or reset directly by applying the low state to the SET or RESET inputs.

LOGIC DIAGRAM

SET 9

J3 12
J2 11
J1 10

CLOCK 13

JK 1

K1 2
K2 3
K3 4

RESET 5

Q 8

\bar{Q} 6

$J = J1 \cdot J2 \cdot J3 \cdot JK$
 $K = K1 \cdot K2 \cdot K3 \cdot JK$

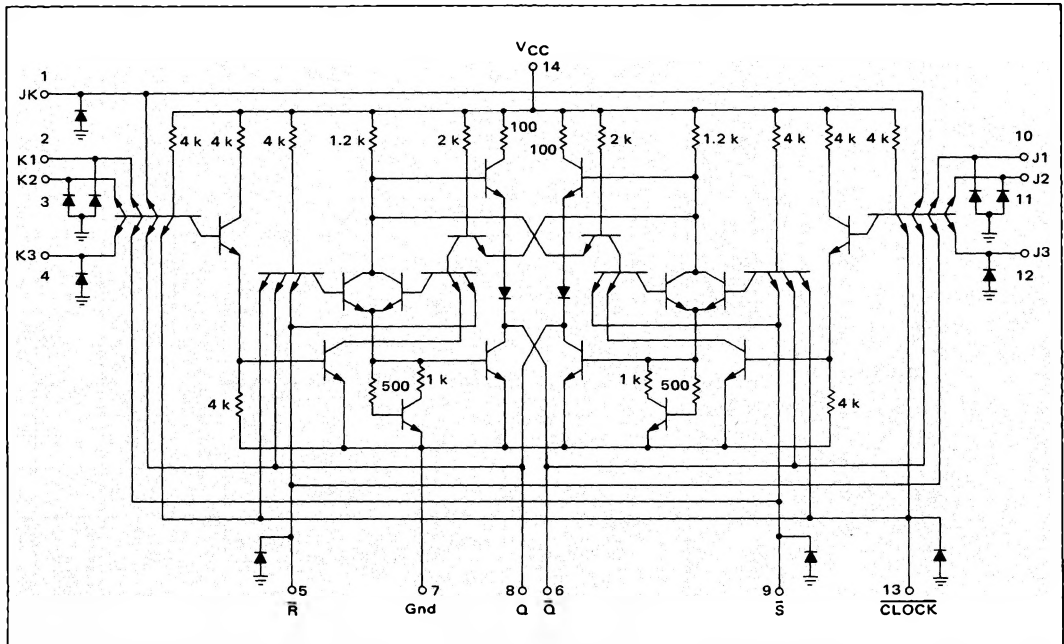
TRUTH TABLE

J	K	Q ⁿ	Q ⁿ⁺¹
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
J, K = 0.75
JK = 1.5
Set, Reset = 2.0
Clock = 2.3

Output Loading Factor = 10

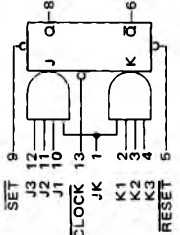
Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C)
Total Power Dissipation = 50 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Time = 5.0 ns
t_{pd-} = 12 ns
t_{pd+} = 14 ns



See General Information section for packaging.

MC3151, MC3051 (continued)

ELECTRICAL CHARACTERISTICS



Characteristic	Symbol	Pin Under Test		MC3151 Test Limits						MC3051 Test Limits						TEST CURRENT/VOLTAGE VALUES											
				-55°C		+25°C		+125°C		0°C		+25°C		+75°C		mAdc				Volts							
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Input Forward Current	K	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	J	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	JK	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-	-	-	-	-	-	-	-	-	-	-	-	-
	Set	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-	-	-	-	-	-	-	-	-	-	-	-	-
	Reset	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-4.0	-	-	-	-	-	-	-	-	-	-	-	-	-
	Clock	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-	-	-	-	-	-	-	-	-	-	-	-	-
Reverse Current	K	50	50	50	50	50	50	50	50	50	50	50	50	50	-	-	-	-	-	-	-	-	-	-	-	-	-
	J	50	50	50	50	50	50	50	50	50	50	50	50	50	-	-	-	-	-	-	-	-	-	-	-	-	-
	JK	100	100	100	100	100	100	100	100	100	100	100	100	100	-	-	-	-	-	-	-	-	-	-	-	-	-
	Set	140	140	140	140	140	140	140	140	140	140	140	140	140	-	-	-	-	-	-	-	-	-	-	-	-	-
	Reset	140	140	140	140	140	140	140	140	140	140	140	140	140	-	-	-	-	-	-	-	-	-	-	-	-	-
	Clock	145	145	145	145	145	145	145	145	145	145	145	145	145	-	-	-	-	-	-	-	-	-	-	-	-	-
Breakdown Voltage	K	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	J	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	JK	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Set	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Reset	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Clock	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-
Clamp Voltage	K	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	J	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	JK	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Set	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Reset	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
	Clock	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-
Output Output Voltage	V _{OL}	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-
	V _{OH}	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{SC}	-65	-65	-65	-65	-65	-65	-65	-65	-65	-65	-65	-65	-65	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{max}	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{max}	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{max}	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-	-	-	-	-	-	-	-	-	-	-	-	-
Power Requirements (Total Device) Maximum Power Current	I _{max}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	I _{ppd}	16	16	16	16	16	16	16	16	16	16	16	16	16	-	-	-	-	-	-	-	-	-	-	-	-	

* Momentary ground before making measurement. If pin number appears in other column, it should be returned to voltage.

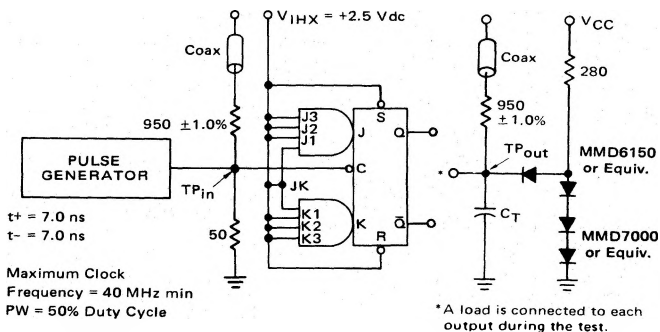
OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain 5.0 ns after the clock signal rises.
 Negative edge triggering: When the clock goes from the high state to the low state, the information in the input steering section is transferred to the bistable section.
 The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED to a voltage between 2.0 and 5.5 Vdc.

Unused Inputs:

JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.
 Unused J inputs should be tied to used J inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.
 Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.
 Unused SET and RESET inputs MUST be tied to a voltage between 2.0 and 5.5 Vdc.

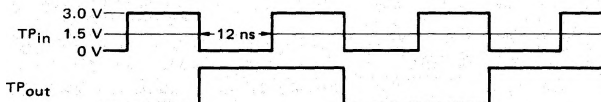
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

WAVEFORMS AND DEFINITIONS

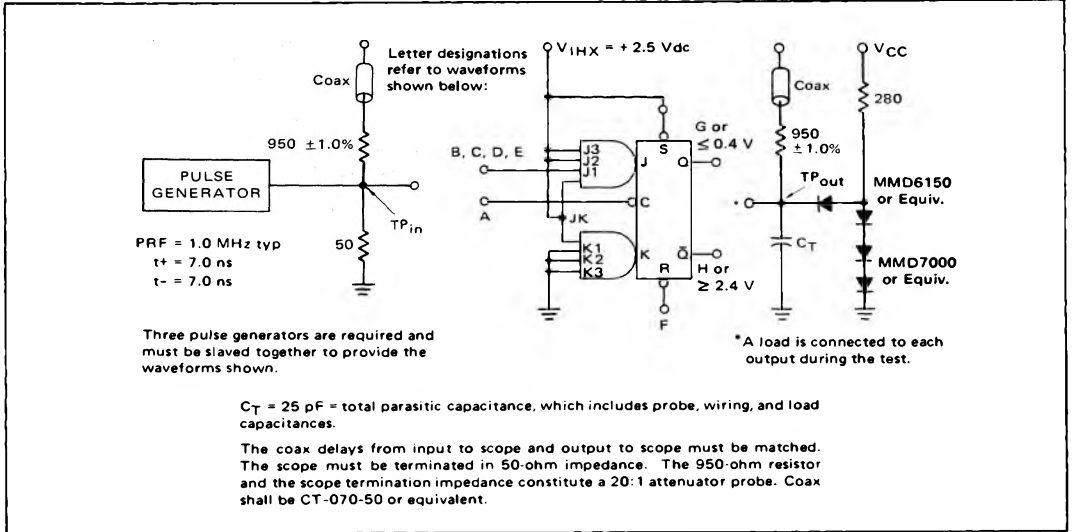


MC3151, MC3051 (continued)

OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS

