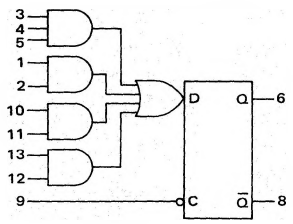
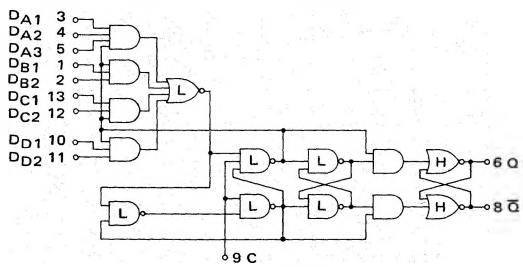
DOUBLE-EDGE-TRIGGERED
MASTER-SLAVE TYPE D
FLIP-FLOP

MC3153F • MC3053F
MC3153L • MC3053L,P

This double-edge-triggered master-slave type D flip-flop accepts data on the rising clock edge and transfers it to the output when the clock input changes back to the logic "0" state. A 4-wide, 2-2-2-3 input AND-OR gate is internally connected to the D input of the flip-flop. This makes the device useful in forming shift registers using one package per bit.





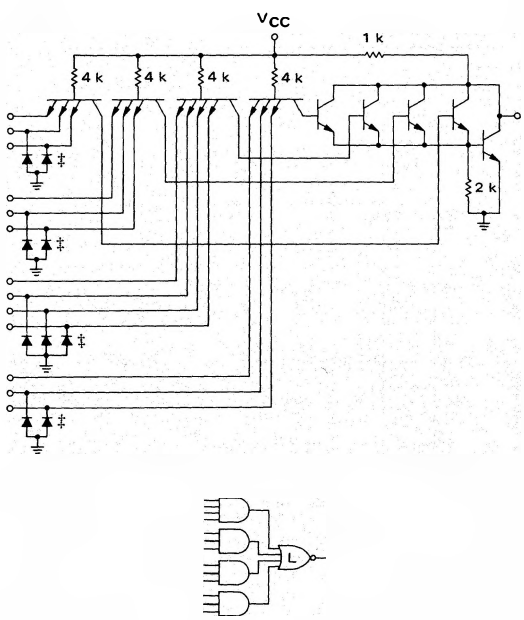
V_{CC} = 14
Gnd = 7

Input Loading Factor:
D Inputs = 1
Clock Input = 2

Output Loading Factor = 10

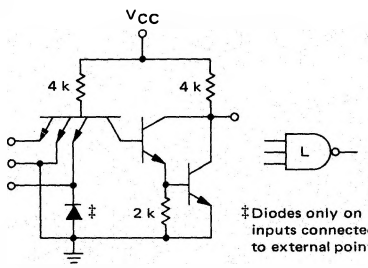
Total Power Dissipation = 100 mW typ

LOW LEVEL "AND-OR-INVERT" GATE



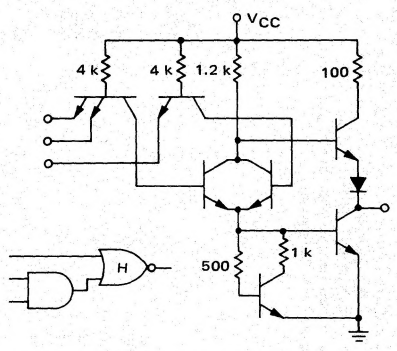
‡Diodes connected from each input to GND.

LOW-LEVEL "NAND" GATE



‡Diodes only on inputs connected to external points.

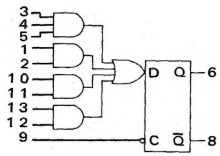
HIGH LEVEL "AND-OR-INVERT" GATE



See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one of the input AND gates. Furthermore only one input on the AND gate is tested. To complete testing, test other gates and inputs in the same manner.

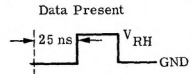


	@ Test Temperature	TEST VOLTAGE/CURRENT VALUES															
		mAdc				Vdc											
		I_{OL1}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}		
MC3153	−55°C	20.0	-1.6	-	-	0.4	1.1	2.0	2.4	4.0	5.0	4.5	5.5	-		
	+25°C	20.0	-1.6	1.0	-10	0.4	1.1	1.8	2.4	4.0	5.0	4.5	5.5	7.0		
	+125°C	20.0	-1.6	-	-	0.4	0.8	1.8	2.4	4.0	5.0	4.5	5.5	-		
MC3053	0°C	20.0	-1.6	-	-	0.4	1.1	2.0	2.5	4.0	5.0	4.75	5.25	-		
	+25°C	20.0	-1.6	1.0	-10	0.4	1.1	1.8	2.5	4.0	5.0	4.75	5.25	7.0		
	+75°C	20.0	-1.6	-	-	0.4	0.9	1.8	2.5	4.0	5.0	4.75	5.25	-		

Characteristic	Symbol	Pin Under Test	MC3153 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3053 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	**	Gnd*
Input																													
Forward Current	I_F																												
Data		1	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	-	1	-	-	-	2	-	-	14	-	-	7
Clock		9	-	-3.2	-	-3.2	-	-3.2	-	-3.2	-	-3.2	-	-3.2	mAdc	-	-	-	-	9	-	-	-	-	-	-	14	-	-	7
Reverse Current	I_R																												
Data		1	-	40	-	40	-	40	-	40	-	40	-	40	μAdc	-	-	-	-	-	-	-	1	-	-	-	14	-	-	2,7*
Clock		9	-	80	-	80	-	80	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	9	-	-	-	14	-	-	9
Breakdown Voltage	BV_{in}																												
Data		1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	2,7*
Clock		9	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	9	-	-	-	-	-	-	-	-	14	-	-	7
Clamp Voltage	V_D																												
Data		1	-	-	-	-1.5	-	-	-	-	-1.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	14	-	-	-	7
Clock		9	-	-	-	-1.5	-	-	-	-	-1.5	-	-	-	Vdc	-	-	-	9	-	-	-	-	-	-	14	-	-	-	7
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	1,2,3,4,5, 10,12,13	11	-	-	-	14	-	-	9	7
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	1,2,3,4,5,10,11	12,13	-	-	-	14	-	-	9	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	3,4,5,10,11,12,13	1,2	-	-	-	14	-	-	9	7
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	1,3,4,5,10,11,12,13	2	-	-	-	14	-	-	9	7
Power Requirements (Total Device)																													
Maximum Power Supply Current	I_{max}	14	-	-	-	39	-	-	-	-	-	39	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	7*
	I_{PDH}	14	-	30	-	30	-	30	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	7

*Other input pins grounded.

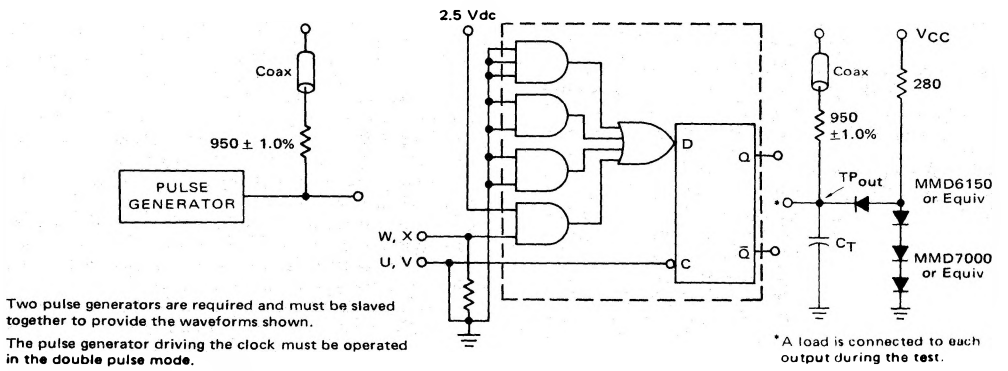
**Apply positive pulse prior to taking measurement to set flip-flop in the desired state.



OPERATING CHARACTERISTICS

Data present at the D inputs 20 ns prior to and 5.0 ns following the rising edge of the clock pulse is stored in the flip-flop until the clock falling edge, when it is transferred to the outputs. The data may change any time except between the setup time (20 ns) and the hold time (5.0 ns) without affecting the outputs.

SWITCHING TIME TEST CIRCUIT



*A load is connected to each output during the test.

Two pulse generators are required and must be slaved together to provide the waveforms shown.

The pulse generator driving the clock must be operated in the double pulse mode.

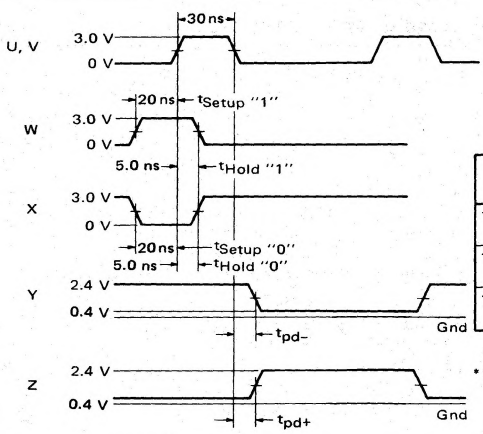
Letter designations refer to waveforms shown below:

SYMBOL	WAVEFORM		
	U	V	W, X
f	20 MHz	1.0 MHz	0.5 MHz
PW	50% Duty Cycle	30 ns	–
t+, t-	7.0 ns	7.0 ns	7.0 ns

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST		SYMBOL	INPUT C̄	INPUT D	Q	Q̄	LIMIT
Turn-On Delay	Q̄	t_{pd-}	V	W	Z	Y	35 ns
	Q		V	X	Y	Z	max.
Turn-Off Delay	Q̄	t_{pd+}	V	X	Y	Z	35 ns
	Q		V	W	Z	Y	max.
Toggle Frequency	Q̄	f_{Tog}	U	*	–	**	20 MHz
	Q		U	*	**	–	min.

*D Input connected to Q̄ output.

**Output must change state with each input pulse.

APPLICATIONS INFORMATION

LOGIC DESCRIPTION

This flip-flop performs the D function, with input logic defined by the following equation:

$$6 = 1 \bullet 2 + 3 \bullet 4 \bullet 5 + 10 \bullet 11 + 12 \bullet 13$$

The operation of the flip-flop is as follows (refer to Figure 1). Assume Q is "0". To set a "1" on the Q output, "1" must be applied to all the inputs on either gate A, B, C, or D. When the clock goes high, a "0" appears on the output of gate G and a "1" appears on the output of gate H. However, because the other input to gate J comes from gate F, the output of J remains "0", and because of the input from gate G to gate I, the output of gate I remains "0". When the clock goes low, the outputs of gates E and F go to "1". Thus gate J now has a "1" applied to both inputs and its output goes to "1". Since gate L now has a "1" applied to it, its output goes to "0", and this is coupled to gate K, which now has zero applied to both inputs causing it to go to a "1". The flip-flop has now switched and Q is a "1". Setting a "0" on the output may be followed through in a similar fashion.

SYSTEM SKEW

Clock skew in a system is one of the most difficult problems that the system designer must solve. Consider the clock driver circuitry shown in Figure 2. Clock skew between C1 and C2 could be caused by a number of factors, including unequal loading, unequal wiring distances, and different turn-on and turn-off times between clock line driver gates that may be in the circuit between C1 and C2. Most flip-flops that are presently available in integrated form do not allow the system designer to control the amount of skew in the system. With the MC3153/3053, system clock skew can be adjusted.

Three basic types of flip-flops are now in use: (1) the charge-controlled flip-flop, (2) the edge-triggered flip-flop, and (3) the master-slave flip-flop. Figure 2 is an example of a system in which the clock skew problem is encountered. The direct-coupled shift register can be made with the two most common types of flip-flops – the negative-edge-triggered flip-flop or the master-slave flip-flop.

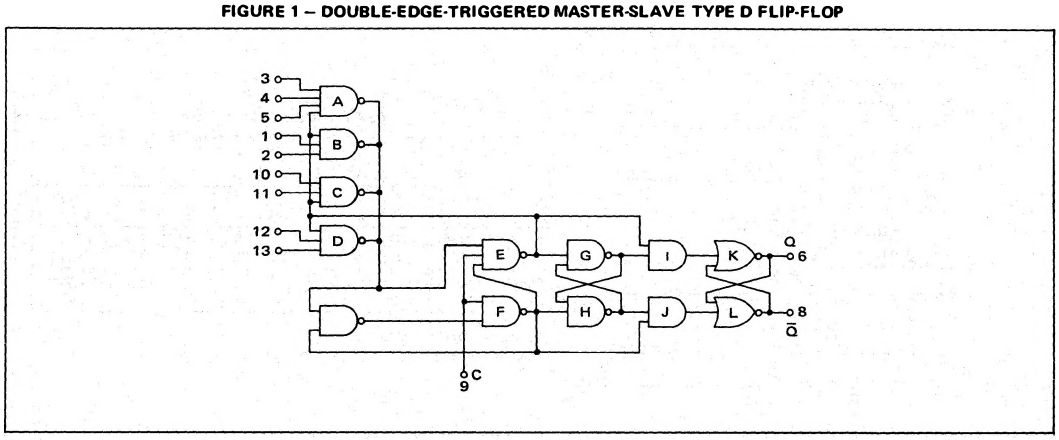
When negative-edge-triggered flip-flops are used to implement the shift register of Figure 2, the maximum allowable clock skew, Figure 3A, is the propagation delay from the falling edge of the clock to the output of flip-flop A minus the hold time of flip-flop B. It should be noted that the maximum propagation delay time and the minimum hold time from data sheets may not be used to calculate maximum allowable clock skew. Instead, the minimum propagation delay and maximum hold times must be used to calculate maximum clock skew to insure proper system operation over the entire temperature and power supply variations expected.

If the shift register of Figure 2 is constructed with master-slave flip-flops, the maximum allowable clock skew, Figure 3B, is the propagation delay from the falling edge of the clock to the output of flip-flop A plus the time required to transfer and latch the information into the master portion of flip-flop B. The minimum propagation delay and latch times must be used in calculating the maximum clock skew to guarantee proper system operation.

By using MC3153/3053 double-edge-triggered master-slave type D flip-flops in the circuit of Figure 2, the maximum clock skew, Figure 3C, is the propagation delay from the falling edge of the clock to the output of flip-flop A minus the hold time of flip-flop B plus the clock pulse width. In this case, minimum propagation delay and maximum hold time must be used in the skew calculations. However, since the clock pulse width is part of the clock skew calculation, system clock skew can be adjusted to any value the system designer feels necessary to insure proper operation of the system simply by adjusting the clock pulse width. The ability to adjust clock skew is a feature that cannot be stressed too highly because it gives the system designer freedom from maximum allowable clock skew restrictions.

It should be noted in Figure 3C that the maximum clock frequency for the MC3153/3053 is the reciprocal of the propagation

FIGURE 1 – DOUBLE-EDGE-TRIGGERED MASTER-SLAVE TYPE D FLIP-FLOP



delay plus the hold time plus the system skew. Therefore, as the clock pulse width is increased to provide clock skew adjustment, the maximum operating frequency is reduced.

INPUT LOGIC UTILIZATION

The input logic available on the MC3153/3053 makes this flip-flop a very powerful logic block. Figure 4 shows four MC3153/3053's wired together to form a universal, clocked, shift register with the following features: (1) serial data entry and shift right, (2) parallel data entry, (3) shift left, and (4) hold the information (store). Since the $\overline{Q}$'s are also available, a one's complement could be formed by entering each $\overline{Q}$ back into its flip-flop. In this shift register, four MC3153/3053's replace four type D flip-flops of another type plus 4-wide AND-OR-INVERT gates.

FIGURE 2 – DIRECT-COUPLED SHIFT REGISTER

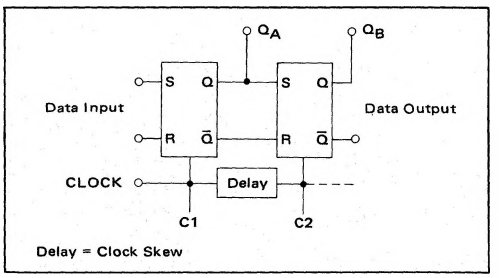
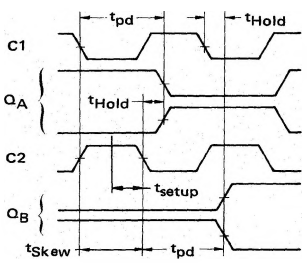


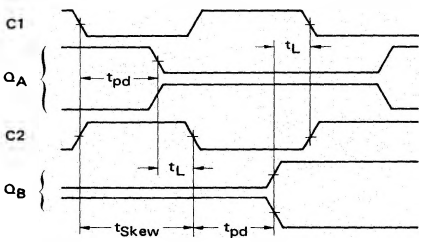
FIGURE 3 – CLOCK SKEW WAVEFORMS

FIGURE 3A – NEGATIVE-EDGE-TRIGGERED FLIP-FLOP



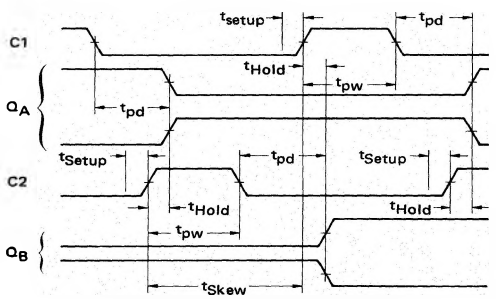
Maximum Clock Skew = $t_{pd} - t_{Hold}$
Minimum Clock Pulse Width (t_{pw}) = t_{Setup}

FIGURE 3B – MASTER-SLAVE FLIP-FLOP



Maximum Clock Skew = $t_{pd} + t_L$
Minimum Clock Pulse Width (t_{pw}) = t_L

FIGURE 3 C – DOUBLE-EDGE-TRIGGERED MASTER-SLAVE TYPE D FLIP-FLOP



Maximum Clock Skew = $t_{pd} - t_{Hold} + t_{pw}$
Minimum Clock Pulse Width (t_{pw}) = t_{Hold}
Minimum Clock Period = $t_{Setup} + t_{pd} + t_{pw}$
(with $t_{pw} = t_{Skew} + t_{Hold} - t_{pd}$)
$= t_{Setup} + t_{pd} + t_{Skew} + t_{Hold} - t_{pd}$
$= t_{Setup} + t_{Skew} + t_{Hold}$

$$f_{max} = \frac{1}{t_{Setup} + t_{Skew} + t_{Hold}}$$

DEFINITIONS

t_{Hold}	Time data must be present after latching edge of clock to be recognized
t_L	Time to recognize and latch data in master portion of master-slave flip-flop
t_{pd}	Propagation delay from latching edge of clock to output
t_{Setup}	Time data must be present before latching edge of clock to be recognized
t_{Skew}	Clock skew time
t_{pw}	Clock positive pulse width

FIGURE 4 – UNIVERSAL CLOCKED SHIFT REGISTER