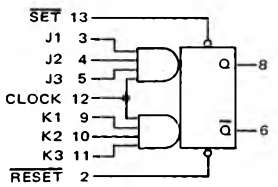
MC3155F • MC3055F
MC3155L • MC3055L, P

(54H72J) (74H72J, N)



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

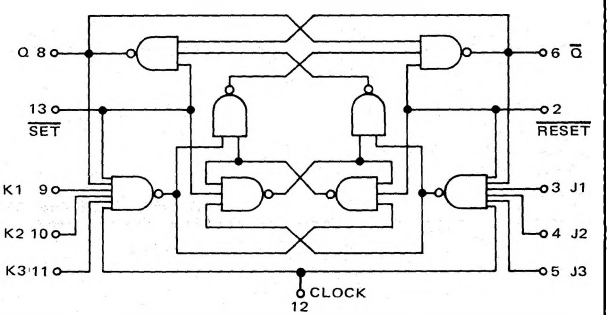
$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

Input Loading Factor:
J, K, CLOCK = 1
$\overline{SET}$, $\overline{RESET}$ = 2

Output Loading Factor = 10

Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 10 ns typ
Operating Frequency = 30 MHz typ

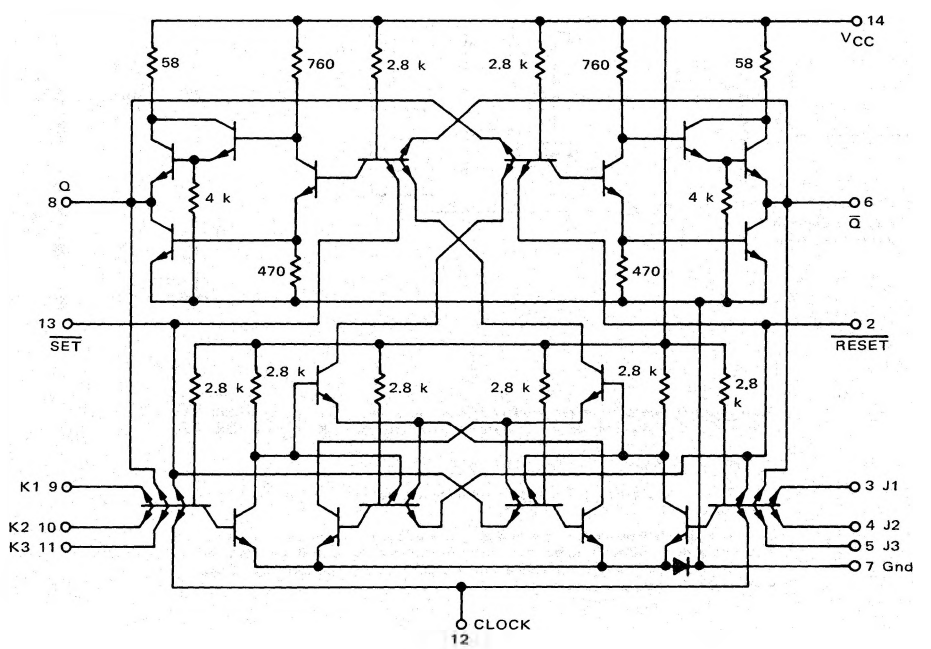
This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. $\overline{SET}$ and $\overline{RESET}$ inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs.



Pin numbers for the 54H72F/74H72F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3155F,L/3055F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H72F/74H72F	6	5	7	8	9	10	11	12	1	13	14	2	3	4

CIRCUIT SCHEMATIC



See General Information section for packaging.

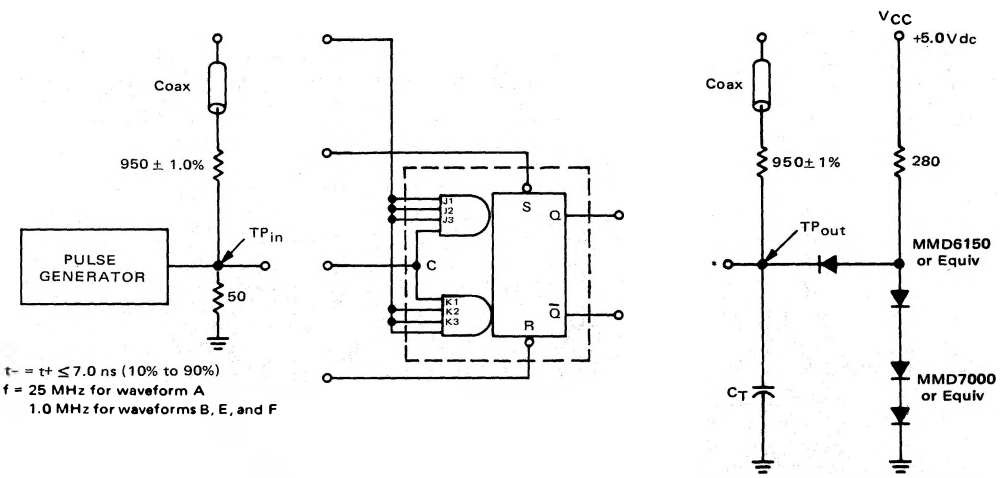
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state, and application of a logic "0" to the $\overline{RESET}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{SET}$ and $\overline{RESET}$ inputs override the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



t- = t+ ≤ 7.0 ns (10% to 90%)
f = 25 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$ and $\overline{RESET}$. Only one pulse generator is required for J, K, and CLOCK tests.

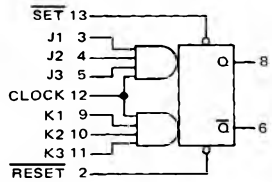
*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
	mA			Volts						
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}
MC3155	20	-2.0	1.0	0.4	2.4	4.0	2.0	0.8	4.5	5.5
MC3055	20	-2.0	1.0	0.4	2.4	4.0	2.0	0.8	4.75	5.25

Characteristic		Symbol	Pin Under Test	MC3155 Test Limits −55 to +125°C Min	Max	Unit	MC3055 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current	J	I_F	3	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	3	-	2*, 4, 5, 12	-	-	-	14	7
	K		9	-	-2.0		-	-2.0		-	-	-	9	-	10, 11, 12, 13*	-	-	-		
	$\overline{Set}$		13	-	-4.0		-	-4.0		-	-	-	13	-	3, 4, 5, 9, 10, 11	-	-	-		
	$\overline{Reset}$		2	-	-4.0		-	-4.0		-	-	-	2	-	3, 4, 5, 9, 10, 11	-	-	-		
	Clock		12	-	-2.0		-	-2.0		-	-	-	12	-	2*, 3, 4, 5, 9, 10, 11	-	-	-		
			12	-	-2.0		-	-2.0		-	-	-	12	-	3, 4, 5, 9, 10, 11, 13*	-	-	-		
Leakage Current	J	I_{R1}	3	-	50	μAdc	-	50	μAdc	-	-	-	-	3	-	-	-	-	14	2,4,5,7,12
	K		9	-	50		-	50		-	-	-	-	9	-	-	-	-		7,10,11,12,13
	$\overline{Set}$		13	-	100		-	100		-	-	-	-	13	-	-	-	-		7,9,10,11,12
	$\overline{Reset}$		2	-	100		-	100		-	-	-	-	2	-	-	-	-		3,4,5,7,12
	Clock		12	-	50		-	50		-	-	-	-	12	-	-	-	-		2,3,4,5,7,9,10,11,13
	J	BV_{in}	3	5.5**	-	Vdc	5.5**	-	Vdc	-	-	3	-	-	-	-	-	-	14	2,4,5,7,12
	K		9		-			-		-	-	9	-	-	-	-	-	-		7,10,11,12,13
	$\overline{Set}$		13		-			-		-	-	13	-	-	-	-	-	-		7,9,10,11,12
	$\overline{Reset}$		2		-			-		-	-	2	-	-	-	-	-	-		3,4,5,7,12
	Clock		12		-			-		-	-	12	-	-	-	-	-	-		2,3,4,5,7,9,10,11,13
Output																				
Output Voltage		V_{OL}	6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	2	13	14	-	7
			8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	13	2	14	-	7
		V_{OH}	6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	13	2	14	-	7
			8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	2	13	14	-	7
Short-Circuit Current		I_{SC}	6	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	14	2, 6, 7, 12
			8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	14	7, 8, 12, 13
Power Requirements																				
Power Supply Drain		I_{PD}	14	-	25	mAdc	-	25	mAdc	-	-	-	-	-	-	-	-	-	14	2,3,4,5,7,9,10,11,12
			14	-	25	mAdc	-	25	mAdc	-	-	-	-	-	-	-	-	-	14	3,4,5,7,9,10,11,12,13

*Momentarily ground pin prior to taking measurement.

**Tested @ 25°C only.

TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	$\overline{Q}$	LIMITS		
		C	J, K	$\overline{R}$	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	A	2.4 V	2.4 V	†	†	25	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	2.4 V	C	D	–	27	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	2.4 V	C	D	–	21	ns
Turn-On Delay	t_{sd-}	2.4 V	2.4 V	E	F	G	H	–	24	ns
Turn-Off Delay	t_{sd+}	2.4 V	2.4 V	E	F	G	H	10	13	ns
Enable Voltage ☆	V_{EN}	B	2.0 V	2.4 V	2.4 V	†	†	†	–	–
Inhibit Voltage ☆	V_{INH}	B	0.8 V	2.4 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.
☆Tested at all temperatures.

VOLTAGE WAVEFORMS AND DEFINITIONS