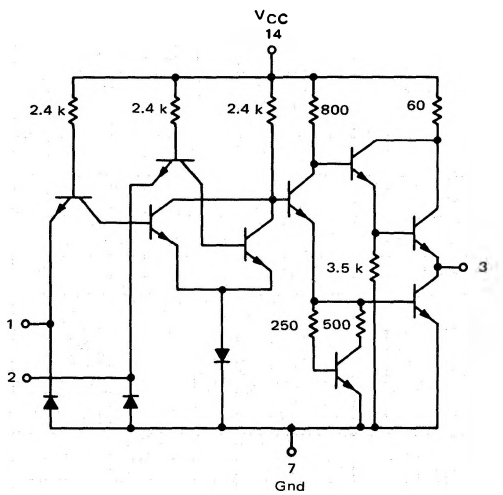
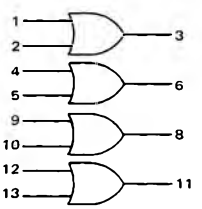
MC3103F • MC3003F
MC3103L • MC3003L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



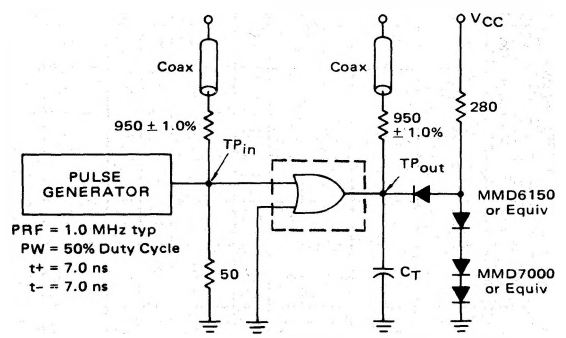
This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

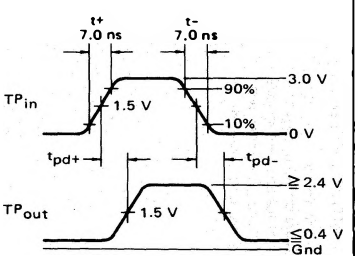


Positive Logic: 3 = 1 + 2
Negative Logic: 3 = 1 • 2

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





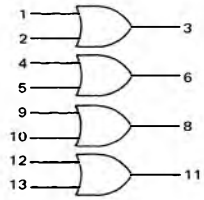
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA				Volts									
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
MC3103	−55°C	20	-2.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	
MC3103	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	
MC3103	+125°C	20	-2.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	
MC3003	0°C	20	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	
MC3003	+25°C	20	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	
MC3003	+75°C	20	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3103 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3003 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	1	-	2*	-	-	-	14	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	1	*	-	-	-	14	2,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	*	-	-	-	14	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	*	-	-	14	-	7
Output Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1	-	-	-	2*	-	-	14	-	7
	V_{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	-	1	-	-	2*	-	-	14	-	7
Short-Circuit Current	I_{SC}	3	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	1,2*	-	-	-	14	3,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	45	-	-	-	-	-	45	-	-	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	34	-	34	-	34	-	34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	-	-	14	7
	I_{PDL}	14	-	58	-	58	-	58	-	58	-	58	-	58	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{pd-}	1,3	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	7
Turn-Off Delay	t_{pd+}	1,3	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	*	-	14	-	-	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}