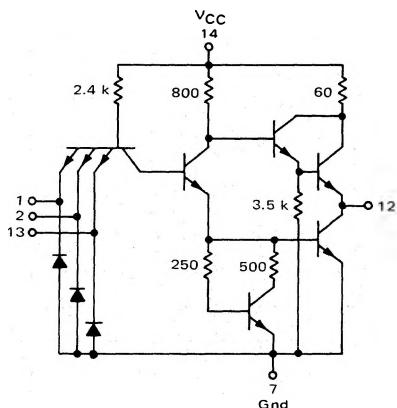


TRIPLE  
3-INPUT "NAND" GATE

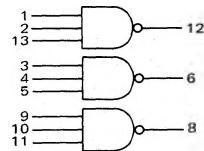
MC3100/MC3000 series

**MC3105F • MC3005F**  
**MC3105L • MC3005L,P**  
(54H10J) (74H10J,N)

CIRCUIT SCHEMATIC  
1/3 OF CIRCUIT SHOWN



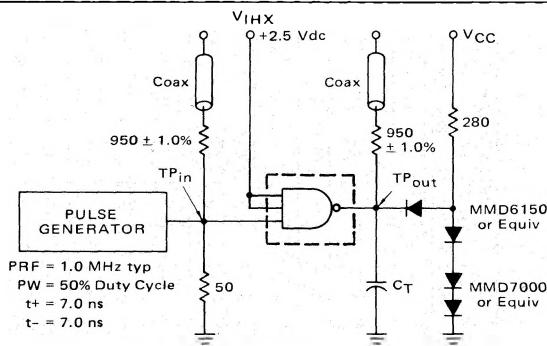
This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic:  $12 = \overline{1} \cdot \overline{2} \cdot \overline{13}$   
Negative Logic:  $12 = \overline{1} + \overline{2} + \overline{13}$

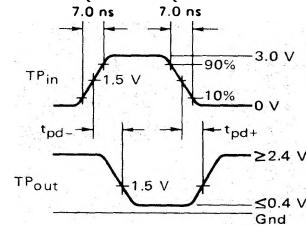
Input Loading Factor = 1  
Output Loading Factor = 10  
Total Power Dissipation = .66 mW typ/pkg  
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$C_T = 25 \text{ pF}$  = total parasitic capacitance, which includes probe, wiring, and load capacitances.

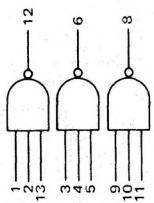
The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.



## MC3105, MC3005 (continued)

### ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



TEST CURRENT/VOLTAGE VALUES											
Characteristic	Symbol	Volts									
		I <sub>OL</sub>	I <sub>OH</sub>	I <sub>in</sub>	I <sub>b</sub>	V <sub>h</sub>	V <sub>ih</sub>	V <sub>f</sub>	V <sub>R</sub>	V <sub>max</sub>	V <sub>cc</sub>
@ Test Temperature											
Forward Current	I <sub>F</sub>	-2.0	-2.0	-	-	2.0	0.4	2.4	4.0	-	5.0
Leakage Current	I <sub>R</sub>	1	-	50	-	50	-	50	-	50	4.5
Breakdown Voltage	BV <sub>in</sub>	1	-	5.5	-	-	5.5	-	-	7.0	5.5
Clamp Voltage	V <sub>D</sub>	1	-	-	-1.5	-	-1.5	-	-	-	4.5
Output	V <sub>OT</sub>	12	-	0.4	-	0.4	-	0.4	Ydc	-	5.5
Output Voltage	V <sub>SC</sub>	12	-	2.4	-	2.4	-	2.5	-	12	-
Short-Circuit Current	I <sub>SC</sub>	12	-40	-100	-40	-100	-40	-100	-40	-100	-
MC3105 Test Limits											
Pin Under Test		MC3105 Test Limits		-55°C		+25°C		+125°C		0°C	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Input		-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0
Forward Current	I <sub>F</sub>	1	-	50	-	50	-	50	-	50	-
Leakage Current	I <sub>R</sub>	1	-	50	-	50	-	50	-	50	-
Breakdown Voltage	BV <sub>in</sub>	1	-	5.5	-	-	5.5	-	-	Ydc	-
Clamp Voltage	V <sub>D</sub>	1	-	-	-1.5	-	-1.5	-	-	Ydc	-
Output	V <sub>OT</sub>	12	-	0.4	-	0.4	-	0.4	Ydc	12	-
Output Voltage	V <sub>SC</sub>	12	-	2.4	-	2.4	-	2.5	-	12	-
Short-Circuit Current	I <sub>SC</sub>	12	-40	-100	-40	-100	-40	-100	-40	-100	-
MC3005 Test Limits											
Pin Under Test		MC3005 Test Limits		-55°C		+25°C		+125°C		0°C	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Input		-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0	-2.0
Forward Current	I <sub>F</sub>	1	-	50	-	50	-	50	-	50	-
Leakage Current	I <sub>R</sub>	1	-	50	-	50	-	50	-	50	-
Breakdown Voltage	BV <sub>in</sub>	1	-	5.5	-	-	5.5	-	-	Ydc	-
Clamp Voltage	V <sub>D</sub>	1	-	-	-1.5	-	-1.5	-	-	Ydc	-
Output	V <sub>OT</sub>	12	-	0.4	-	0.4	-	0.4	Ydc	12	-
Output Voltage	V <sub>SC</sub>	12	-	2.4	-	2.4	-	2.5	-	12	-
Short-Circuit Current	I <sub>SC</sub>	12	-40	-100	-40	-100	-40	-100	-40	-100	-
Switching Parameters											
Turn-On Delay	t <sub>pd+</sub>	1, 12	-	-	-	10	-	-	10	-	-
Turn-Off Delay	t <sub>pd-</sub>	1, 12	-	-	-	10	-	-	10	-	-
Power Requirements (Total Device)											
Maximum Power Supply Current	I <sub>max</sub>	14	-	20	-	-	20	-	mAdc	-	-
Power Supply Drain	I <sub>PDH</sub>	14	-	30	-	30	-	30	mAdc	-	-
I <sub>PDL</sub>	14	-	12.6	-	12.6	-	12.6	-	mAdc	-	-
Switching											
Parameters									Pulse In	Pulse Out	
Turn-On Delay	t <sub>pd+</sub>	1, 12	-	-	10	-	-	10	-	-	-
Turn-Off Delay	t <sub>pd-</sub>	1, 12	-	-	10	-	-	10	-	-	-

\* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.