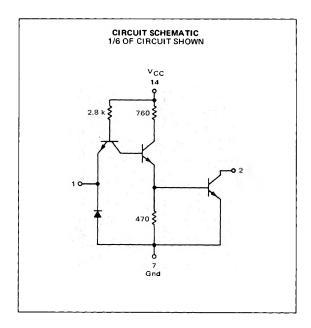
## MC3100/MC3000 series

**HEX INVERTER** 

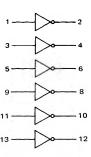
## MC3109F · MC3009F MC3109L · MC3009L,P

(54H05J)

(74H05J,N)



This device consists of six independent inverting gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



Positive Logic:  $2 = \overline{1}$ 

Input Loading Factor = 1 Output Loading Factor = 10 Total Power Dissipation = 90 mW typ/pkg Propagation Delay Time = 8 ns typ

Pin numbers for the 54H05F/74H05F device are shown in the chart. These devices are available on special request.

DEVICE						PIN	NU	MBE	RS					
MC3109F,L/3009F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H05F/74H05F	1	14	3	2	5	6	11	8	7	10	9	12	13	4

## SWITCHING TIME TEST CIRCUIT AND WAVEFORMS **TPout** Vсс 280 -3.0 V 10% PULSE GENERATOR tpdtpd+ PRF = 1.0 MHz typ ≥2.4 V PW = 50% Duty Cycle TPout 井cτ \$ 50 t+ = 7.0 ns <0.4 V t- = 7.0 ns Gnd CT = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

V<sub>max</sub> V<sub>cc</sub> V<sub>cct</sub> V<sub>ccн</sub>

Volts

V<sub>RH</sub>

lor I'm

TEST CURRENT / VOLTAGE VALUES

## **ELECTRICAL CHARACTERISTICS**

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

11/2/2	3 - 4	5	8 - 6	11	13 -12

Pin														MC	MC3109	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	
Hand Hand Hand Hand Hand Hand Hand Hand															<u> </u>	+125°C		-		0.8	-	0	2.4	4.0	5.5		5.0	4.5	5.5	
															)	0,0				1.	-	-	2.5	4.0	5.5		5.0	4.75	5.25	
														¥	3000	+25°C		1.0	_	_	_		2.5	4.0	5,5	7.0	5.0	4.75	5.25	
																+75°C		-		0.9	_		2.5	4.0	5.5	-	5.0	4.75	5.25	-
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			Pin		Ž	C3109	Test Li				_	AC3009	Test Lir								TEST (	URRENT	/VOLTAGE	APPLIED TO	PINS L	ISTED B	TOW:			
Symbol   Year   Min   Max   Min			Ilnder	ī'	25°C	+	25°C	+	125°C	-	ပ္စ	+	25°C	+	ر ک ک				-	-	1		1							
Francisco   Fran	Characteristic	Symbol	Test	Win	Max	-	-	<	$\vdash$	×	$\vdash$	-	$\vdash$	-		_	_ŏ	<sup>5</sup>	٥-	-		-	>"	V <sub>RH</sub>	VCEX	Vmax	<mark>&gt;</mark>	Vcct	V <sub>ссн</sub>	
Harmonian   Harm	Input Forward Current	IF.	-	2.	-2.0		-2.0		-2. (	-			-2.0		-2.0			Ŀ	<u> </u>	1	L	-		,		-		-	14*	* -
Figure   1   1   2   2   2   2   2   2   2   2	Leakage Current	l <sub>R</sub>	1	'	20	1.:	20	-	20	-	-	-	20		20	μAdc	,	•	,	'	'		1		,		1		14	* 1
Vol. 2 - 0.4 - 0.4 - 0.4 - 0.4 - 0.4 - 0.4 Vdc 2 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	Breakdown Voltage		1	-	•	5.5	_	'	r	-	-	5.5	-			Vdc	ı	-	1	'	1		-						14	* 4
Vol.         2         0.4         0.4         0.4         0.4         Vol.         0.4	Clamp Voltage	$^{\rm V}_{ m D}$	1	1,7	'	1	1. 1.			-	-	'	-1.5	1_		Vdc	,		-	!	Ŀ			,		1		14	Ŷ.	* L
CEX   2   2   2   2   2   2   2   2   2	Output Output Voltage	Vol	23		0.4		0.4		0.4	-	-		0.4	-	0.4	Vdc	. 67	,	1	1	-					1	1	14	S . I	* 4
1   1   1   1   2   2   2   2   2   2	Output Leakage Current	LCEX	2		250	-	250	-	250		-	_	250		250	μAdc		,		-		'			2	1	-	14	1.7	**
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Power Requirements (Total Device) Maximum Power Supply Current		14				37.5		- '	'			37.5		- 1	mAdc		,	,	,	-		,			14		'		1,3,5,7, 9,11,13
Selfaborary Fig. 1.4 - 2.6 - 2	Power Supply Drain		14	1	28	1, 1	28	1	28	'	-	-	28		28	mAdc		1	'			,	,	1,3,5,7, 9,11,13	,				14	1
Selay 'pd- 1,2 15 18 18 18 18 18 18 18		IPDL	14		26	1	26	-	26	-	-	-	26	1	26	mAdc		1		'	'		,		,	'			14	1,3,5,7, 9,11,13
elay 'pd- 1,2 15 15 18 - 18 - 18 18 18 18 18 18 18 18 18 18	Switching Parameters								_	_	_	_					Pulse	Pulse												
th+ 1,2 18 18 14 -	Turn-On Delay	tpd-	1,2	1	•	,	15	1	1	'		•	12	'	1	su	-	67	'	'	'	,	,			,	14	1		* -
	Turn-Off Delay	tpd+	1,2	.1	1		18		'	'		-	18	'	!	su	-	22	'	'		,				,	14	'		* -

\* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.