MC33566

Smart Voltage Regulator for Peripheral Card Applications

The MC33566 Low Dropout Regulator is designed for computer peripheral card applications complying with the *instantly available requirements* as specified by ACPI objectives. The MC33566 permits glitch–free transitions from "sleep" to "active" system modes and has internal logic circuitry to detect whether the system is being powered from the motherboard main 5.0 V power supply or the 3.3 V aux supply.

The MC33566 provides a regulated output voltage of 3.3 V via either an internal low dropout 5.0 V–to–3.3 V voltage regulator or an external P–channel MOSFET, depending on the operating status of the system in which the card is installed. During normal operating mode (5.0 V main supply available) the 3.3 V output is provided from the internal low dropout regulator at an output current of 0.4 A. When the motherboard enters sleep mode, the MC33566 operates from the 3.3 V aux supply and routes the aux current to the output via the external P–channel MOSFET bypass transistor controlled by the *drive out* pin. As a result, the output voltage provided to the peripheral card remains constant at 3.3 V even during host systems transitions to and from sleep mode.

MC33566 Features:

- Output Current up to 0.4 A
- Excellent Line and Load Regulation
- Low Dropout Voltage
- Prevents Reverse Current Flow During Sleep Mode
- Glitch–Free Transfer from Sleep Mode to Active Mode
- Compatible with *Instantly Available* PC Systems

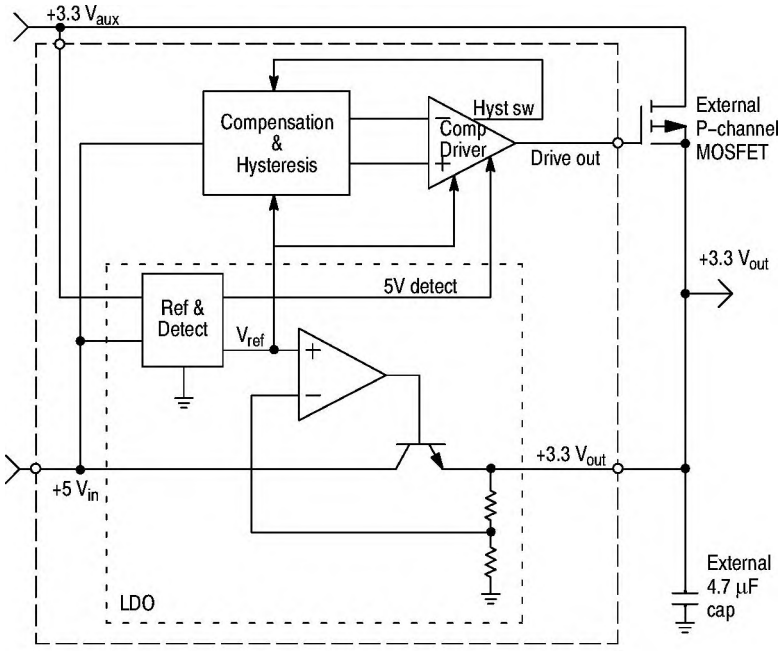

Figure 1. Simplified Block Diagram

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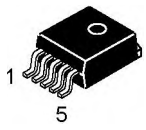
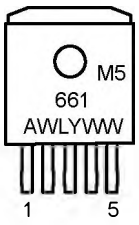
MARKING DIAGRAM



D²PAK
D2T SUFFIX
CASE 936A



Pin 1. Vaux
2. V_{in}
3. Gnd
4. V_{out}
5. Drv

Note: Tab is ground

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC33566D2T–1	D²PAK	50 Units/Rail
MC33566D2T–1RK	D²PAK	2500 Tape & Reel

PIN ASSIGNMENTS AND FUNCTIONS

Pin #	Pin Name	Pin Description
1	+3.3 V_{aux}	Auxiliary input. Typical voltage 3.3 V.
2	+5.0 V_{in}	This is the input supply for the IC. Typical voltage 5.0 V. (Notes 1 and 2)
3	Gnd	Logic and power ground.
4	+3.3 V_{out}	3.3 V output provided to the application circuit (output current is sourced to this pin from the 5.0 V input.)
5	Drive out	This output drives a P–channel MOSFET with up to 2000 pF of “effective” gate capacitance. Recommended devices are the MMFT5P03HD and MTSF1P02HD. Drive out has active internal pull–up and pull–down circuitry to guarantee fast transitions.

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
+5.0 V_{in} Supply Voltage	V_{in}	7.0	Vdc
	V_{in}	–0.5 (Note 3)	Vdc
Operating Ambient Temperature	T_a	–5.0 to +85	°C
Operating Junction Temperature	T_J	– 5.0 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature	T_{stg}	– 55 to +150	°C
Package Thermal Resistance	$R_{\theta JA}$ (Note 4)	65	°C/W

AC ELECTRICAL SPECIFICATIONS (Notes 5, 6, and 7)

Characteristic	Symbol	Min	Typ	Max	Unit
Drive High Delay (V_{in} ramping up) C_{drive} = 1.2 nF, measured from +5.0 V_{in} = $V_{thresHi}$ to V_{Drive} = 2.0 V	t_{DH}	–	0.5	3.5	μS
Drive Low Delay (V_{in} ramping down) C_{drive} = 1.2 nF, measured from +5.0 V_{in} = $V_{thresLo}$ to V_{Drive} = 2.0 V	t_{DL}	–	0.5	3.5	μS

1. See 5.0 V Detect Thresholds Diagram.
2. Recommended source impedance for 5.0 V supply: ≤ 0.12 Ω. This will ensure that I_o x R_{source} < V_{hyst}, thus avoiding driveout toggling during 5.0 V detect threshold transitions.
3. V_{in} should not be allowed to go negative relative to ground.
4. Mounted on recommended minimum PCB pad on FR4, 2–oz. copper circuit board.
5. AC specs are guaranteed by characterization, but not production tested after characterization.
6. See Figure 3. Application Block Diagram.
7. See Timing Diagram.

DC ELECTRICAL CHARACTERISTICS (Note 8)

Characteristic	Symbol	Min	Typ	Max	Unit
+5.0 V_{in} Supply Voltage Range	+5.0 V_{in}	4.35	5.0	5.5	Vdc
Reverse Leakage Current from Output	$I_{reverse}$	–	–	25	μA
V_{aux} Quiescent Current	I_{qaux}	–	–	2.0	mA
+5.0 V_{in} Quiescent Current, Operating	I_{qvin}	–	–	10	mA
Load Capacitance (Note 9)	C_{load}	4.7	22	–	μF
REGULATOR OUTPUT					
Output Voltage (4.35 V ≤ V_{in} ≤ 5.5 V, 0 mA ≤ I_o ≤ 400 mA) T_A = 25°C (T_J = –5°C to 150°C)	+3.3 V_{out}	 3.267 3.234	 3.30 3.30	 3.333 3.366	Vdc
In–to–Out Voltage (3.9 V ≤ V_{in} ≤ 4.35 V, V_{aux} = 3.3 V)	V_d	3.0	–	–	Vdc
Voltage Out at Max Voltage In (V_{in} = 7.0 V)	V_{outmax}	3.1	3.3	3.5	Vdc
Line Regulation (I_o = 400 mA)	Linereg	–	–	0.4	%
Load Regulation (I_o = 0 to 400 mA)	Loadreg	–	–	0.8	%
5.0 V DETECT					
Low Threshold Voltage (+5.0 V_{in} Falling, I_o = 400 mA)	$V_{thresLo}$	3.9	4.05	–	Vdc
High Threshold Voltage (+5.0 V_{in} Rising, I_o = 400 mA)	$V_{thresHi}$	–	4.2	4.35	Vdc
Hysteresis	V_{hyst}	0.05	–	–	Vdc
DRIVE OUTPUT					
Output Peak Source Current (+5.0 V_{in} > $V_{thresHi}$)	I_{peak}	15	–	–	mA
Output Peak Sink Current (+5.0 V_{in} < $V_{thresLo}$)	I_{peak}	15	–	–	mA
Low Output Voltage (I_{oL} = 200 μA, V_{in} < $V_{thresLo}$)	V_{oL}	–	100	200	mVdc
High Output Voltage (I_{oH} = 200 μA)	V_{oH}	3.4	–	–	Vdc

8. –5°C < T_a < 70°C, 4.35 V < V_{in} < 5.5 V, C_{load} ≥ 4.7 μF unless otherwise noted.
9. 4.7 μF minimum over temperature; 22 μF recommended; 500 mΩ ESR maximum.

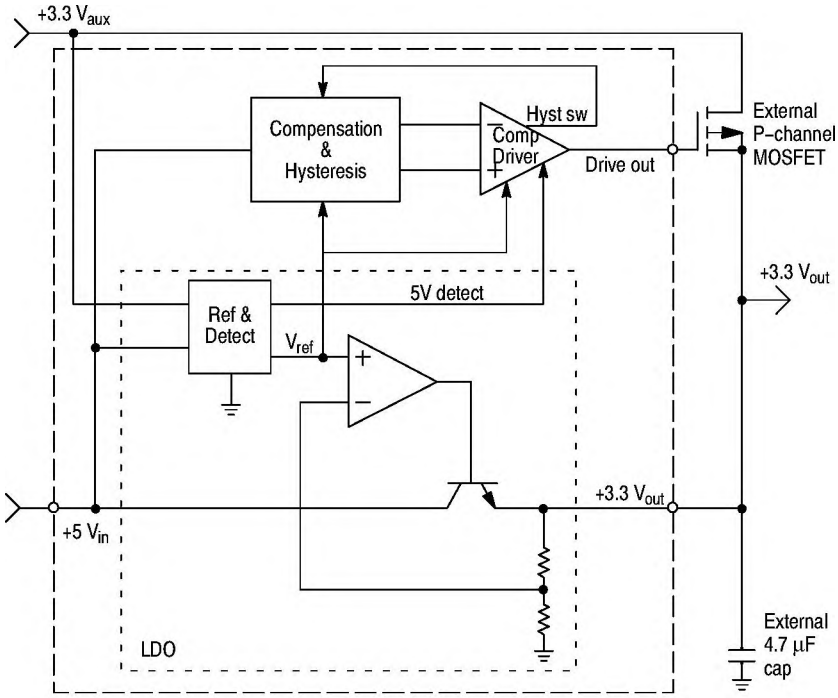


Figure 2. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Input Blocking – The internal NPN pass transistor of the LDO regulator ensures that no significant reverse current will flow from +3.3 V_{out} back to the +5.0 V_{in} input when the 5.0 V input is not powered and the 3.3 V_{in} supply is present.

5.0 Volt Detect – Internal circuitry detects the presence of the 5.0 V input supply. When the 5.0 V supply drops below a given threshold, the +3.3 V_{in} bypass transistor (an external P–channel MOSFET) is enabled. The 5.0 V detect logic is active throughout the entire range of ramp–up from 0 to 5.5 V. Additionally, the drive out signal is never turned ON or OFF inappropriately during ramp–up of the +5.0 V_{in} supply. Also, +3.3 V_{out} never drops below 3.0 V while +5.0 V_{in} is above the 5.0 V detect minimum threshold.

Glitch–free Transfer – The design of the 5.0 V detect circuitry and drive out control circuitry guarantees that the +3.3 V_{out} will not exceed the output voltage specification listed in the table of DC Operating Specifications even with +5.0 V_{in} ramping up and down at the extremes of the slew rates in the table of AC Operating Specifications.

Offset Voltage Performance – To ensure performance when external offsets are present on the +5.0 V_{in} and +3.3 V_{in} power inputs, the device has been designed to be capable of operating with either one or both of these inputs rising from or falling to zero volts, or with offsets of 0.05 V to 0.9 V as the inputs ramp up and down.

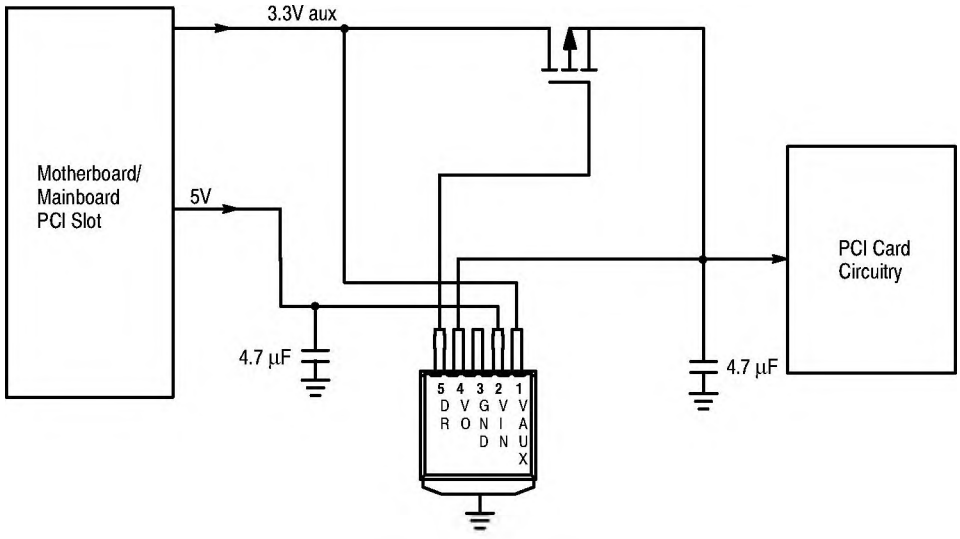
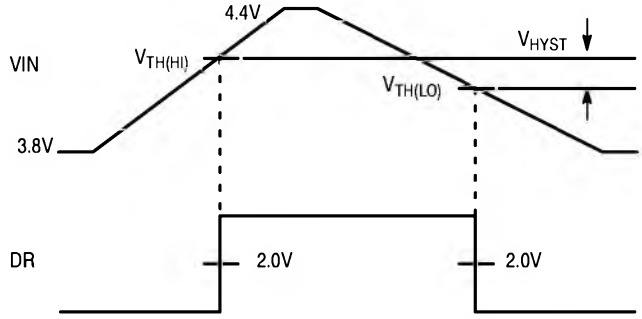
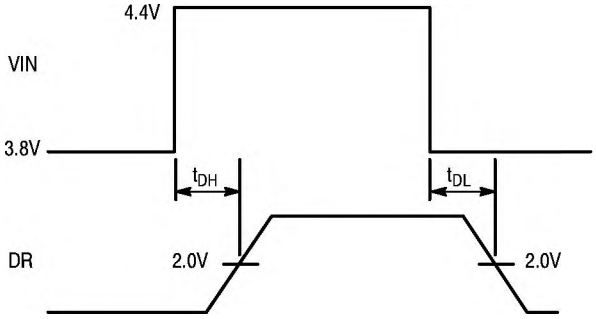


Figure 3. Application Block Diagram



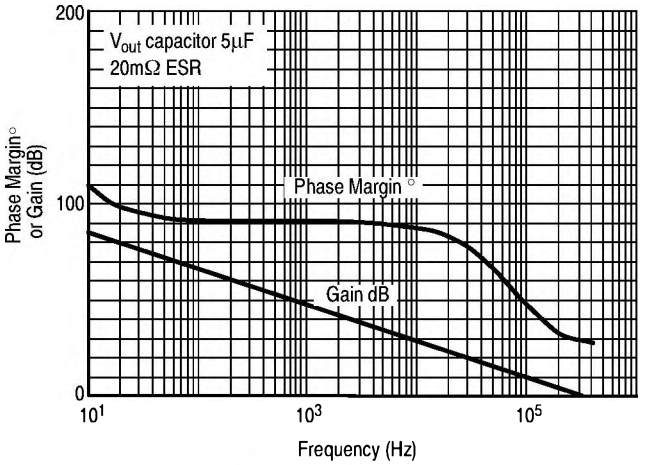
NOTE:
(1) V_{in} rise and fall times (10% to 90%) to be ≥ 100 μs.

Figure 4. 5.0 V Detect Thresholds Diagram



NOTE:
(1) V_{in} rise and fall times (10% to 90%) to be ≤ 100 ns.

Figure 5. Timing Diagram



NOTE: V_{out} capacitor ≥ 4.7 μF over operating temperature range.
Maximum ESR permissable = 500 mΩ over operating temperature range.

Figure 6. Predicted Gain and Phase at Zero Load Current

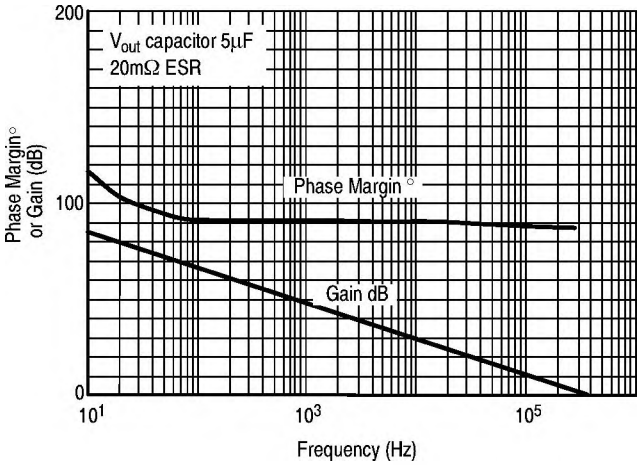


Figure 7. Predicted Gain and Phase at Full Load Current