Preliminary Information

1.5 A Switch-Mode Power Supply with Linear Regulator

The 33701 provides the means to efficiently supply the Power QUICC™ I, II, and other families of Motorola microprocessors and DSPs. The 33701 incorporates a high-performance switching regulator, providing the direct supply for the microprocessor's core, and a low dropout (LDO) linear regulator control circuit providing the microprocessor I/O and bus voltage.

The switching regulator is a high-efficiency synchronous buck regulator with integrated 50 mΩ N-channel power MOSFETs to provide protection features and to allow space-efficient, compact design.

The 33701 incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system.

Features

- Operating Voltage: 2.8 V to 6.0 V
- High-Accuracy Output Voltages
- Fast Transient Response
- Switcher Output Current Up to 1.5 A
- Undervoltage Lockout
- Power Sequencing
- Programmable Watchdog Timer
- Voltage Margining via I^{2}C™ Bus
- Overcurrent Protection
- Reset with Programmable Power-ON Delay
- Enable Inputs

I^{2}C is a trademark of Phillips Corporation.

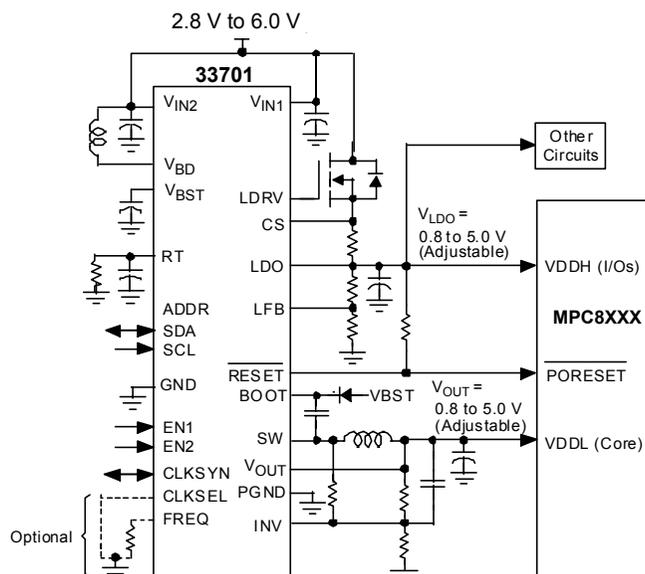---

33701

POWER SUPPLY INTEGRATED CIRCUIT
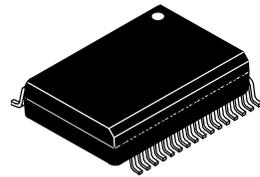
DWB SUFFIX
CASE 1324-02
32-LEAD SOICW

ORDERING INFORMATION

Device	Temperature Range (T$_A$)	Package
PC33701DWB/R2	–40 to 85°C	32 SOICW

33701 Simplified Application Diagram

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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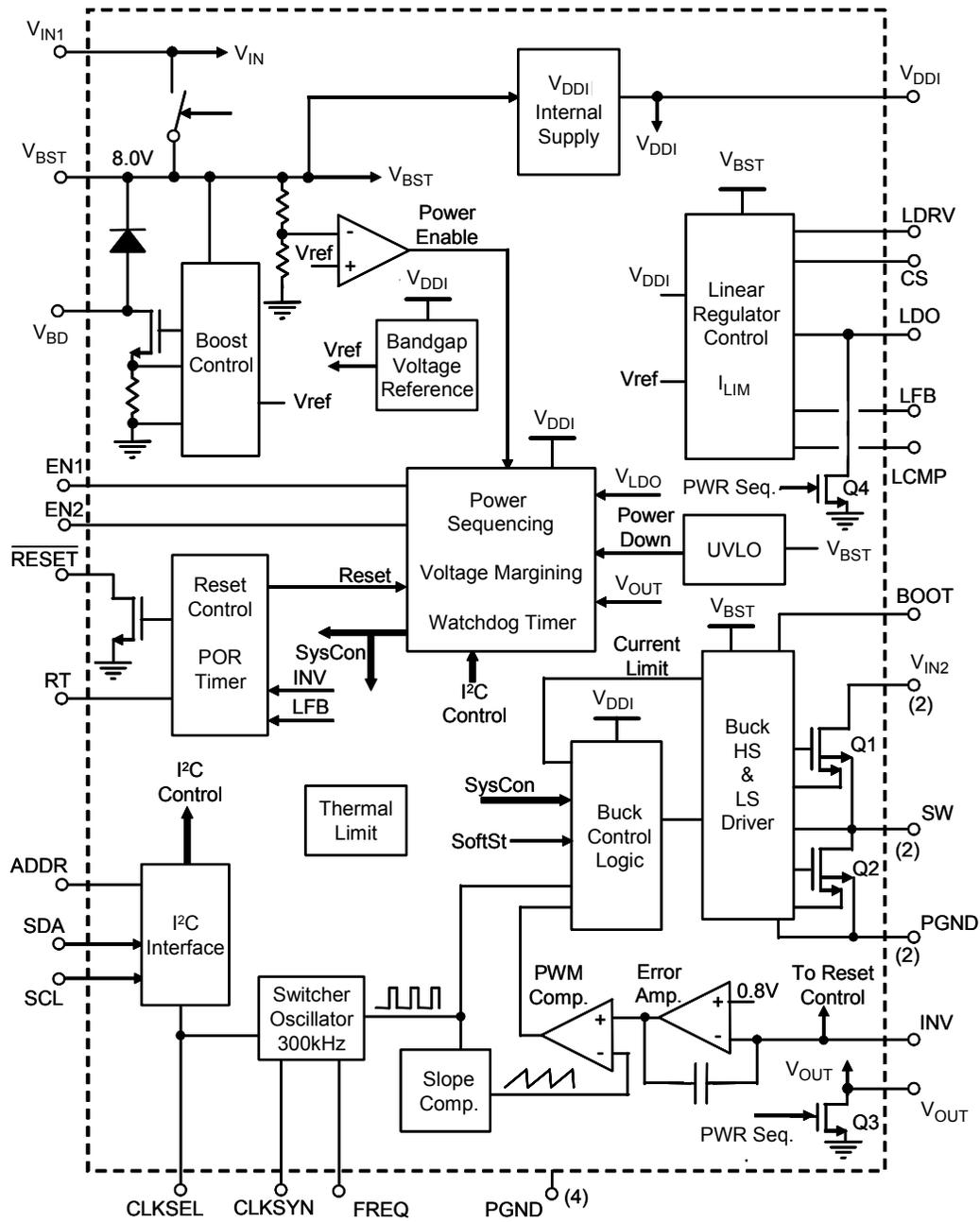
Figure 1. 33701 Simplified Block Diagram

```
              FREQ  ┌──1 •      32──┐  CLKSYN
               INV  ┌──2        31──┐  CLKSEL
             V_OUT  ┌──3        30──┐  RESET
             V_IN2  ┌──4        29──┐  RT
             V_IN2  ┌──5        28──┐  EN2
                SW  ┌──6        27──┐  EN1
                SW  ┌──7        26──┐  ADDR
               GND  ┌──8        25──┐  GND
               GND  ┌──9        24──┐  GND
              PGND  ┌──10       23──┐  V_DD1
              PGND  ┌──11       22──┐  V_IN1
              V_BD  ┌──12       21──┐  LDRV
             V_BST  ┌──13       20──┐  CS
              BOOT  ┌──14       19──┐  LDO
               SDA  ┌──15       18──┐  LFB
               SCL  ┌──16       17──┐  LCMP
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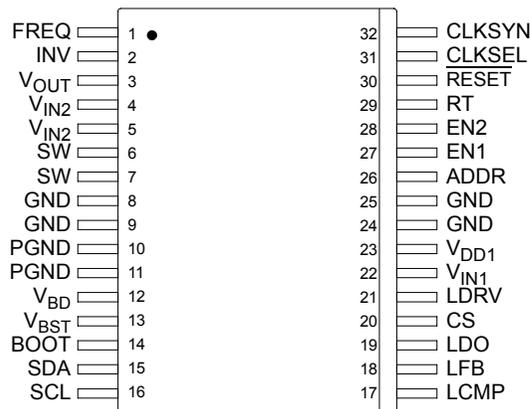
PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1	FREQ	Oscillator Frequency	This selection switcher pin can be adjusted by connecting external resistor R_F to the FREQ pin. The default switching frequency (FREQ pin left open or tied to V_{DDI}) is set to 300 kHz.
2	INV	Inverting Input	Buck Controller Error Amplifier inverting input.
3	V_{OUT}	Output Voltage	Output voltage of the buck converter. Input pin of the switching regulator power sequence control circuit.
4, 5	V_{IN2}	Input Voltage 2	Buck regulator power input. Drain of the high-side power MOSFET.
6, 7	SW	Switch	Buck regulator switching node. This pin is connected to the inductor.
8, 9 24, 25	GND	Ground	Analog ground of the IC, thermal heatsinking.
10, 11	PGND	Power Ground	Buck regulator power ground.
12	V_{BD}	Boost Drain	Drain of the internal boost regulator power MOSFET.
13	V_{BST}	Boost Voltage	Internal boost regulator output voltage. The internal boost regulator provides a 20 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the V_{BST} pin is 8.0 V nominal.
14	BOOT	Bootstrap	Bootstrap capacitor input.
15	SDA	Serial Data	I^2C bus pin. Serial data.
16	SCL	Serial Clock	I^2C bus pin. Serial clock.
17	LCMP	Linear Compensation	Linear regulator compensation pin.
18	LFB	Linear Feedback	Linear regulator feedback pin.
19	LDO	Linear Regulator	Input pin of the linear regulator power sequence control circuit.
20	CS	Current Sense	Current sense pin of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor R_S is sensed between the CS and LDO pins. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor R_S.
21	LDRV	Linear Drive	LDO gate drive of the external pass N-channel MOSFET.
22	V_{IN1}	Input Voltage 1	The input supply pin for the integrated circuit. The internal circuits of the IC are supplied through this pin.

PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Formal Name	Definition
23	V_{DDI}	Power Supply	Internal supply voltage.
26	ADDR	Address	I²C address selection. This pin can be either left open, tied to V_{DDI}, or grounded through a 10 kΩ resistor.
27	EN1	Enable 1	Enable 1 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determine operation mode and type of power sequencing of the IC.
28	EN2	Enable 2	Enable 2 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determine operation mode and type of power sequencing of the IC.
29	RT	Reset Timer	This pin allows programming the Power-ON Reset delay by means of an external RC network.
30	$\overline{RESET}$	Reset Overbar	The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.
31	CLKSEL	Clock Selection	This pin sets the CLKSYN pin either as an oscillator output or synchronization input pin. The CLKSEL pin is also used for the I²C address selection.
32	CLKSYN	Clock Synchronization	Oscillator output/synchronization input pin.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Supply Voltage	V_{IN1}, V_{IN2}	-0.3 to 7.0	V
Switching Node	SW	-1.0 to 7.0	V
Buck Regulator Bootstrap Input (BOOT - SW)	BOOT	-0.3 to 8.5	V
Boost Regulator Output	V_{BST}	-0.3 to 8.5	V
Boost Regulator Drain	V_{BD}	-0.3 to 9.5	V
$\overline{RESET}$ Drain Voltage	$\overline{RESET}$	-0.3 to 7.0	V
Enable Pins (EN1, EN2)	–	-0.3 to 7.0	V
Logic Pins (SDA, SCL, CLKSYN)	–	-0.3 to 7.0	V
Analog Pins (INV, V_{OUT}, $\overline{RESET}$)	–	-0.3 to 7.0	V
Analog Pins (LDRV, LFB, LDO, LCMP, CS)	–	-0.3 to 8.5	V
Analog Pins (CLKSEL, ADDR, RT, FREQ, V_{DDI})	–	-0.3 to 3.6	V
ESD Voltage 　Human Body Model (Note 1) 　Machine Model (Note 2)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation (T_A = 85°C) (Note 3)	P_D	TBD	W
Lead Soldering Temperature (Note 4)	T_{SOLDER}	260	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	68	°C/W
Thermal Resistance, Junction to Base (Note 6)	$R_{\theta JB}$	18	°C/W

OPERATING CONDITIONS

Supply Voltage (V_{IN1}, V_{IN2})	V_{IN1}, V_{IN2}	2.8 to 6.0	V
Operational Package Temperature (Ambient Temperature)	T_A	-40 to 85	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω).

2. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).

3. Maximum power dissipation at indicated junction temperature.

4. Lead soldering temperature limit is for 10 seconds maximum duration. Contact Motorola Sales Office for device immersion soldering time/temperature limits.

5. Thermal resistance measured in accordance with EIA/JESD51-2.

6. Theoretical thermal resistance from the die junction to the exposed pins.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions -40°C ≤ T$_J$ ≤ 125°C unless otherwise noted. Input voltages V$_{IN1}$ = V$_{IN2}$ = 3.3 V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Operating Voltage Range (V$_{IN1}$, V$_{IN2}$)	V$_{IN}$	2.8	–	6.0	V
Start-Up Voltage Threshold (Boost Switching)	V$_{ST}$	–	1.6	1.8	V
V$_{BST}$ Undervoltage Lockout	V$_{BST\_UVLO}$	–	6.0	–	V
Input DC Supply Current (Normal Operation Mode, Enabled)	I$_{IN}$	–	60	–	mA
V$_{IN1}$ Pin Input Supply Current (EN1 = EN2 = 0)	I$_{IN1}$	–	9.0	–	mA
V$_{IN2}$ Pin Input Leakage Current (EN1 = EN2 = 0)	I$_{IN2}$	–	TBD	–	μA
V$_{DDI}$ Internal Supply Voltage	V$_{DDI}$	3.0	–	3.3	V
V$_{DDI}$ Maximum Output Current	I$_{DDI}$	–	TBD	–	μA
BUCK CONVERTER					
Buck Converter Output Voltage Range I$_{VOUT}$ = 15 mA to 1.5 A, V$_{IN1}$ = V$_{IN2}$ = 2.8 V to 6.0 V	V$_{OUT}$	0.8	–	5.0	V
Buck Converter Feedback Voltage I$_{VOUT}$ = 15 mA to 1.5 A, V$_{IN1}$ = V$_{IN2}$ = 2.8 V to 6.0 V. No R$_B$ Resistor. Includes Load Regulation Error	V$_{INV}$	0.784	0.8	0.816	V
Buck Converter Voltage Margining Step	V$_{MVO}$	–	1.0	–	%
Buck Converter Line Regulation V$_{IN1}$ = V$_{IN2}$ = 2.8 V to 6.0 V, I$_{VOUT}$ = 1.5 A	REG$_{LNVO}$	-1.0	–	1.0	%
Buck Converter Load Regulation I$_{VOUT}$ = 15 mA to 1.5 A	REG$_{LDVO}$	-1.0	–	1.0	%
V$_{OUT}$ Input Leakage Current V$_{OUT}$ = 5.0 V	I$_{VOUTLK}$	–	TBD	–	μA
High-Side Power MOSFET Q1 R$_{DS(ON)}$ I$_D$ = 1.0 A, T$_A$ = 25°C, V$_{BST}$ = 8.0 V	R$_{DS(ON)}$	–	–	50	mΩ
Low-Side Power MOSFET Q2 R$_{DS(ON)}$ I$_D$ = 1.0 A, T$_A$ = 25°C, V$_{BST}$ = 8.0 V	R$_{DS(ON)}$	–	–	50	mΩ
Buck Converter Peak Current Limit (High Level)	I$_{H\_LIM}$	1.65	2.25	3.0	A
Buck Converter Valley Current Limit (Low Level)	I$_{L\_LIM}$	0.825	1.125	1.45	A
V$_{OUT}$ Pull-Down MOSFET Q3 Current Limit T$_A$ = 25°C, V$_{BST}$ = 8.0 V	I$_{Q3\_LIM}$	–	2.0	–	A
V$_{OUT}$ Pull-Down MOSFET Q3 R$_{DS(ON)}$ I$_D$ = 1.0 A, T$_A$ = 25°C, V$_{BST}$ = 8.0 V	R$_{DS(ON)}$	–	–	1.0	Ω
Thermal Shutdown (Switcher, V$_{OUT}$ FET)	T$_{SD}$	150	170	190	°C
Thermal Shutdown Hysteresis	T$_{SDHys}$	–	15	–	°C

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions -40°C $\leq$ T$_J$ $\leq$ 125°C unless otherwise noted. Input voltages V$_{IN1}$ = V$_{IN2}$ = 3.3 V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER (BUCK CONVERTER)					
Input Impedance (Note 7)	R$_{IN}$	–	500	–	kΩ
Output Impedance (Note 7)	R$_{OUT}$	–	150	–	Ω
DC Open Loop Gain (Note 7)	A$_{VOL}$	–	80	–	dB
Gain Bandwidth Product (Note 7)	GBW	–	35	–	MHz
Slew Rate (Note 7)	SR	–	200	–	V/μs
Output Voltage Swing – High Level V$_{IN1}$ $\geq$ 3.3 V, I$_{OEA}$ = -1.0 mA (Note 7)	V$_{EA\_OH}$	–	2.0	–	V
Output Voltage Swing – Low Level I$_{OEA}$ = -1.0 mA (Note 7)	V$_{EA\_OL}$	–	0.4	–	V
Slope Compensation Ramp (Note 7)	V$_{SCRamp}$	–	0.6	–	V
OSCILLATOR					
Oscillator Low Level Output Voltage (Pin CLKSYN), CLKSEL Open	V$_{OSC\_OL}$	–	–	0.4	V
Oscillator High Level Output Voltage (Pin CLKSYN), CLKSEL Open	V$_{OSC\_OH}$	3.0	–	–	V
Oscillator Input Voltage Threshold (Pin CLKSYN), CLKSEL Grounded	V$_{OSC\_IH}$	1.2	1.6	2.0	V
Oscillator Frequency Adjusting Reference Voltage (FREQ)	V$_{FREQ}$	–	1.29	–	V
Oscillator Frequency Adjusting Resistor Range	R$_{FREQ}$	100	–	200	kΩ
BOOST REGULATOR					
Boost Regulator Output Voltage I$_{BST}$ = 20 mA, V$_{IN1}$ = V$_{IN2}$ = 2.8 V to 6.0 V	V$_{BST}$	7.5	8.0	8.5	V
Boost Regulator Start-Up Voltage	V$_{IN\_BSU}$	–	1.6	1.8	V
Boost Regulator Peak Current Limit (Power FET Peak Current)	I$_{P\_BD}$	0.75	1.0	1.5	A
Boost Regulator Power FET Valley Current Limit (Low Level)	I$_{L\_BD}$	450	600	800	mA
Boost Power FET R$_{DS(ON)}$ I$_{BD}$ = 1.0 A, T$_A$ = 25°C	R$_{DS(ON)}$	–	150	400	mΩ
Boost Regulator Recommended Output Capacitor	C$_{BST}$	–	10	–	μF
Boost Regulator Recommended Output Capacitor Maximum ESR	ESR$_{CBST}$	–	100	–	mΩ

Notes
7. Design information only. It is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions -40°C $\leq T_J \leq$ 125°C unless otherwise noted. Input voltages $V_{IN1} = V_{IN2} = 3.3$ V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LINEAR REGULATOR (LDO)					
LDO Output Voltage Range $V_{IN1} = V_{IN2}$ = 2.8 V to 6.0 V, I_{LDO} = 10 mA to 1000 mA	V_{LDO}	0.8	–	5.0	V
LDO Feedback Voltage, LFB Pin Connected to LDO Pin $V_{IN1} = V_{IN2}$ = 2.8 V to 6.0 V, I_{LDO} = 10 mA to 1000 mA. Includes Load Regulation Error	V_{LDO}	0.784	0.8	0.816	V
LDO Voltage Margining Step Size	V_{MLDO}	–	1.0	–	%
LDO Line Regulation $V_{IN1} = V_{IN2}$ = 2.8 V to 6.0 V, I_{LDO} = 1000 mA	REG_{LNVLDO}	-1.0	–	1.0	%
LDO Load Regulation I_{LDO} = 10 mA to 1000 mA	REG_{LDVLDO}	-1.0	–	1.0	%
LDO Ripple Rejection, Dropout Voltage V_{DO} = 1.0 V, V_{RIPPLE} = +1.0 V p-p Sinusoidal, f = 300 kHz, I_{LDO} = 500 mA	V_{LDO_RR}	–	40	–	dB
LDO Maximum Dropout Voltage (V_{IN} - V_{LDO}) V_{LDO} = 2.5 V, I_{LDO} = 1000 mA	V_{DO}	–	–	TBD	V
LDO Current Sense Comparator Threshold Voltage (V_{CS} - V_{LDO})	V_{CSTH}	35	45	55	mV
LDO Pin Input Current	I_{LDO}	1.6	2.0	2.4	mA
LDO Feedback Input Current (LFB Pin)	I_{LFB}	-5.0	–	5.0	μA
LDO Drive Output Current (LDRV Pin)	I_{LDRV}	2.0	3.6	5.0	mA
LDO Drive Current Limit (LDRV Pin)	I_{DRLIM}	–	3.6	–	mA
CS Pin Input Leakage Current V_{CS} = 5.0 V	I_{CSLK}	50	–	300	μA
LDO Error Amplifier Input Impedance (LFB Pin)	R_{IN}	–	TBD	–	Ω
LDO Error Amplifier Output Impedance (LCMP Pin)	R_{OUT}	–	TBD	–	Ω
LDO Pull-Down MOSFET Q4 Current Limit T_A = 25°C, V_{BST} = 8.0 V (LDO Pin)	I_{Q4_LIM}	–	-2.0	–	A
LDO Pull-Down MOSFET Q4 $R_{DS(ON)}$ I_D = 1.0 A, T_A = 25°C, V_{BST} = 8.0 V	$R_{DS(ON)}$	–	–	1.0	Ω
LDO Recommended Output Capacitance	C_{LDO}	–	10	–	μF
LDO Recommended Output Capacitor ESR	ESR_{CLDO}	–	TBD	–	mΩ
Thermal Shutdown (LDO Pull-Down FET Q4)	T_{SD}	150	170	190	°C
Thermal Shutdown Hysteresis	T_{SDHys}	–	15	–	°C

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions $-40°C \leq T_J \leq 125°C$ unless otherwise noted. Input voltages $V_{IN1} = V_{IN2} = 3.3$ V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL AND SUPERVISORY CIRCUITS					
Enable (EN1, EN2) Input Voltage Threshold	V_{TH_EN}	1.2	1.6	2.0	V
Enable (EN1, EN2) Input Voltage Threshold Hysteresis	V_{IHYS}	–	0.1	–	V
Enable (EN1, EN2) Pull-Down Resistance	R_{PU}	30	60	120	kΩ
$\overline{RESET}$ Low-Level Output Voltage, $I_{OL} = 5.0$ mA	V_{OL}	–	–	0.4	V
$\overline{RESET}$ Leakage Current, OFF State, Pulled Up to 5.0 V	$I_{LKG-\overline{RST}}$	–	–	10	μA
$\overline{RESET}$ Undervoltage Threshold on V_{OUT} ($\Delta V_{OUT}/V_{OUT}$) (Note 8)	V_{OUTITh}	-10	-7.5	-5.0	%
$\overline{RESET}$ Overvoltage Threshold on V_{OUT} ($\Delta V_{OUT}/V_{OUT}$) (Note 8)	V_{OUTITh}	5.0	7.5	10	%
$\overline{RESET}$ Undervoltage Threshold on V_{LDO} ($\Delta V_{LDO}/V_{LDO}$) (Note 8)	V_{LDOITh}	-10	-7.5	-5.0	%
$\overline{RESET}$ Overvoltage Threshold on V_{LDO} ($\Delta V_{LDO}/V_{LDO}$) (Note 8)	V_{LDOITh}	5.0	7.5	10	%
Reset Timer Voltage Threshold	V_{TH-RT}	TBD	1.2	TBD	V
Reset Timer Source Current	I_{S-RT}	20	–	30	mA
Reset Timer Leakage Current	I_{LKG-RT}	-1.0	–	1.0	μA
Reset Timer Saturation Voltage, Reset Timer Current = 300 μA	V_{SAT-RT}	–	100	TBD	mV
Maximum Value of the Reset Timer Capacitor	C_t	–	–	47	μF
CLKSEL Threshold Voltage	V_{thCLKS}	1.2	1.6	2.0	V
CLKSEL Pull-Up Resistance	$R_{PU-CLKS}$	60	120	240	kΩ
ADDR Threshold Voltage	V_{thADDR}	1.2	1.6	2.0	V
ADDR Pull-Up Resistance	$R_{PU-ADDR}$	60	120	240	kΩ
SDA, SCL Pins I^{2}C Bus (STANDARD)					
Input Threshold Voltage	V_{Ith}	1.3	–	1.7	V
Input Voltage Threshold Hysteresis	V_{IHYS}	–	0.2	–	V
SDA, SCL Input Current, Input Voltage = 0.4 V to 6.0 V	I_I	–	–	10	μA
SDA Low-Level Output Voltage, 3.0 mA Sink Current	V_{OL}	–	–	0.4	V
SCA, SCL Capacitance	C_I	–	–	10	pF

Notes
8. This parameter does not include the tolerance of the external resistor divider.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions -40°C $\leq$ T$_J$ $\leq$ 125°C unless otherwise noted. Input voltages V$_{IN1}$ = V$_{IN2}$ = 3.3 V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTER					
Duty Cycle Range (Normal Operation)	D	0	–	90	%
Switching Node SW Rise Time (Note 9) I$_{LOAD}$ = 1.5 A	t$_{RISE}$	–	TBD	–	ns
Switching Node SW Fall Time (Note 9) I$_{LOAD}$ = 1.5 A	t$_{FALL}$	–	TBD	–	ns
Maximum Deadtime (Note 9)	t$_D$	–	TBD	–	ns
Buck Control Loop Propagation Delay (Note 9) V$_{INV}$ < 0.8 V to V$_{SW}$ > 90% of High Level or V$_{INV}$ > 0.8 V to V$_{SW}$ < 10% of Low Level	t$_{PD}$	–	50	–	ns
Soft Start Duration (Power Sequencing Disabled, EN1 = 1, EN2 = 1)	t$_{SS}$	200	350	800	μs
Fault Condition Timeout	t$_{FAULT}$	–	10	–	ms
Retry Timer Cycle	t$_{Ret}$	–	100	–	ms
OSCILLATOR					
Oscillator Default Frequency (Switching Frequency), FREQ Pin Open	f$_{OSC}$	270	300	330	kHz
Oscillator Frequency Range	f$_{OSC}$	200		400	kHz
Oscillator Frequency Accuracy R$_F$ = 100 kΩ	f$_{OSC}$	360	400	440	kHz
Oscillator Frequency Accuracy R$_F$ = 200 kΩ	f$_{OSC}$	180	200	220	kHz
Oscillator Output Signal Duty Cycle (Square Wave, 180° Out-of-Phase with the Internal Suitable Oscillator)	D$_{OSC}$	–	50	–	%
Synchronization Pulse Minimum Duration	t$_{SYNC}$	300	–	–	ns
BOOST REGULATOR					
Boost Regulator FET Maximum ON Time	t$_{ON}$	–	24	–	μs
Boost Regulator Control Loop Propagation Delay (Note 9)	t$_{BST\_PD}$	–	50	–	ns
Boost Switching Node V$_{BD}$ Rise Time (Note 9) I$_{BST}$ = 20 mA	t$_{B\_RISE}$	–	15	40	ns
Boost Switching Node V$_{BD}$ Fall Time (Note 9) I$_{BST}$ = 20 mA	t$_{B\_FALL}$	–	15	40	ns

Notes
9. Design Information only. Not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions -40°C $\leq T_J \leq$ 125°C unless otherwise noted. Input voltages $V_{IN1} = V_{IN2}$ = 3.3 V using the typical application circuit (see Figure 20) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LINEAR REGULATOR (LDO)					
LDO Output Current Slew Rate	I_{SR}	–	TBD	–	mA/µs
Fault Condition Timeout	t_{FAULT}	–	1.0	–	ms
Retry Timer Cycle	t_{Ret}	–	100	–	ms
SCA, SCL PIN, I²C BUS (STANDARD)					
SCL Clock Frequency	f_{SCL}	0	–	100	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}	4.7	–	–	µs
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.)	t_{HD-STA}	4.0	–	–	µs
Low Period of the SCL Clock	t_{LOW}	4.7	–	–	µs
High Period of the SCL Clock	t_{HIGH}	4.0	–	–	µs
SDA Fall Time from V_{IH_MAX} to V_{IL_MIN}, Bus Capacitance 10 pF to 400 pF, 3.0 mA Sink Current	t_F	–	–	250	ns
Setup Time for a Repeated START Condition	t_{SU-STA}	4.7	–	–	µs
Data Hold Time for I²C bus devices (Note 10), (Note 11)	t_{HD-DAT}	0	–	–	µs
Data Setup Time	t_{SU-DAT}	250	–	–	ns
Setup Time for STOP Condition	t_{SU-STO}	4.0	–	–	µs
Capacitive Load for Each Bus Line	C_B	–	–	400	pF

Notes
10. Design Information only. Not production tested.
11. The device provides an internal hold time of at least 300 ns for the SDA signal (refer to the V_{IH_MIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Timing Diagram
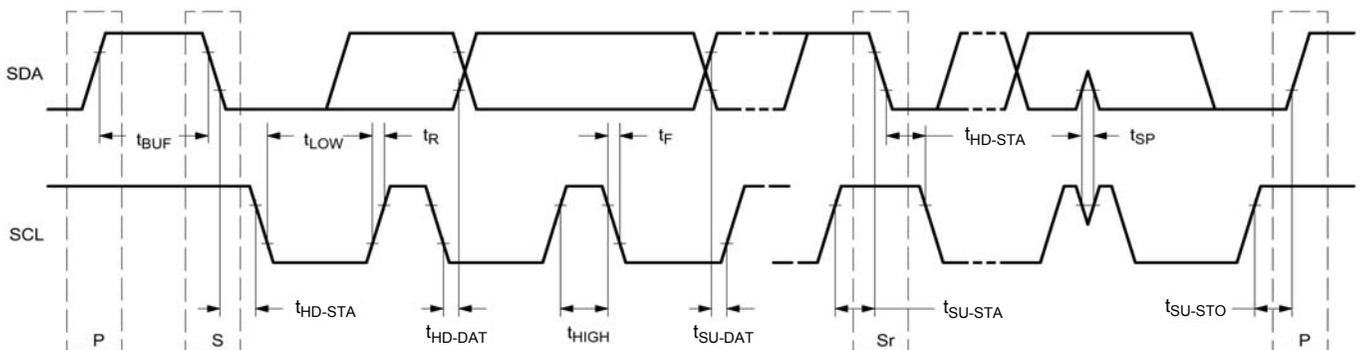
Figure 2. Definition of Time on the I²C Bus

Electrical Performance Curves
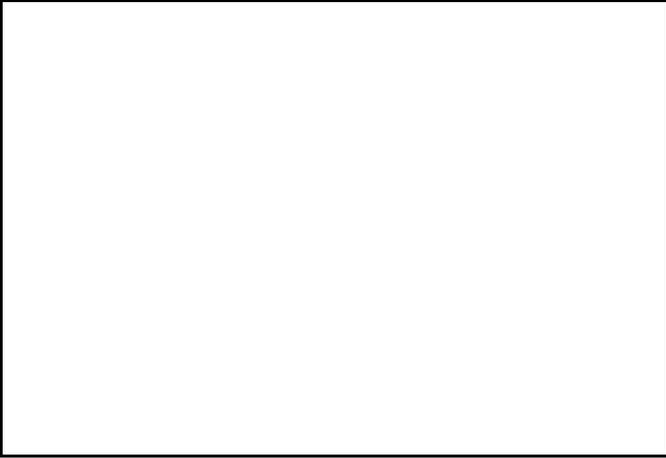
Figure 3. Buck $R_{DS(ON)}$ (Temp)
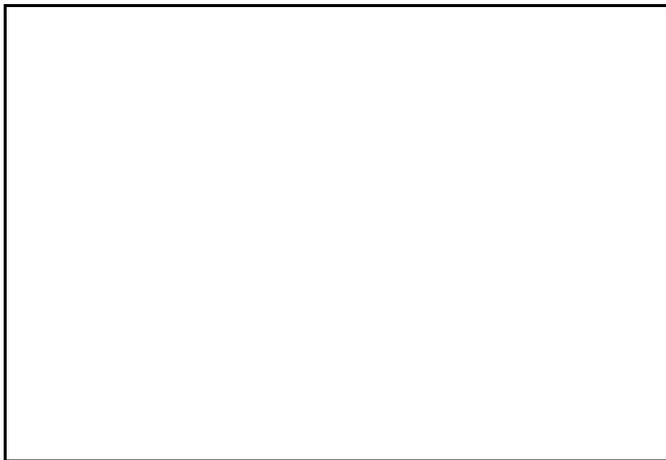
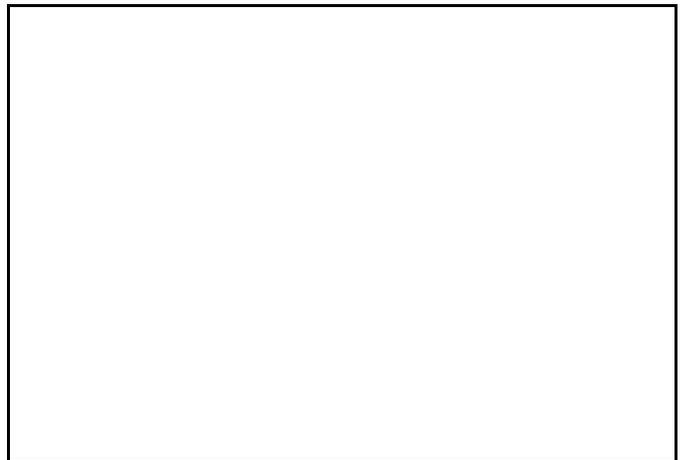Figure 4. F_{OSC} (R_F)

Figure 5. Buck Efficiency

Figure 6. I_{LIM} (Temp)

Figure 7. Vref (Temp)

Figure 8. RT Timer (R_t, C_t)

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33701 power supply integrated circuit provides the means to efficiently supply the Power QUICC and other families of Motorola microprocessors. It incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages.

This device incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system. At the same time, it provides high flexibility of configuration, allowing the maximum optimization of the power supply system.

FUNCTIONAL DESCRIPTION

Switching Regulator

The switching regulator is a high-frequency (300 kHz default, adjustable in the range from 200 kHz to 400 kHz), synchronous buck converter driving integrated high-side and low-side N-channel power MOSFETs. The switching regulator output voltage is adjustable by means of an external resistor divider to provide the required output voltage within plus/minus two percent accuracy, and it is intended to directly power the core of the microprocessor. The buck controller utilizes a Sensorless PWM Current Mode Control topology to achieve excellent line rejection, stabilize the feedback loop, and provide cycle-by-cycle current limiting.

A typical bootstrap technique is used to provide voltage necessary to properly enhance the high-side MOSFET gate. When the regulator is supplied only from low-input voltage (e.g., single +3.3 V supply rail), the bootstrap capacitor is charged from the internal boost regulator output V_{BST} through an external diode. This arrangement allows the 33701 to operate from very low input voltage and also comply with the power sequencing requirements of the supplied microcontroller.

To avoid destruction of the supplied circuits, a current limit with retry capability was implemented in the switching regulator. When an overcurrent condition occurs and the switch current reaches the peak current limit value, the main (high-side) switch is turned off until the inductor current decays to the valley value, which is one-half of the peak current limit. If an overcurrent condition exists for 10 ms, the buck regulator control circuit shuts the switcher OFF and the switcher retry timer starts to time out. When the timer expires after 100 ms, the switcher engages the start-up sequence and runs for 10 ms, repeatedly checking for the overcurrent condition. During the current limited operation (e.g., in case of short circuit on the switching regulator output), the switching regulator operation is not synchronized to the oscillator frequency.

The output voltage V_{OUT} can be adjusted by means of an external resistor divider connected to the feedback control pin INV. The switching regulator output voltage can be adjusted in the range of 0.8 V to 5.0 V, but the V_{OUT} output voltage is always lower than the input voltage to the regulator. Power-up, power-down, and fault management are coordinated with the linear regulator.

Thermal Shutdown

To increase the overall safety of the system designed with the 33701, an internal thermal shutdown function has been incorporated into the switching regulator circuit. The 33701 senses the temperature of the buck regulator main switching FET (high-side FET Q1; see Figure 1), the low-side (synchronous FET Q2), and control circuit. If the temperature of any of the monitored components exceeds the limit of safe operation (thermal shutdown), the switching regulator will be shut down. After the temperature falls below the value given by the thermal shutdown hysteresis window, the switcher will retry to operate again.

The V_{OUT} pull-down FET Q3 has an independent thermal shutdown control. When the Q3 temperature exceeds the thermal shutdown limit, the Q3 will be turned off without affecting the switcher operation.

Soft Start

A switching regulator soft start feature is incorporated in the 33701. The soft start is active each time the IC is enabled, V_{IN} is reapplied, or after a fault retry. Other transient events do not activate the soft start.

Boost Regulator

A boost regulator provides a high voltage necessary to properly drive the buck regulator power MOSFETs, especially during the low input voltage condition. The LDO regulator external N-channel MOSFET gate is also powered from the boost regulator. In order to properly enhance the high-side MOSFETs when only a +3.3 V supply rail powers the integrated circuit, the boost regulator provides an output voltage of 8.0 V nominal value.

The 33701 boost regulator uses a simple hysteretic current control technique, which allows fast power-up and does not require any compensation. When the boost regulator main power switch (low side) is turned on, the current in the inductor starts to ramp up. After the inductor current reaches the upper current limit (nominally set at 1.0 A), the low-side switch is turned off and the current charges the output capacitor through the internal rectifier. When the inductor current falls below the valley current limit value (nominally 600 mA), the low-side switch is turned on again, starting the next switching cycle. After

the boost regulator output capacitor reaches its regulation limit, the low-side switch is turned off until the output voltage falls below the regulation limit again.

Oscillator

A 300 kHz (default) oscillator sets the switching frequency of the buck regulator. The frequency of the oscillator can be adjusted between 200 kHz and 400 kHz by an optional external resistor R_F connected from the FREQ pin of the integrated circuit to ground. See Figure 4 for frequency resistor selection.

The CLKSYN pin can be configured either as an oscillator output when the CLKSEL pin is left open or it can be used as a synchronization input when the CLKSEL pin is grounded. The oscillator output signal is a square wave logic signal with 50 percent duty cycle, 180 degrees out-of-phase with the internal clock signal. This allows opposite phase synchronization of two 3370x devices.

When the CLKSYN pin is used as synchronization input (CLKSEL pin grounded), the external resistor R_F chosen from the chart in Figure 4 should be used to synchronize the internal slope compensation ramp to the external clock. Operation is only recommended between 200 kHz and 400 kHz. The supplied synchronization signal does not need to be 50 percent duty cycle. Minimum pulse width is 300 ns.

Low Dropout Linear Regulator (LDO)

The adjustable low dropout linear regulator (LDO) is capable of supplying a 1.0 A output current. It has a current limit with retry capability. When the voltage measured across the current sense resistor reaches the 45 mV threshold, the control circuit limits the current for 1.0 ms and if the overcurrent condition still exists the linear regulator is turned off. At the same time the overcurrent condition is detected, the Retry Timer starts to time out. When the timer expires after 100 ms, the LDO tries to power up again for 1.0 ms, repeatedly checking for the overcurrent condition. The current limit of the LDO can be set by using the following formula:

$$I_{LIM} = 45 \text{ mV}/R_S$$

Where R_S is the LDO current sense resistor, connected between the CS pin and the LDO pin output (see Figure 20).

When no current sense resistor is used, it is still possible to detect the overcurrent condition by tying the current sense pin CS to the V_{BST} voltage. In this case, the overcurrent condition is sensed by saturation of the linear regulator driver buffer.

The output voltage of the LDO can be adjusted by means of an external resistor divider connected to the feedback control pin LFB. The linear regulator output voltage can be adjusted in the range of 0.8 V to 5.0 V, but the LDO output voltage is always lower than the input voltage to the regulator. Power-up, power-down, and fault management are coordinated with the switching regulator.

Thermal Shutdown

The LDO pull-down FET Q4 has an independent thermal shutdown control. When the Q4 temperature exceeds the

thermal shutdown limit, the Q4 will be turned off without affecting the LDO operation.

Voltage Margining

The 33701 includes a voltage margining feature accessed through the I^{2}C bus. Voltage margining allows for independent adjustment of the Switcher V_{OUT} voltage and the linear output V_{LDO}. Each can be adjusted up and down in 1% steps to a range of ±7%. This feature allows for worst case system validation; i.e., determining the design margin. Margining details are described in the section entitled I^{2}C Bus Operation, beginning on page 19 of this datasheet.

RESET

The $\overline{\text{RESET}}$ pin is an open drain output. The Reset Control circuit supervises both output voltages—the linear regulator output V_{LDO} and the switching regulator output V_{OUT}. When either of these two regulators is out of regulation (high or low), the $\overline{\text{RESET}}$ pin is pulled low. There is a 20 μs delay filter preventing erroneous resets. During power-up sequencing, $\overline{\text{RESET}}$ is held low until the Reset Timer times out.

Reset Timer Power-Up Delay (RT)

The Reset Timer Power-Up Delay (RT) pin is used to set the delay between the time when the LDO and switcher outputs are active and stable and the release of the $\overline{\text{RESET}}$ output. An external resistor and capacitor are used to program the timer. The power-up delay can be obtained by using the following formula:

$$T_D = 10 \text{ ms} + R_t C_t$$

Where R_t is the Reset Timer programming resistor and C_t is the Reset Timer programming capacitor, both connected in parallel from RT to ground.

Note Observe the maximum C_t value and expect reduced accuracy if R_t is less than 10 kΩ.

Watchdog Timer

A watchdog function is available via I^{2}C bus communication. It is possible to select either window watchdog or time-out watchdog operation, as illustrated in Figure 9 on page 15.

Watchdog time-out starts when the watchdog function is activated via I^{2}C bus sending a Watchdog Programming command byte, thus determining watchdog operation (window or time-out) and period duration (refer to Table 1, page 15). If the watchdog is cleared by receiving a new Watchdog Programming command through the I^{2}C bus, the watchdog timer is reset and the new time-out period begins. If the watchdog time expires, the $\overline{\text{RESET}}$ will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms. After a watchdog time-out, the function is no longer active.
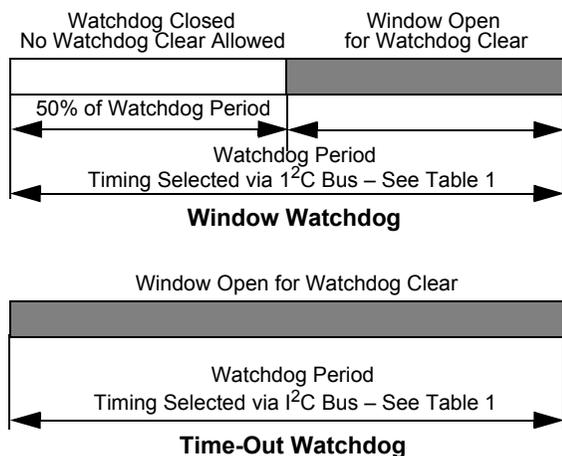
Window Watchdog

Time-Out Watchdog

Figure 9. Watchdog Operation

Table 1. Watchdog Programming Command Byte (as a 2nd Command Byte)

Address			Value					Action
0	1	1	0	0	0	0	0	1st Command
0	1	1	0	0	0	0	0	WD OFF (Note 12)
0	1	1	0	1	0	0	0	WD 1280 ms WinOFF
0	1	1	0	1	0	0	1	WD 320 ms WinOFF
0	1	1	0	1	0	1	0	WD 80 ms WinOFF
0	1	1	0	1	0	1	1	WD 20 ms WinOFF
0	1	1	0	1	1	0	0	WD 1280 ms WinON
0	1	1	0	1	1	0	1	WD 320 ms WinON
0	1	1	0	1	1	1	0	WD 80 ms WinON
0	1	1	0	1	1	1	1	WD 20 ms WinON

Notes

12. The Watchdog feature will be turned ON automatically after receiving any other valid command byte changing watchdog time.

When the Window Watchdog function is selected, the timer cannot be cleared during the Closed Window time, which is 50% of the total watchdog period. When the watchdog is cleared, the timer is reset and starts a new time-out period. If the watchdog is not cleared during the Open Window time, the $\overline{RESET}$ will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms.

EN1 and EN2 Control Pins

These two pins permit positive logic control of the Enable function and selection of the Power Sequencing mode concurrently. Table 2 depicts the EN1 and EN2 function and Power Sequencing mode selection.

Both EN1 and EN2 pins have internal pull-down resistors and both can withstand a short circuit to the supply voltage, 6.0 V.

Table 2. Operating Mode Selection

EN1	EN2	Operating Mode
0	0	Regulators Disabled
0	1	Standard Power Sequencing
1	0	Inverted Power Sequencing
1	1	Regulators Enabled, No Power Sequencing

Power Sequencing Modes

The power sequencing of the two outputs of this power supply IC is in compliance with the Motorola Power QUICC and other 32-bit microprocessor requirements. When the input voltage is applied, the switcher and linear regulator outputs follow the supply rail voltage during power-up and power-down in the limits given by the microcontroller power sequencing specification, illustrated in Figures 10 through 12. There are two possible power sequencing modes, Standard and Inverted, as explained in more detail below. The third mode of operation is Power Sequencing Disabled.
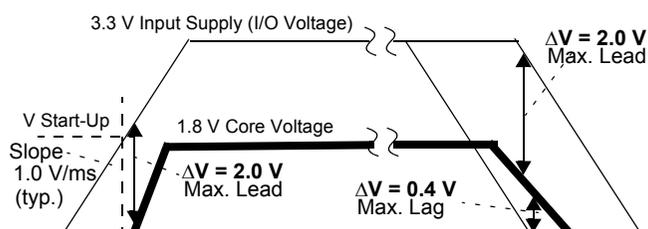
Figure 10. Standard Power Up/Down Sequence in +3.3 V Supply System
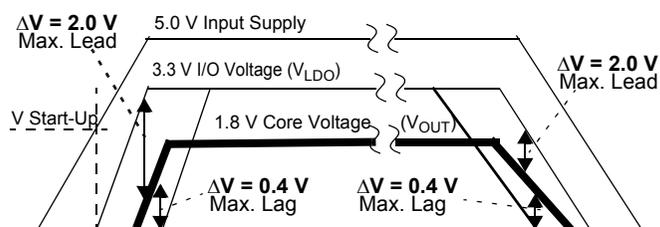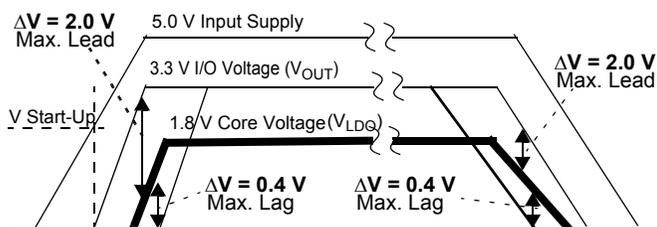

Figure 11. Standard Power Up/Down Sequence in +5.0 V Supply System

Figure 12. Inverted Power Up/Down Sequence in +5.0 V Supply System

Standard Power Sequencing

When the power supply IC operates in the Standard Power Sequencing mode, the switcher output provides the core voltage for the microprocessor. This situation and operating conditions are illustrated in Figure 10 and Figure 11. Table 2, page 15, shows the Power Sequencing mode selection.

Inverted Power Sequencing

When the power supply IC is operating in the Inverted Power Sequencing mode, the linear regulator (LDO) output provides the core voltage for the microprocessor, as illustrated in Figure 12. Table 2 shows the Power Sequencing mode selection.

33701 POWER SEQUENCING

Requirements

1. I/O supply voltage not to exceed core voltage by more than 2.0 V.

2. Core supply voltage not to exceed I/O voltage by more than 0.4 V.

Methods of Control

The 33701 has several methods of monitoring and controlling the regulator output voltages, as described in the paragraphs below. Power sequencing control is also achieved through the intrinsic operation of the regulators. The EN1 and EN2 pins can be used to disable the power sequencing (refer to Table 2, page 15.

Intrinsic Operation

For both the LDO and switcher, whenever the output voltage is below the regulation point, the LDO external Pass FET will be on or the Buck High-Side FET will be on at a duty cycle controlled by the switcher. Because these devices are FETs, current can flow in either direction, balancing the voltages via the common supply pin. The ability to maintain the FETs on will depend on the available gate voltage, and thus the size of the boost regulator storage capacitor.

Standard Power Sequencing Control

Comparators monitor voltage differences between the LDO (LDO pin) and the switcher (V_{OUT} pin) outputs as follows:

1. *LDO > V_{OUT} + 1.8 V, turn off LDO.* The LDO can be forced off. This occurs whenever the LDO output voltage exceeds the switcher output voltage by more than 1.8 V.

2. *LDO > V_{OUT} + 1.9 V, shunt LDO to ground.* If turning off the LDO is insufficient and the LDO output voltage exceeds the switcher output voltage by more than 1.9 V, a 1.0 Ω shunt FET is turned on that discharges the LDO load capacitor to ground. The shunt FET is used for switcher output shorts to ground and for power down in case of $V_{IN1} \neq V_{IN2}$ with the switcher output falling faster than the LDO.

3. *LDO < V_{OUT} + 1.7 V, cancel (1) and (2) above, re-enable LDO.* Normal operation resumes when the LDO output voltage is less than 1.7 V above the switcher output voltage.

4. *LDO < V_{OUT} - 0.2 V, turn off switcher.* The switcher can be forced off. This occurs whenever the LDO is less than V_{OUT} - 0.2 V.

5. *LDO < V_{OUT} - 0.3 V, turn on Sync (LS) FET and 1.0 Ω V_{OUT} sink FET.* The Buck High-Side FET is forced off and the Sync FET is forced on. This occurs when the switcher output voltage exceeds the LDO output by more than 300 mV.

6. *LDO > V_{OUT}, reset (4) and (5) above.* Normal operation resumes when LDO > V_{OUT}.

Inverted Power Sequencing Control

Comparators monitor voltage differences between the switcher (V_{OUT} pin) and LDO (LDO pin) outputs as follows:

1. *V_{OUT} > LDO + 1.8 V, turn off V_{OUT}.* The switcher V_{OUT} can be forced off. This occurs whenever the V_{OUT} output voltage exceeds the LDO output voltage by more than 1.8 V.

2. *V_{OUT} > LDO + 1.9 V, shunt V_{OUT} to ground.* If turning off the switcher V_{OUT} is insufficient and the V_{OUT} output voltage exceeds the LDO output voltage by more than 1.9 V, a 1.0 Ω shunt FET is turned on that discharges the V_{OUT} load capacitor to ground. The shunt FET is used for LDO output shorts to ground and for power-down in case of $V_{IN1} \neq V_{IN2}$ with LDO output falling faster than the V_{OUT}.

3. *V_{OUT} < LDO + 1.7 V, cancel (1) and (2) above, re-enable V_{OUT}.* Normal operation resumes when the V_{OUT} output voltage is less than 1.7 V above the LDO output voltage.

4. *V_{OUT} < LDO - 0.2 V, turn off LDO.* The LDO can be forced off. This occurs whenever the V_{OUT} is less than V_{LDO} - 0.2 V.

5. *V_{OUT} < LDO - 0.3 V, turn on the 1.0 Ω LDO sink FET.* This occurs when the LDO output voltage exceeds the V_{OUT} output by more than 300 mV.

6. *V_{OUT} > LDO, reset (4) and (5) above.* Normal operation resumes when V_{OUT} > LDO.

Standard Operating Mode

1. Single 3.3 V Supply, $V_{IN} = V_{IN1} = V_{IN2} = 3.3$ V

The 3.3 V supplies the microprocessor I/O voltage, the switcher supplies core voltage (e.g., 1.8 V nominal), and the LDO operates independently (see Figure 10, page 15). Power sequencing depends only on the normal switcher intrinsic operation to control the Buck High-Side FET.

Power Up

When V_{IN} is rising, initially V_{OUT} will be below the regulation point and the Buck High-Side FET will be on. In order not to exceed the 2.0 V differential requirement between the I/O (V_{IN}) and the core (V_{OUT}), the switcher must start up at 2.0 V or less and be able to maintain the 2.0 V or less differential. The maximum slew rate for V_{IN} is 1.0 V/ms.

Power Down

When V_{IN} is falling, V_{OUT} will be below the regulation point; therefore the Buck High-Side FET will be on. In the case where V_{OUT} is falling faster than V_{IN}, the Buck High-Side FET will attempt to maintain V_{OUT}. In the case where V_{IN} is falling faster

than V_{OUT}, the Buck High-Side FET is also on, and the V_{OUT} load capacitor will be discharged through the Buck High-Side FET to V_{IN}. Thus, provided V_{IN} does not fall too fast, the core voltage (V_{OUT}) will not exceed the I/O voltage (V_{IN}) by more than a maximum of 0.4 V.

Shorted Load

1. *V_{OUT} shorted to ground.* This will cause the I/O voltage to exceed the core voltage by more than 2.0 V. No load protection.

2. *V_{IN} shorted to ground.* Until the switcher load capacitance is discharged, the core voltage will exceed the I/O voltage by more than 0.4 V. By the intrinsic operation of the switcher, the load capacitor will be discharged rapidly through the Buck High-Side FET to V_{IN}.

3. *V_{OUT} shorted to supply.* No load protection. 33701 protected by current limit and thermal limit.

2. Single 5.0 V Supply, $V_{IN1} = V_{IN2}$, or Dual Supply $V_{IN1} \neq V_{IN2}$

The LDO supplies the microprocessor I/O voltage. The switcher supplies the core (e.g., 1.8 V nominal) (see Figure 11, page 15).

Power Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the V_{IN1} and V_{IN2} supplies. There are 2 cases:

1. *LDO rises faster than V_{OUT}.* The LDO uses control methods (1) and (2) described in the Methods of Control section, page 16.

2. *V_{OUT} rises faster than LDO.* The switcher uses control methods (4) and (5) described in the Methods of Control section, page 16.

Power Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the V_{IN1} and V_{IN2} supplies. There are 2 cases:

1. *V_{OUT} falls faster than LDO.* The LDO uses control methods (1) and (2) described in the Methods of Control section, page 16.

In the case $V_{IN1} = V_{IN2}$, the intrinsic operation will turn on both the Buck High-Side FET and the LDO external Pass FET, and will discharge the LDO load capacitor into the V_{IN} supply.

2. *LDO falls faster than V_{OUT}.* The switcher uses control methods (4) and (5) described in the Methods of Control section, page 16.

Shorted Load

1. *V_{OUT} shorted to ground.* The LDO uses method (1) and (2) described in the Methods of Control section, page 16.

2. *LDO shorted to ground.* The switcher uses control methods (4) and (5) described in the Methods of Control section, page 16.

3. *V_{IN1} shorted to ground.* This is equivalent to the LDO output shorted to ground.

4. *V_{IN2} shorted to ground.* This is equivalent to the switcher output shorted to ground.

5. *V_{OUT} shorted to supply.* No load protection. 33701 protected by current limit and thermal limit.

6. *LDO shorted to supply.* No load protection. 33701 protected by current limit and thermal limit.

Inverted Operating Mode

1. Single 3.3 V Supply, $V_{IN} = V_{IN1} = V_{IN2} = 3.3$ V

The 3.3 V supplies the microprocessor I/O voltage, the LDO supplies core voltage (e.g., 1.8 V nominal), and the switcher V_{OUT} operates independently. Power sequencing depends only on the normal LDO intrinsic operation to control the Pass FET.

Power Up

When V_{IN} is rising, initially LDO will be below the regulation point and the Pass FET will be on. In order not to exceed the 2.0 V differential requirement between the I/O (V_{IN}) and the core (LDO), the LDO must start up at 2.0 V or less and be able to maintain the 2.0 V or less differential. The maximum slew rate for V_{IN} is 1.0 V/ms.

Power Down

When V_{IN} is falling, LDO will be below the regulation point; therefore the Pass FET will be on. In the case where LDO is falling faster than V_{IN}, the Pass FET will attempt to maintain LDO. In the case where V_{IN} is falling faster than LDO, the Pass FET is also on, and the LDO load capacitor will be discharged through the Pass FET to V_{IN}. Thus, provided V_{IN} does not fall too fast, the core voltage (LDO) will not exceed the I/O voltage (V_{IN}) by more than maximum of 0.4 V.

Shorted Load

1. *LDO shorted to ground.* This will cause the I/O voltage to exceed the core voltage by more than 2.0 V. No load protection.

2. *V_{IN} shorted to ground.* Until the LDO load capacitance is discharged, the core voltage will exceed the I/O voltage by more than 0.4 V. By the intrinsic operation of the LDO, the load capacitor will be discharged rapidly through the Pass FET to V_{IN}.

3. *LDO shorted to supply.* No load protection.

2. Single 5.0 V Supply, $V_{IN1} = V_{IN2}$, or Dual Supply $V_{IN1} \neq V_{IN2}$

The switcher V_{OUT} supplies the microprocessor I/O voltage. The LDO supplies the core (e.g., 1.8 V nominal) (see Figure 12, page 16).

Power Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the V_{IN1} and V_{IN2} supplies. There are 2 cases:

1. *V_{OUT} rises faster than LDO.* The switcher V_{OUT} uses control methods (4) and (5) described in the Methods of Control section, page 17.

2. *LDO rises faster than V_{OUT}.* The LDO uses control methods (1) and (2) described in the Methods of Control section, page 17.

Power Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the V_{IN1} and V_{IN2} supplies. There are 2 cases:

1. *LDO falls faster than V_{OUT}.* The V_{OUT} uses control methods (4) and (5) described in the Methods of Control section, page 17.

In the case $V_{IN1} = V_{IN2}$ the intrinsic operation will turn both the Buck High-Side FET and the LDO external Pass FET, and will discharge the V_{OUT} load capacitor into the V_{IN} supply.

2. *V_{OUT} falls faster than LDO.* The LDO uses control methods (1) and (2) described in the Methods of Control section, page 17.

Shorted Load

1. *LDO shorted to ground.* The V_{OUT} uses methods (4) and (5) described in the Methods of Control section, page 17.

2. *V_{OUT} shorted to ground.* The LDO uses control methods (1) and (2) described in the Methods of Control section.

3. *V_{IN1} shorted to ground.* This is equivalent to the LDO output shorted to ground.

4. *V_{IN2} shorted to ground.* This is equivalent to the switcher V_{OUT} output shorted to ground.

5. *LDO shorted to supply.* No load protection.

6. *V_{OUT} shorted to supply.* No load protection. 33701 protected by current limit and thermal limit.

I²C BUS OPERATION

Introduction

The 33701 device is compatible with the I²C interface standard. SDA and SCL pins are the Serial Data and Serial Clock pins of the I²C bus.

I²C Command and Data Formats

Communication Start

Communication starts with a START condition, followed by the slave device unique address. Figure 13 illustrates the data transfer beginning an I²C communication for a 7-bit slave address.
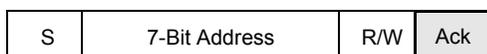
S	7-Bit Address	R/W	Ack

Figure 13. Communication Using 7-Bit Address

Slave Address Definition

33701 has the two LSB's address bits defined by the state of the CLKSEL pin and the ADDR pin.

Note The state of the CLKSEL pin also defines the configuration of the oscillator synchronization CLKSYN pin.

This feature allows up to four 33701 ICs to communicate in the same I²C bus, all of them sharing the same high-order address bits. A different combination of bits A1 and A0 is assigned to each individual part to assure its unique address. Figure 14 illustrates the flexible addressing feature for a 7-bit address. Table 3 provides the definition of the selectable portion of the device address.

Bits	6	5	4	3	2	1	0
	1	1	1	0	1	A1	A0

Fixed Address   Selectable Address
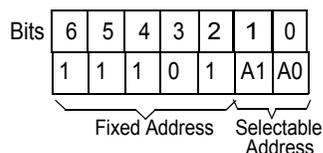
Figure 14. Address Bit Definition for 7-Bit Address

Table 3. Definition of Selectable Portion of Device Address

CLKSEL Pin	ADDR Pin	A1	A0
Low	Low	0	0
Low	Open	0	1
Open	Low	1	0
Open	Open	1	1

Writing Data Into the Slave Device

After the address acknowledgment by the slave, DATA can be written into the slave registers. The R/W bit must be set to 0 so DATA will be read. Figure 15 shows the data write sequence. Actions performed by the slave device are grayed.

S	7-Bit Address	0	Ack	DATA	Ack
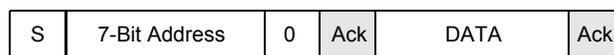
Figure 15. Data Transfer for Write Operations

Data Definition

For the sake of 33701 acting as a slave device, the master writes a Command Byte and writes one Data Byte. The Command Byte identifies the kind of operation required by the master and has two fields, as illustrated in Figure 16:

1. Address field
2. Value field

The address field is selected from the list in Table 4.

Bits	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Address Field   Value Field
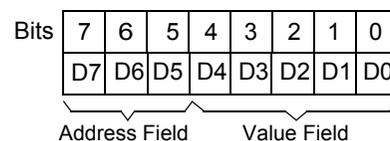
Figure 16. Command Byte

Table 4. Address Field Definitions

Code	Operation	Write
001	Voltage Margining	W
010	Not Used	–
011	Watchdog	W

Refer to Table 5, page 20, which summarizes the value field definitions for the entire set of operation options.

Table 5. Command Byte Definitions

Operation	Address			Value					Action
Voltage Margining	0	0	1	0	0	0	0	0	1st Command
(As a 2nd Command Byte)	0	0	1	x	0	0	0	0	Output Normal
	0	0	1	x	0	0	0	1	+ 1%
	0	0	1	x	0	0	1	0	+ 2%
	0	0	1	x	0	0	1	1	+ 3%
	0	0	1	x	0	1	0	0	+ 4%
LDO Output: x = 0	0	0	1	x	0	1	0	1	+ 5%
Switcher Output x = 1	0	0	1	x	0	1	1	0	+ 6%
	0	0	1	x	0	1	1	1	+ 7%
	0	0	1	x	1	0	0	1	- 1%
	0	0	1	x	1	0	1	0	- 2%
	0	0	1	x	1	0	1	1	- 3%
	0	0	1	x	1	1	0	0	- 4%
	0	0	1	x	1	1	0	1	- 5%
	0	0	1	x	1	1	1	0	- 6%
	0	0	1	x	1	1	1	1	- 7%
Watchdog Programming	0	1	1	0	0	0	0	0	1st Command
(As a 2nd Command Byte)	0	1	1	0	0	0	0	0	WD OFF (Note 13)
	0	1	1	0	1	0	0	0	WD 1280 ms WinOFF
	0	1	1	0	1	0	0	1	WD 320 ms WinOFF
	0	1	1	0	1	0	1	0	WD 80 ms WinOFF
	0	1	1	0	1	0	1	1	WD 20 ms WinOFF
	0	1	1	0	1	1	0	0	WD 1280 ms WinON
	0	1	1	0	1	1	0	1	WD 320 ms WinON
	0	1	1	0	1	1	1	0	WD 80 ms WinON
	0	1	1	0	1	1	1	1	WD 20 ms WinON

Notes
13. The Watchdog feature will be turned ON automatically after receiving any other valid command byte changing watchdog time.

Security in Writing Commands

All writing operations are critical and must not be inadvertently latched after a false command. To improve the security level, a so-called *first command* is defined to initiate each write communications.

A first command has the Command Byte address field equal to the related operation one, followed by a null value field (all zeros). Table 6 summarizes first command definitions. The master sends the first command before the Command Byte for the intended operation.

Table 6. First Command Definitions

First Command	Operation
001 00000	Voltage Margining
011 00000	Watchdog Programming

Voltage Margining Operation

After starting the communication in Writing mode, the master sends the first command followed by the specific Command Byte to set the required voltage margining for either the LDO or the switcher (see Figure 17). To achieve a simultaneous set for both LDO and switcher, two specific commands must be issued in sequence after the first command, one for each supply.

First Byte for Voltage Margining   Command Byte
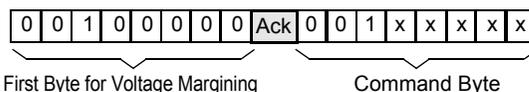
Figure 17. Voltage Margining Programming (One Supply Only)

Note x bits are defined in Table 5.

Watchdog Programming Operation

For watchdog operation control, the master periodically sends a watchdog first command followed by a command byte selecting, or confirming, the watchdog period according to the options listed in Table 5. Also see Figure 18.

The internal watchdog timer will be cleared each time a watchdog command is written into the device, provided it arrives during the window open time. The Command 01100000 sent twice will shut the time OFF, and the watchdog function will be disabled. Any other valid watchdog command turns on the timer again.

First Byte for Watchdog Programming   Command Byte
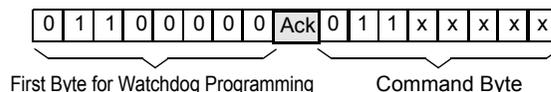
Figure 18. Watchdog Timer Programming

Note x bits are defined in Table 5.

Communication Stop

Only the master can terminate the data transfer by issuing a STOP condition. The slave waits for this condition to resume its initial state waiting for the next START condition (see Figure 19).
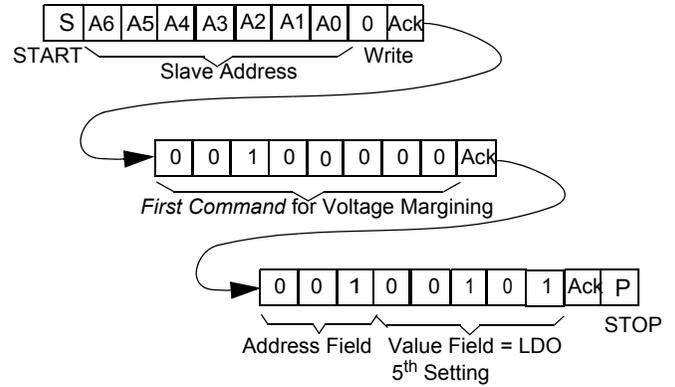
Data Transfer Example

The master device controlling the I^2C bus will always start addressing a 33701 slave IC in writing mode (R/W = 0) in order to be able to write a Command Byte just after the address acknowledge. I^2C bus protocol defines this circumstance as a master-transmitter and slave-receiver configuration.

Eventually this Command Byte can again define a Write operation (e.g., Voltage Margining, see Figure 19), and the master will keep the data transfer direction.

Figure 19 illustrates a communication beginning with the slave address, the *first command* for voltage margining, and a third byte containing the address field *001* and the value field *00101* corresponding with the LDO fifth setting (LDO output voltage = +5% above its nominal value). If a simultaneous

setting for switcher is needed, a fourth byte should be included before the STOP condition (P); for instance, *001 10010* to set switcher in its second setting (switcher output voltage = +2% above its nominal value).

Figure 19. Complete Data Transfer Example

APPLICATION INFORMATION

Figure 20. Simplified Block Diagram and Typical Application

PACKAGE DIMENSIONS

DWB SUFFIX
32-LEAD SOIC WIDE BODY
PLASTIC PACKAGE
CASE 1324-02
ISSUE A
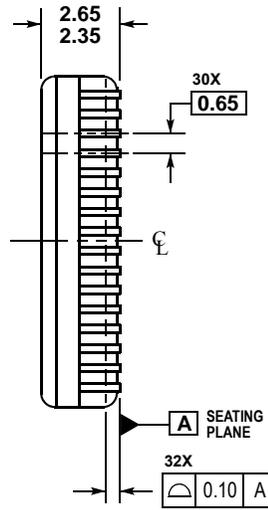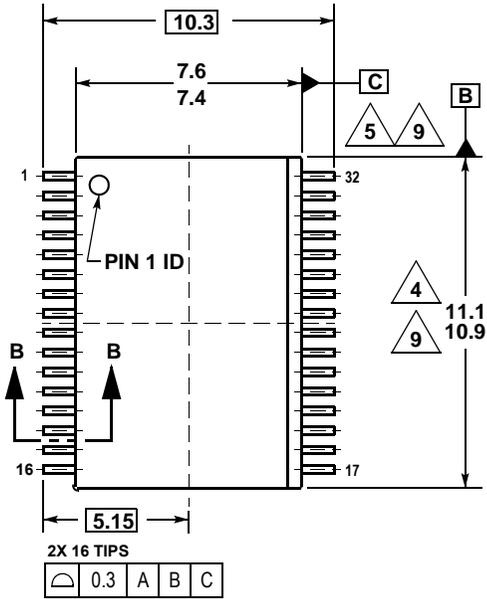
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

PIN 1 ID

B B

2X 16 TIPS

⌐ 0.3 A B C

A A

SEATING PLANE

A

32X

⌐ 0.10 A

30X

0.65

10.3
7.6
7.4
11.1
10.9
5.15
2.65
2.35

(0.29) — BASE METAL

0.25
0.19
(0.203)
0.38
0.22 — PLATING

⊕ 0.13 Ⓜ C A Ⓜ B

SECTION A-A
ROTATED 90° CLOCKWISE

R0.08 MIN
0.25 GAUGE PLANE
0° MIN
0.29
0.13
8°
0°
0.9
0.5

SECTION B-B

HOW TO REACH US:

MOTOROLA