MC33GD3100

Advanced IGBT Gate Driver

Rev. 3.1 — 26 October 2018 Short data sheet: advance information

1 General description

The MC33GD3100 is an advanced single channel gate driver for IGBTs. Integrated Galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage and rail-to-rail gate voltage control.

Current and temperature sense minimizes IGBT stress during faults. Accurate and configurable under voltage lockout (UVLO) provides protection while ensuring sufficient gate drive voltage headroom.

The MC33GD3100 autonomously manages severe faults and reports faults and status via INTB pin and an SPI interface. It is capable of directly driving gates of most IGBTs. Self test, control and protection functions are included for design of high reliability systems (ASIL C/D). It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

2 Simplified application diagram

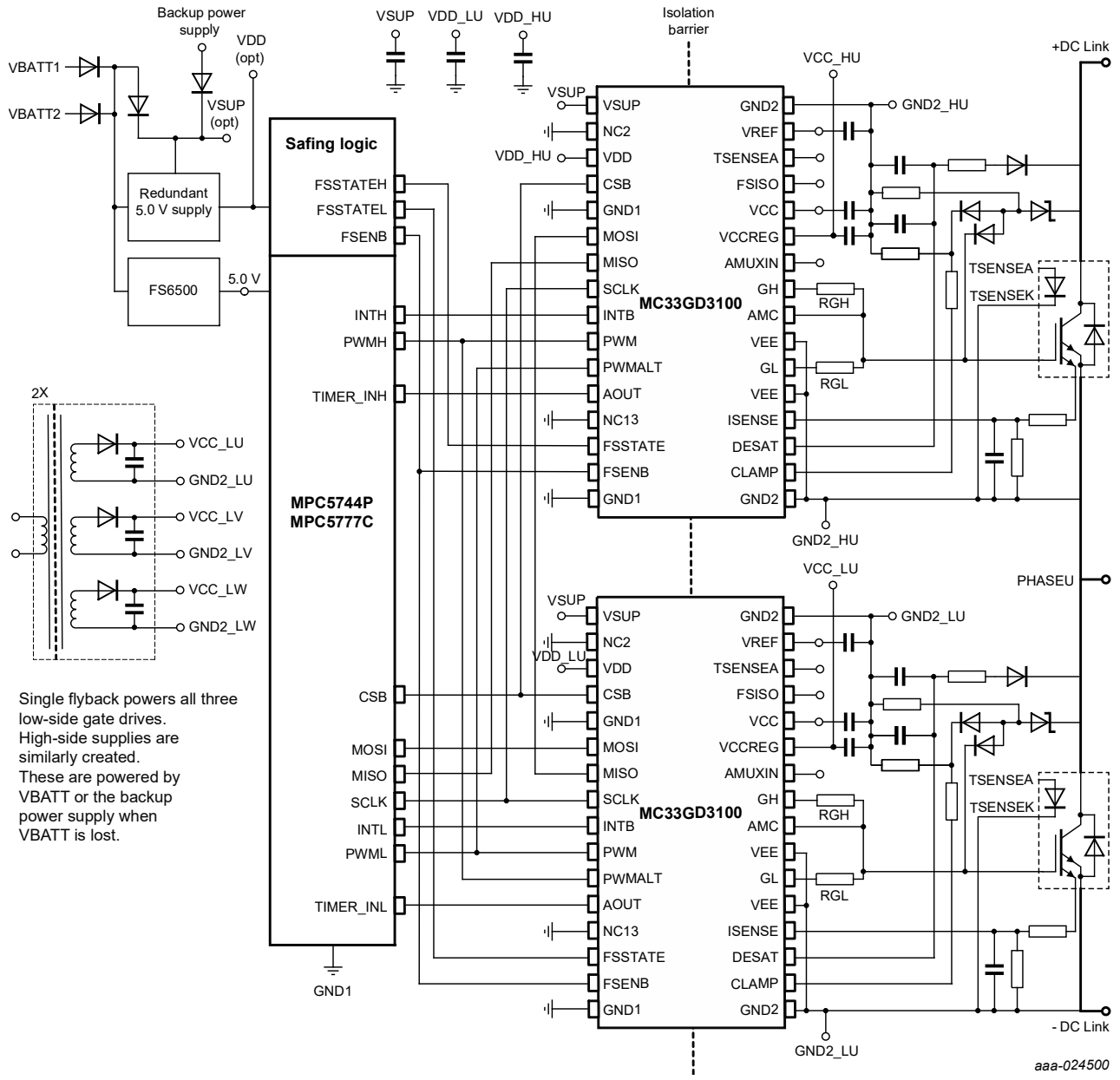


Figure 1. Simplified application diagram

3 Features and benefits

This section summarizes the key features:

- Compatible with current sense and temp sense IGBTs
- Fast short-circuit protection for IGBTs with current sense feedback
- Compliant with ASIL D ISO 26262 functional safety requirements
- SPI interface for safety monitoring, programmability and flexibility
- Integrated Galvanic signal isolation
- Integrated gate drive power stage capable of 10 A peak source and sink
- Interrupt pin for fast response to faults
- Compatible with negative gate supply
- Compatible with 200 V to 1700 V IGBTs, power range > 125 kW
- AEC-Q100 grade 1 qualified

4 Ordering information

Table 1. Orderable part variations

Part number [1]	VDD	Temperature (T_J)	Package
PC33GD3100EK	5.0 V	−40 °C to 150 °C	32-pin wide body SOIC, 0.65 mm pitch
PC33GD3100A3EK	3.3 V		

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Internal block diagram

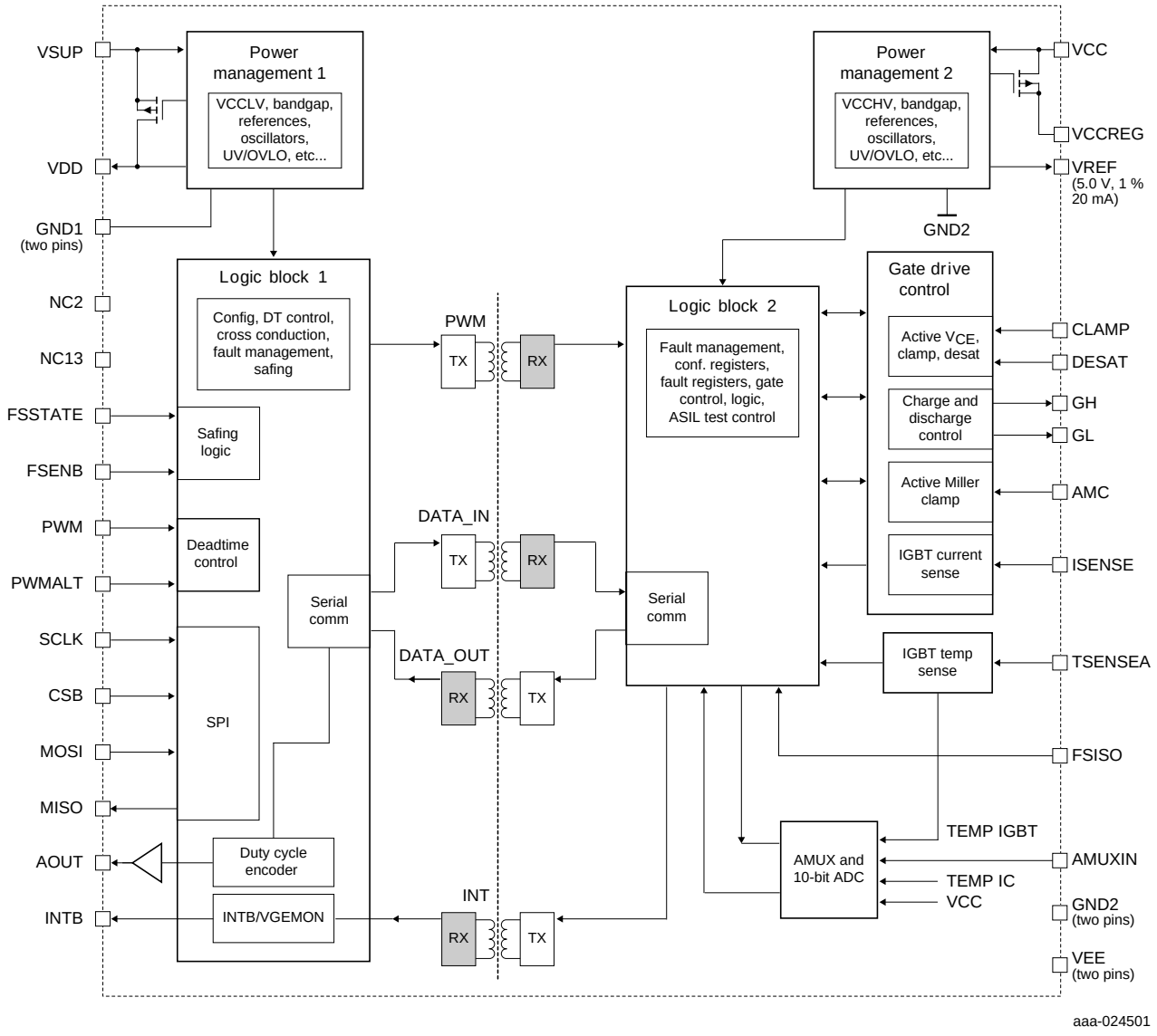


Figure 2. Internal block diagram

6 Pinning information

6.1 Pinning

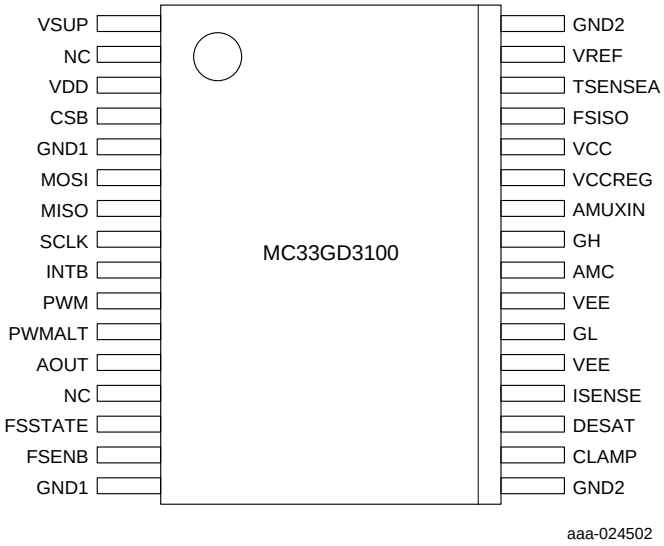


Figure 3. Pinout diagram

6.2 Pin description

Table 2. Pin definitions

Pin number	Pin name	Pin type		Definition	Comments
Pins 1 to 16 (low-voltage, non-isolated pins)					
1	VSUP	power	input	Externally supplied voltage source supply; primary supply for non-isolated circuits	Typically supplied by vehicle battery
2, 13	NC2, NC13	—	—	No connection	NC2 and NC13 must be connected to GND1
3	VDD	power	input	Internally generated supply to power AOUT, MISO and INTB	Not to be used to power other circuitry. External capacitor should be placed at this pin. May be supplied externally (MC33GD3100EK only).
4	CSB	digital	input	SPI chip select	Chip select input. Active low. CSB frames SPI commands and enables SPI port.
5, 16	GND1	ground	ground	Ground for the non-isolated circuitry: input logic including SPI, PWM, PWMALT, FSENB, FSSTATE, AMUX, VDD, INTB	Isolated from all circuitry referenced to GND2
6	MOSI	digital	input	SPI master out slave in pin	Input data for SPI port. MC33GD3100 latches MOSI on rising edge of SCLK, MSB first

Pin number	Pin name	Pin type		Definition	Comments
7	MISO	digital	output	SPI master in slave out pin	Output data for SPI port, MC33GD3100 outputs MISO on falling edge of SCLK.
8	SCLK	digital	input	SPI clock	Clock for SPI
9	INTB	digital	output	Interrupt/Fault status output	Interrupt pin output, reports faults with active pulldown. Pin is left open if unused.
10	PWM	digital	input	PWM input for the IGBT gate	Active high input logic signal turns on the IGBT
11	PWMALT	digital	input	PWM input for opposing IGBT gate	Active high input logic signal turns off IGBT gate (opposing IGBT is turned on). Connected to GND1 if unused.
12	AOUT	analog	output	Duty cycle encoded analog signals for temperature or voltage	Desired analog signal is selected by SPI. Pin is left open if unused.
14	FSSTATE	digital	input	Fail-safe state specifies the desired state of the output during a fail-safe condition	Allows fail-safe logic control. Connected to GND1 if unused.
15	FSENB	digital	input	Enables the fail-safe state	Allows fail-safe logic control. Connected to VDD if unused.
Pins 17 to 32 (high-voltage, isolated pins)					
17, 32	GND2	ground 2	ground 2	Ground for the isolated (high-voltage) circuitry	Must be connected to IGBT's emitter
18	CLAMP	analog	input	V_{CE} sense terminal for actively clamping the collector voltage at turn-off	Connected to VEE if unused
19	DESAT	analog	output	V_{CE} desaturation monitoring pin	Connected to GND2 if unused
20	ISENSE	analog	input	Current sense feedback pin	Receives current sense feedback from the IGBT's current sense. Connected to GND2 if unused.
21, 23	VEE	power	input	Negative voltage supply for gate of the IGBT	Typically −5.0 to −8.0 V, referenced to GND2. Connect to GND2 if a negative supply is not used.
22	GL	analog	output	Primary discharging pin for IGBT gate	Pulldown transistor at this pin discharges the IGBT gate
24	AMC	analog	input	Pin connected directly to IGBT gate for gate sensing and Active Miller Clamping	Used for diagnostics and Active Miller Clamping
25	GH	analog	output	Sole charging pin for IGBT gate	Pullup transistor at this pin charges the IGBT gate
26	AMUXIN	analog	input	Analog MUX input	Connected to GND2 if unused

Pin number	Pin name	Pin type		Definition	Comments
27	VCCREG	power	in/out	Regulated positive supply for the IGBT gate. Requires capacitance.	15 V supply derived from VCC. Connected to VCC if regulator unused.
28	VCC	power	input	Positive voltage supply for isolated circuitry and gate of the IGBT	Typically 15 to 18 V, referenced to GND2
29	FSISO	digital	input	Tri-states gate drive transistors to allow external control of IGBT gate	Used for HV domain management of fail-safe state. Connected to GND2 if unused.
30	TSENSEA	analog	input	Anode of temp sense diode of IGBT	Sources current and reads voltage of temp sense diode of one IGBT die. Connect to VREF if unused.
31	VREF	analog	output	5.0 V reference for isolated analog circuitry	Capable of sourcing up to 20 mA

7 Absolute maximum ratings

All voltages are referenced to GND1 or GND2. Currents are positive into and negative out of the specified pins. Exceeding these ratings may cause malfunction or permanent device damage.

Table 3. Absolute maximum ratings

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). Currents are positive into and negative out of the specified pins.

Symbol	Description (Rating)		Min.	Max.	Unit
POWER SUPPLIES AND CURRENT REFERENCES					
V_{VSUP}	Low voltage domain supply voltage	[1]	−0.3	40	V
V_{VDD3p3}	Low voltage domain logic supply voltage, 3.3 V version	[1]	−0.3	7.0	V
V_{VDD5}	Low voltage domain logic supply voltage, 5.0 V version	[1]	−0.3	7.0	V
V_{VCC}	High voltage domain positive supply voltage	[2]	−0.3	25	V
V_{VEE}	High voltage domain negative supply voltage	[2]	−12	0.3	V
$V_{VCC-VVEE}$	High voltage domain positive/negative supply		−0.3	37	V
V_{VCCREG}	High voltage domain post regulated supply voltage	[2]	−0.3	25	V
I_{VCCREG}	VCCREG output current		—	100	mA
V_{VREF}	VREF voltage	[2]	−0.3	7.0	V
I_{VREF}	VREF output current		—	20	mA
LOGIC PINS					
V_{IN}	Logic input pin voltage (FSSTATE, FSENB, PWM, PWMALT, SCLK, CSB, MOSI)	[1]	−0.3	18	V
V_{OUT}	Logic output pin voltage (MISO, INTB, AOUT)	[1]	−0.3	V_{VDD} + 0.3 V	V
V_{FSISO}	Logic input pin voltage (FSISO)	[2]	−0.3	12	V
GATE DRIVE OUTPUT STAGE					

Symbol	Description (Rating)		Min.	Max.	Unit
V_{GH}	GH voltage	[2]	VEE − 0.3	V_{VCCREG} + 0.3 V	V
V_{GL}	GL voltage	[2]	VEE − 0.3	V_{VCCREG} + 0.3 V	V
V_{AMC}	AMC voltage	[2]	VEE − 0.3	V_{VCCREG} + 0.3 V	V
$I_{SOURCEMAX}$	GH max. source Current	[3]	—	10	A
$I_{SINKMAX}$	GL, AMC max. sink current	[3]	—	−10	A
V_{CLAMP}	CLAMP voltage	[2]	VEE − 0.3	V_{VCCREG} + 0.3 V	V
V_{DESAT}	DESAT voltage	[2]	−0.3	V_{VCCREG} + 0.3 V	V
TEMPERATURE SENSE PIN					
$V_{TSENSEA}$	TSENSEA voltage	[2]	−0.3	7.0	V
INTB PIN					
I_{INTB}	Open drain DC output current	[4]	—	20	mA
ISENSE SENSE PIN					
V_{ISENSE}	ISENSE voltage	[2]	−2.0	V_{VCCREG} + 0.3 V	V
AMUXIN PIN					
V_{AMUXIN}	AMUXIN voltage	[2]	−0.3	7.0	V
ESD RATINGS					
V_{ESDHBM}	ESD voltage (HBM) All pins	[5]	 −2.0	 2.0	kV
V_{ESDCDM}	ESD voltage (CDM) Corner pins Other pins	[6]	 −750 −500	 750 500	V
$V_{ESDModule}$	ESD voltage (module level) VSUP, GND1, GND2 pins	[7]	 −8.0	 8.0	kV
IMMUNITY					
dV_{ISO}/dt	Common mode transient immunity	[8]	—	50	V/ns
PWM FREQUENCY					
f_{PWMMAX}	Maximum switching frequency		0	40	kHz

[1] Ref = GND1
[2] Ref = GND2
[3] P.W. = 2 µs, 1.0 % DC max.
[4] VINTB < 0.8 V
[5] **Human Body Model (HBM) at device level**
ANSI/ESDA/JEDEC JS-001: 2010 Model HBM (human body model)
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
Test points: pin to GND1 and pin to GND2
[6] **Charged Device Model (CDM)**
ANSI/ESD S5.3.1-2009
ESD Association Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
[7] **Module Level ESD Tests**
ISO 10605:2008/Cor. 1:2010(E)
Road vehicles – Test methods for electrical disturbances from electrostatic discharge
[8] Pulse width = 10 ns

8 General functional description

8.1 Introduction

The MC33GD3100 is an advanced single channel gate driver for N-channel power IGBTs. Integrated galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage and rail-to-rail gate voltage control. Collector current, collector-emitter voltage, and IGBT temperature sense minimize IGBT stress during faults.

The MC33GD3100 autonomously manages severe faults and reports faults and status via INTB pin and an SPI interface. It is capable of directly driving gates of most IGBTs. Self test, control and protection functions are included for design of high reliability systems (ASIL/SIL).

8.2 Power supply options

The MC33GD3100 is available in two options: VDD of 3.3 V or 5.0 V. The two options are desired to allow interfacing to MCUs with 3.3 or 5.0 V I/O.

VDD regulator output is set to 5.0 V or 3.3 V based on fuse programming at NXP (MC33GD3100EK and AEK, respectively).

If VDD is fuse-programmed to 3.3 V, then the user must supply VSUP with a voltage source greater than VSUPUV_TH, usually battery in a vehicle. In this case, power for VDD is always derived from VSUP; an external VDD supply is not allowed. The MC33GD3100A3EK cannot be powered exclusively by VDD = 3.3 V.

If VDD is fuse-programmed to 5.0 V, the IC can be powered from a single voltage source at VSUP. In this case, VDD is derived from VSUP.

If VDD is fuse-programmed to 5.0 V, the IC can be powered from a single, 5.0 V source. In this case, VSUP and VDD must be connected on the PCB. Since an externally supplied V_{VSUP} never exceeds VSUPUV_TH, the internal VDD regulator is never turned on.

8.3 Features

The MC33GD3100 is designed for a wide range of IGBT voltage ratings. Its logic interface and feedback signals are galvanically isolated from the high voltage circuitry that directly drives the IGBT gate and monitors its temperature sense, DESAT, CLAMP and current sense pins.

The MC33GD3100 is built with two domains and each has its own GND reference. Control and fault signals are transmitted between the non-isolated, “low voltage” domain (LV domain) and the isolated, "high voltage" domain (HV domain) via magnetic coupling. GND1 must be connected to the logic controller’s GND. GND2 must be connected to the IGBT’s emitter.

Pins 1 through 16 are connected to the low voltage domain. These pins provide interface to all the control, programming, fault monitoring and fail-safe features. A power supply connected to the VSUP pin provides power for low voltage domain.

Pins 17 through 32 are connected to the high voltage domain. These pins provide the interface to the IGBT gate, its power supplies and its terminals (collector sense,

temperature sense and current sense). A power supply connected to the VCC pin provides power for the high voltage domain.

VCC and VEE are the positive and negative power supplies used to charge and discharge the IGBT's gate. VCCREG is the output of a post regulator. This post regulator can be used to minimize positive supply voltage variation when multiple gate voltage supplies are generated from a single source.

The gate drive stage consists of three transistors and a current source. The GH transistor is a high current pullup (gate charging) transistor connected between VCCREG and the GH pin. Pins GL and AMC have separate transistors that provide gate discharge paths. GL is intended to be used as the primary turn-off path with an external resistor used to control discharge current. The AMC pin provides an "Active Miller Clamp", which clamps the IGBT's gate to its emitter when the IGBT is off. The GH, GL and AMC transistors are capable of currents up to 10 A for 2.0 µs. A soft shutdown current source is in parallel with the GL transistor. Its role is to provide a slower gate discharge during a short-circuit condition. Fault conditions can trigger a "two level turn-off" (2LTO). If this feature is enabled, the gate drive temporarily decreases the IGBT's gate voltage while the possible fault is being validated. Reducing the gate voltage limits the maximum fault current and thereby lessens the safe operating area stress on the IGBT.

The MC33GD3100 can be used with or without a negative gate drive voltage. Negative gate voltage is often used to ensure an IGBT is kept off when its opposing IGBT is turning on. However, using a negative supply increases gate drive losses and complicates the gate drive power supply. Using a low impedance turn off circuit is another way to alleviate or eliminate the problem of dv/dt induced turn on. The AMC transistor provides a very low turn off impedance to hold the IGBT off when the other half-bridge IGBT devices turns on.

By monitoring the IGBT's collector-emitter voltage, the MC33GD3100 can provide two means of protection. When the IGBT is commanded on, its V_{CE} should be only a few volts at most. A short-circuit condition is likely to cause the IGBT's V_{CE} to exceed its normal on-state voltage. The MC33GD3100's V_{CE} desaturation detection circuitry monitors V_{CE} for this condition.

Active clamping of V_{CE} via a zener placed across the IGBT's collector-gate terminals is another fault management technique. The MC33GD3100 monitors the zener clamp and reduces the turn-off gate drive when excessive V_{CE} is present. Reducing the gate discharge current improves clamping tolerance and reduces the size of the zeners.

The current sense pin, ISENSE, can be used to monitor the sense cells of a current sense IGBT. Responding directly to an overcurrent or short-circuit condition using current sensing can be a much faster way to respond to a severe overcurrent condition (as compared to desaturation detection).

The MC33GD3100 can also monitor temperature sense diodes if the IGBT has them. An ADC allows reporting the temperature via the SPI as well as using the ADC reading to trigger overtemperature warning or fault conditions. Monitoring the IGBT's temperature via the AOUT pin also allows real time monitoring of the system's performance in the field.

The MC33GD3100's AMUX pin provides a means to read other important system voltages, which can be duty cycle encoded and provided at the AOUT pin.

The IC has two ways to report fault and status data. The INTB pin immediately reports latched faults. It is active low when a fault occurs. The SPI can also report fault details as well as status and configuration information.

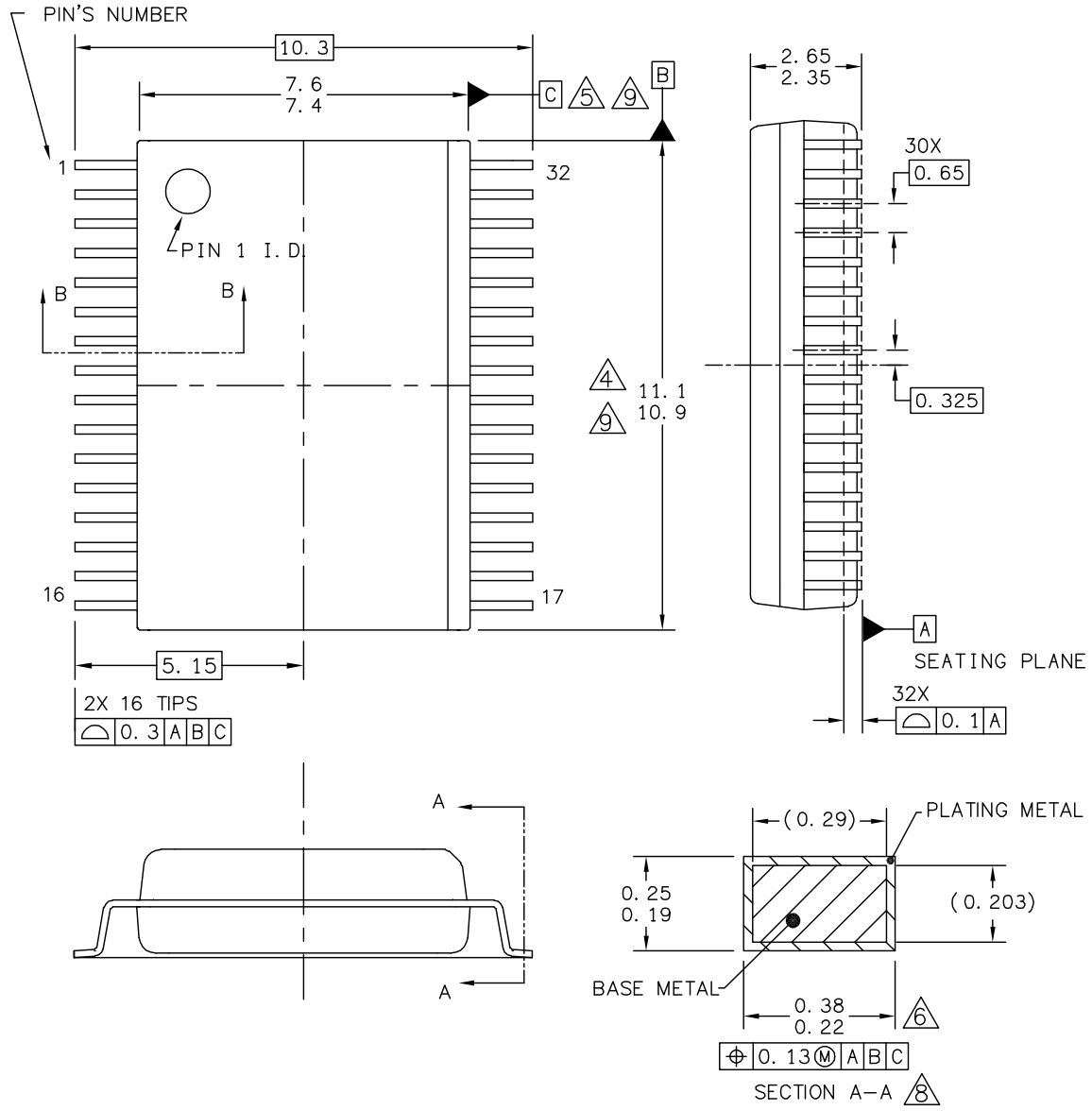
9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 4. Package outline

Package	Suffix	Package outline drawing number
32-pin wide body SOIC	EK	98ARH99137A



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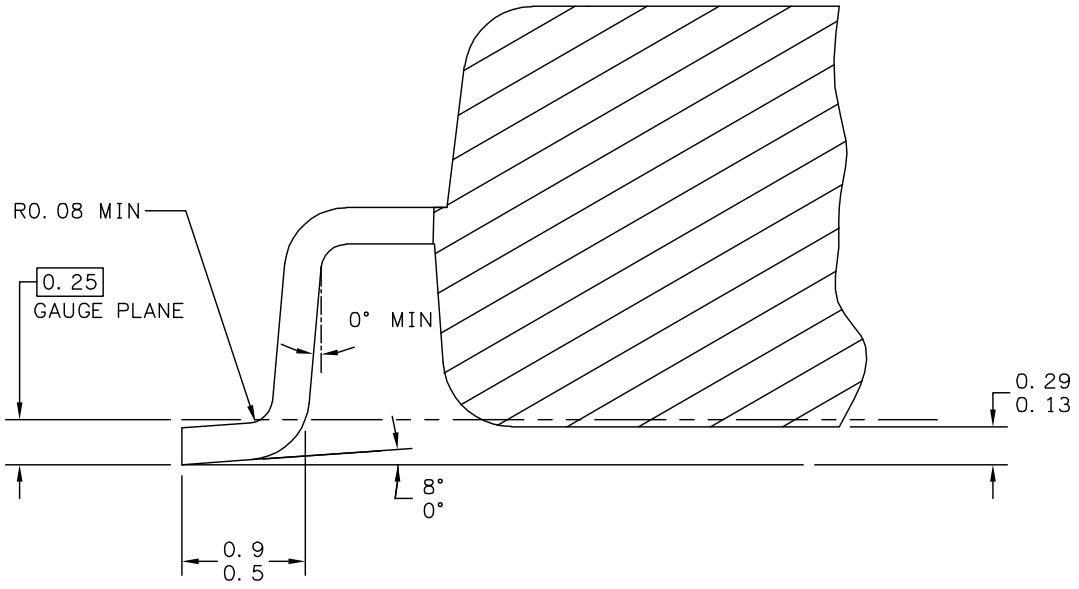
TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: C
	STANDARD: NON–JEDEC	
	SOT1762–1	29 FEB 2016



SECTION B–B

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TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: C
	STANDARD: NON-JEDEC	
	SOT1762-1	29 FEB 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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TITLE: 32LD SOIC W/B, 0.65 PITCH, CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: C
	STANDARD: NON–JEDEC	
	SOT1762–1	29 FEB 2016

10 Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33GD3100_SDS v.3.1	20181026	Advance information	—	MC33GD3100_SDS v.3.0
Modifications	• Updated revision number to align with the data sheet			
MC33GD3100_SDS v.3.0	20181011	Advance information	—	MC33GD3100_SDS v.2.0
Modifications	• Globally changed Die 1 and Die 2 to low voltage domain and high voltage domain, respectively			
MC33GD3100_SDS v.2.0	20180813	Advance information	—	MC33GD3100_SDS v.1.9
Modifications	• Added AEC-Q100 grade 1 qualified to Section 1 and Section 3			
MC33GD3100_SDS v.1.9	20180731	Advance information	—	MC33GD3100_SDS v.1.6
Modifications	• Updated revision number to align with the data sheet			
MC33GD3100_SDS v.1.6	20180419	Product preview	—	—

11 Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
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[2] The term 'short data sheet' is explained in section "Definitions".
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