MC34167, MC33167

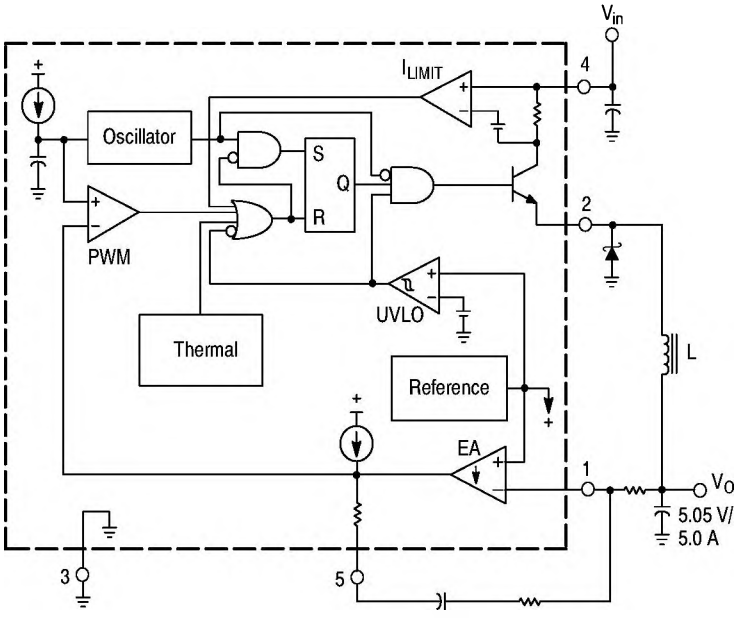
5.0 A, Step-Up/Down/ Inverting Switching Regulators

The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle–by–cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μA.

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^2PAK Package
- Moisture Sensitivity Level (MSL) Equals 1



This device contains 143 active transistors.

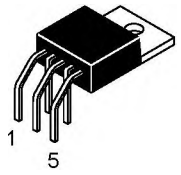
Figure 1. Simplified Block Diagram
(Step Down Application)

ON Semiconductor™

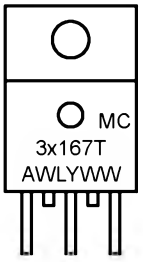
http://onsemi.com

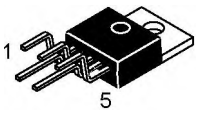
x = 3 or 4
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

MARKING DIAGRAMS

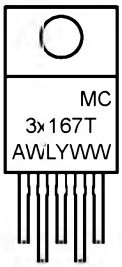


TO–220
TH SUFFIX
CASE 314A

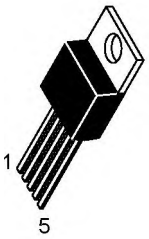




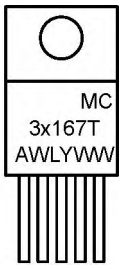
TO–220
TV SUFFIX
CASE 314B



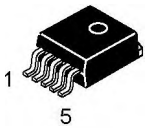
Heatsink surface connected to Pin 3



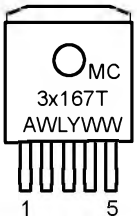
TO–220
T SUFFIX
CASE 314D



Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby



D^2PAK
D2T SUFFIX
CASE 936A



Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1562 of this data sheet.

MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	–2.0 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	–1.0 to + 7.0	V
Power Dissipation			
Case 314A, 314B and 314D (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936A (D^2PAK) (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34167 MC33167	T_A	 0 to + 70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL–STD–883, Method 3015.
   Machine Model Method 200 V.
3. T_{low} = 0°C for MC34167 T_{high} = + 70°C for MC34167
   = – 40°C for MC33167 = + 85°C for MC33167

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 4, 5], unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency (V_{CC} = 7.5 V to 40 V)	T_A = +25°C T_A = T_{low} to T_{high}	f_{OSC}	65 62	72 –	79 81	kHz
ERROR AMPLIFIER						
Voltage Feedback Input Threshold	T_A =+ 25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	4.95 4.85	5.05 –	5.15 5.20	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = +25°C)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)		I_{IB}	–	0.15	1.0	μA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)		PSRR	60	80	–	dB
Output Voltage Swing	High State (I_{Source} = 75 μA, V_{FB} = 4.5 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	V_{OH} V_{OL}	4.2 –	4.9 1.6	– 1.9	V
PWM COMPARATOR						
Duty Cycle (V_{CC} = 20 V)	Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	$DC_{(max)}$ $DC_{(min)}$	92 0	95 0	100 0	%
SWITCH OUTPUT						
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 5.0 A)		V_{sat}	–	(V_{CC} –1.5)	(V_{CC} –1.8)	V
Off–State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)		$I_{sw(off)}$	–	0	100	μA
Current Limit Threshold (V_{CC} = 7.5 V)		$I_{pk(switch)}$	5.5	6.5	8.0	A
Switching Times (V_{CC} = 40 V, I_{pk} = 5.0 A, L = 225 μH, T_A = +25°C) Output Voltage Rise Time Output Voltage Fall Time		 t_r t_f	 – –	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT						
Startup Threshold (V_{CC} Increasing, T_A = +25°C)		$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = +25°C)		$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE						
Power Supply Current (T_A = +25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)		I_{CC}	 – –	 36 40	 100 60	 μA mA

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. T_{low} = 0°C for MC34167 T_{high} = + 70°C for MC34167
   = – 40°C for MC33167 = + 85°C for MC33167

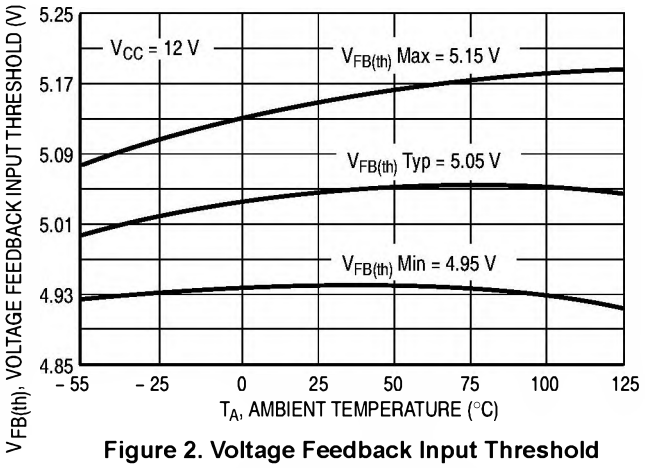


Figure 2. Voltage Feedback Input Threshold versus Temperature

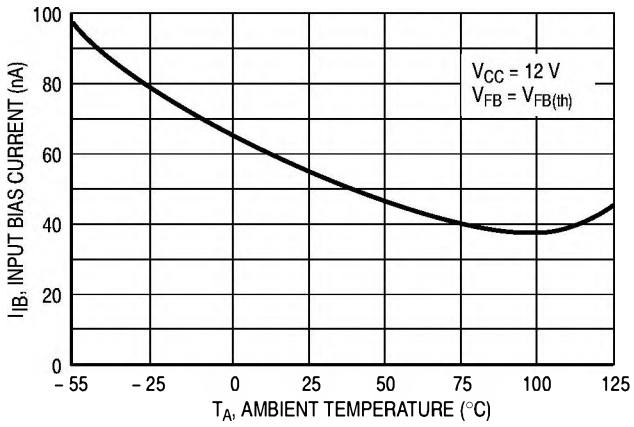


Figure 3. Voltage Feedback Input Bias Current versus Temperature

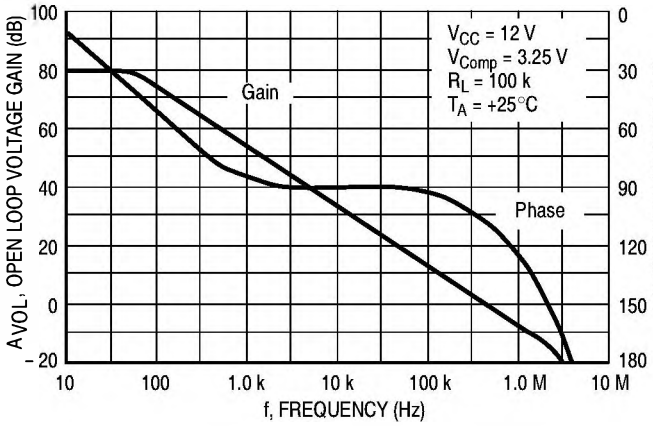


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

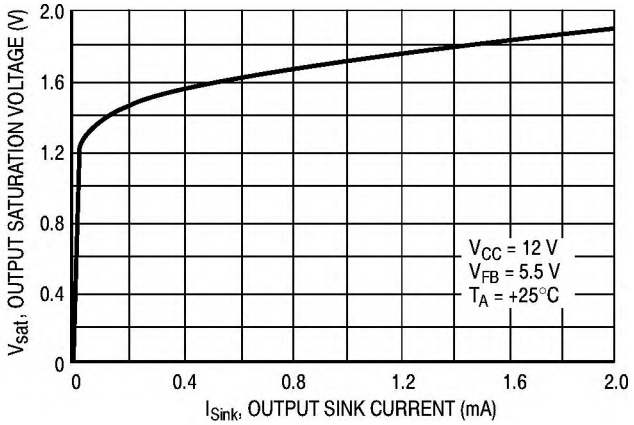


Figure 5. Error Amp Output Saturation versus Sink Current

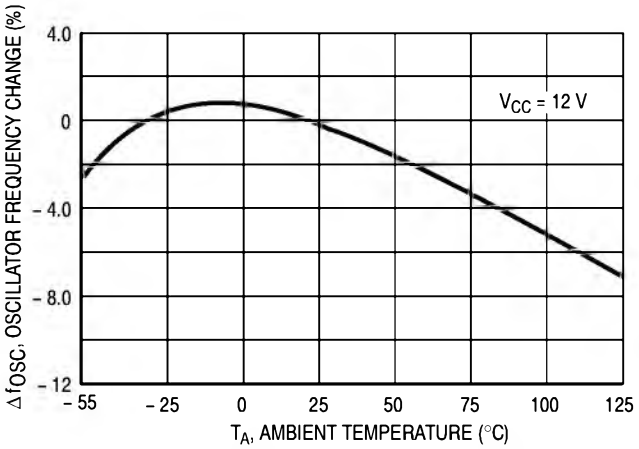


Figure 6. Oscillator Frequency Change versus Temperature

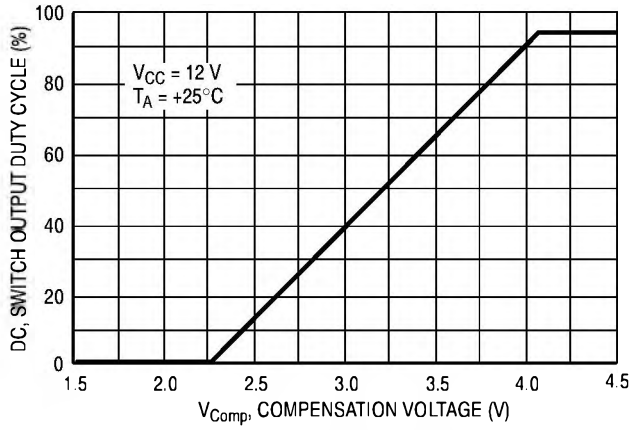


Figure 7. Switch Output Duty Cycle versus Compensation Voltage

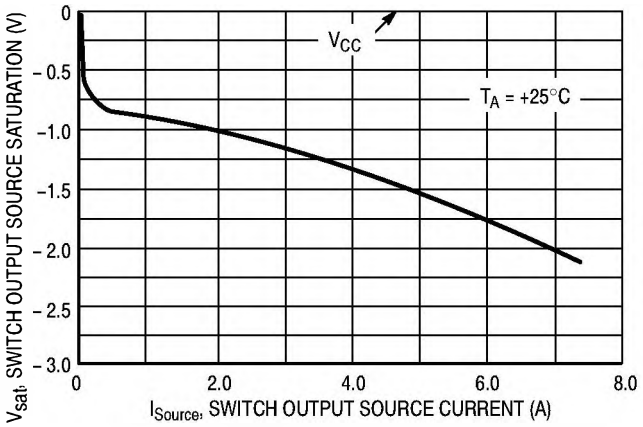


Figure 8. Switch Output Source Saturation versus Source Current

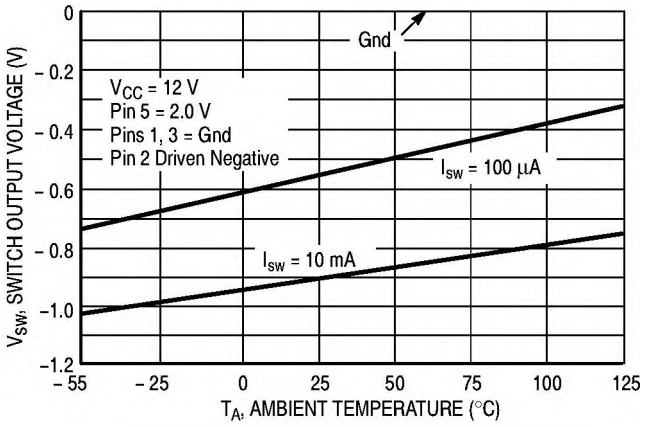


Figure 9. Negative Switch Output Voltage versus Temperature

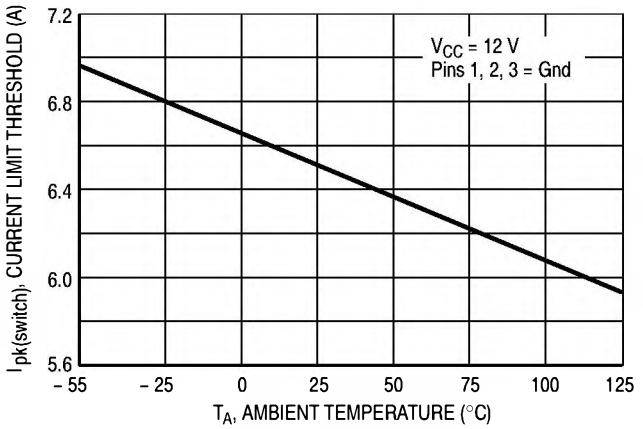


Figure 10. Switch Output Current Limit Threshold versus Temperature

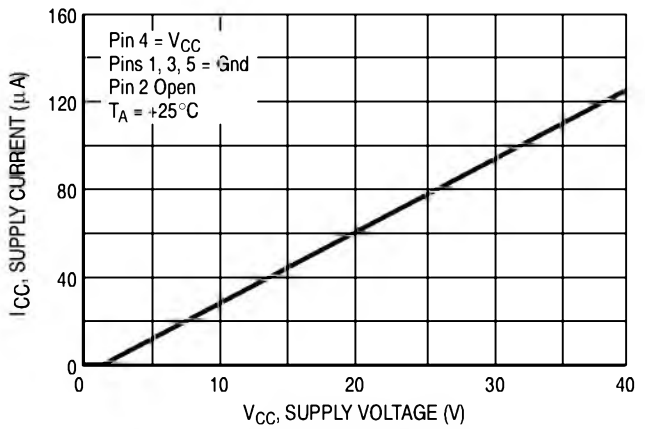


Figure 11. Standby Supply Current versus Supply Voltage

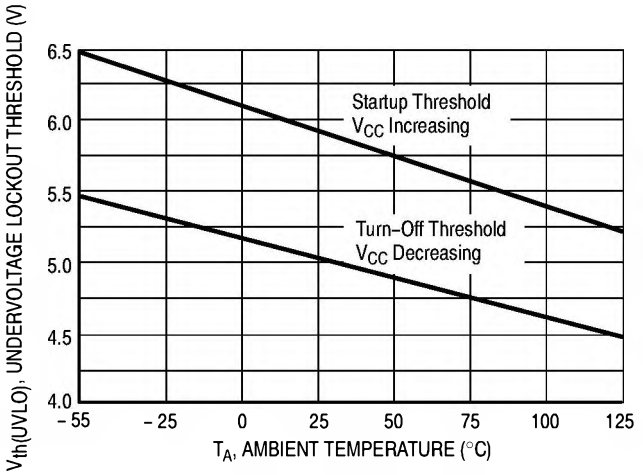


Figure 12. Undervoltage Lockout Thresholds versus Temperature

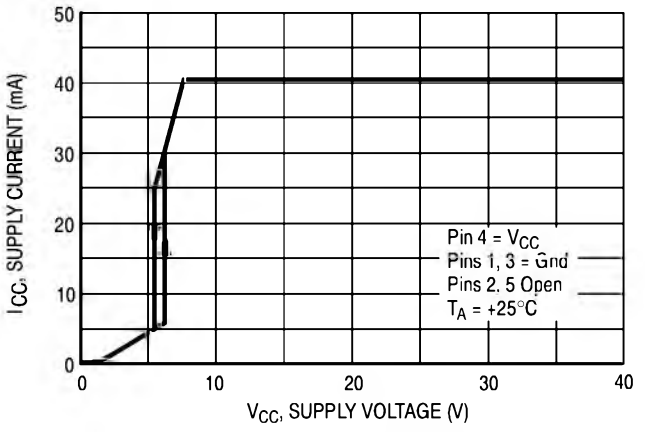


Figure 13. Operating Supply Current versus Supply Voltage

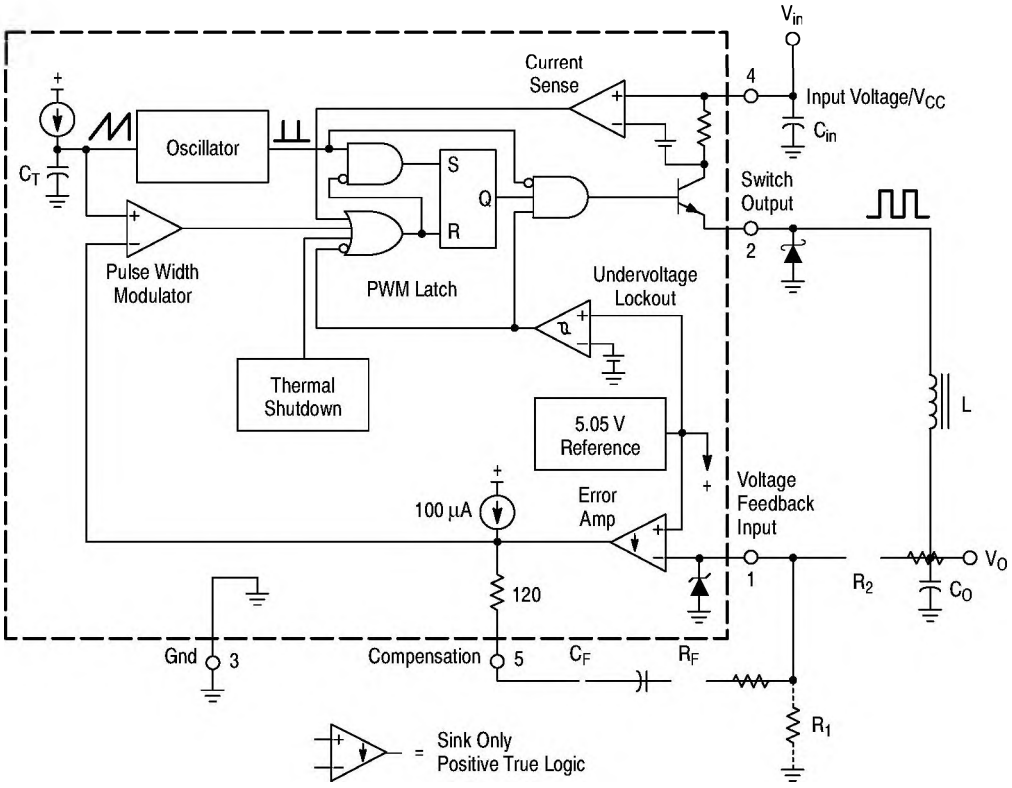


Figure 14. MC34167 Representative Block Diagram

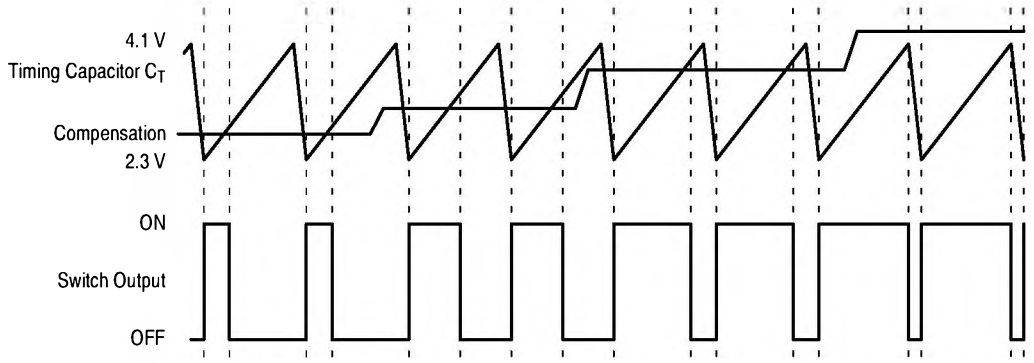


Figure 15. Timing Diagram

INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for dc–to–dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. They can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 14.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp–up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 7 and 15 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34167 series utilizes cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A. Figure 10 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 4). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 14 and 19. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05\left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step–down converter (Figure 19) is the easiest to compensate for stability. The step–up (Figure 21) and voltage–inverting (Figure 23) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μA with a 12 V supply voltage. Figure 11 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μA current source pull–up that can be used to implement soft–start. Figure 18 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 5.5 A. When configured for step–down or voltage–inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34167 is contained in a 5–lead TO–220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{in}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

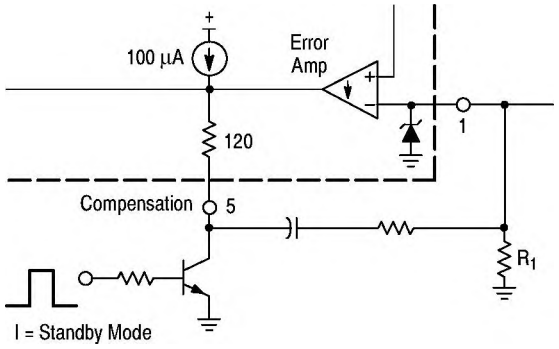


Figure 16. Low Power Standby Circuit

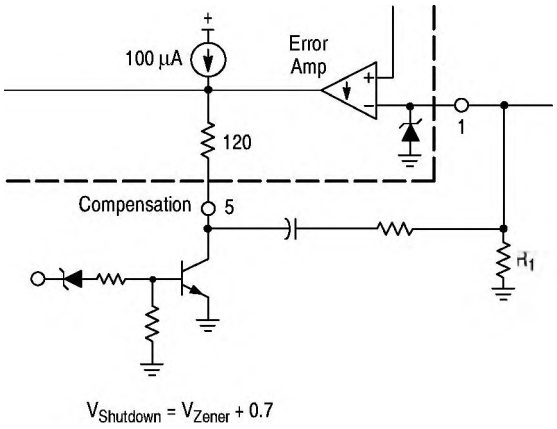


Figure 17. Over Voltage Shutdown Circuit

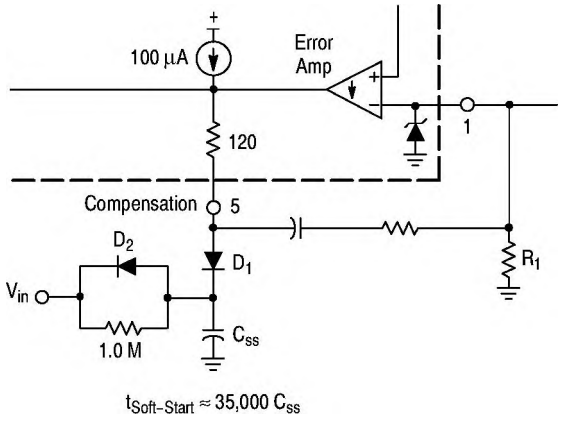
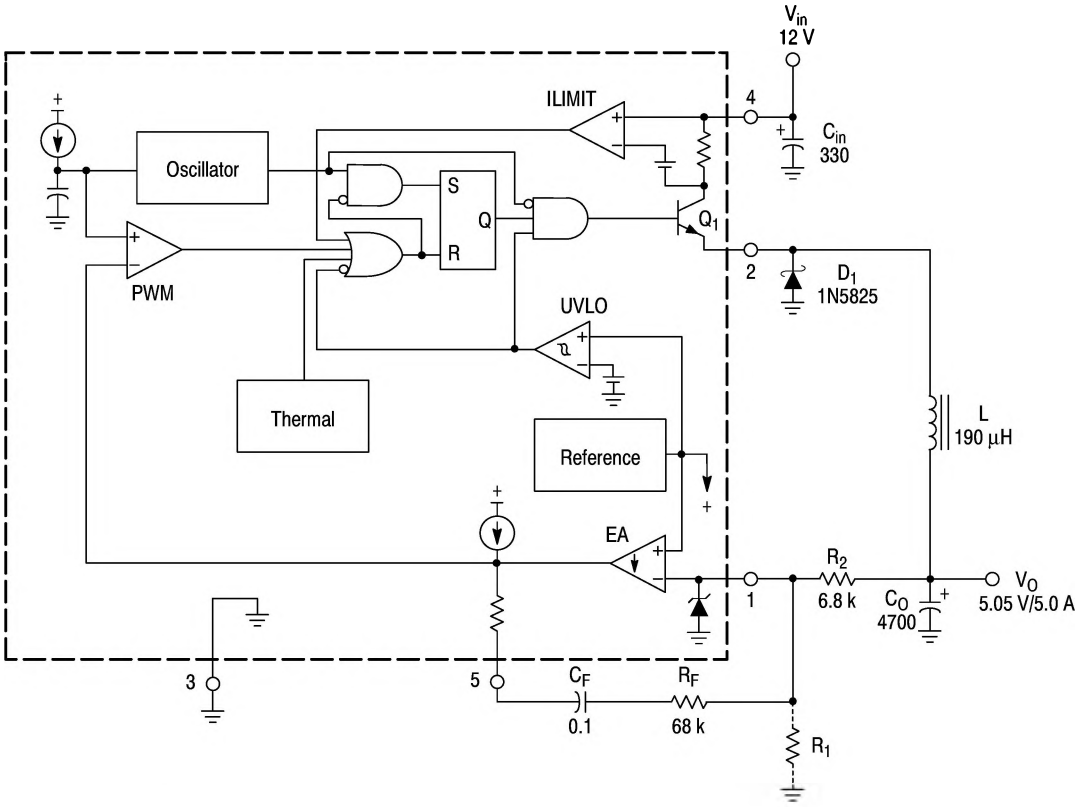


Figure 18. Soft–Start Circuit



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 36 V, I_O = 5.0 A	4.0 mV = ± 0.039%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 5.0 A	1.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 5.0 A	20 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.5 A
Efficiency	V_{in} = 12 V, I_O = 5.0 A V_{in} = 24 V, I_O = 5.0 A	78.9% 82.6%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure 19. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step–Down Converter

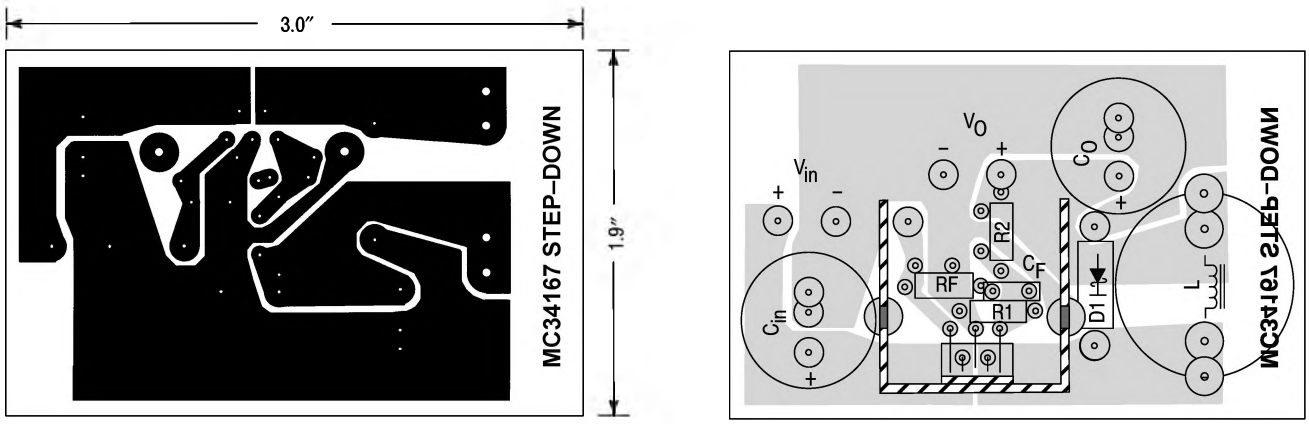
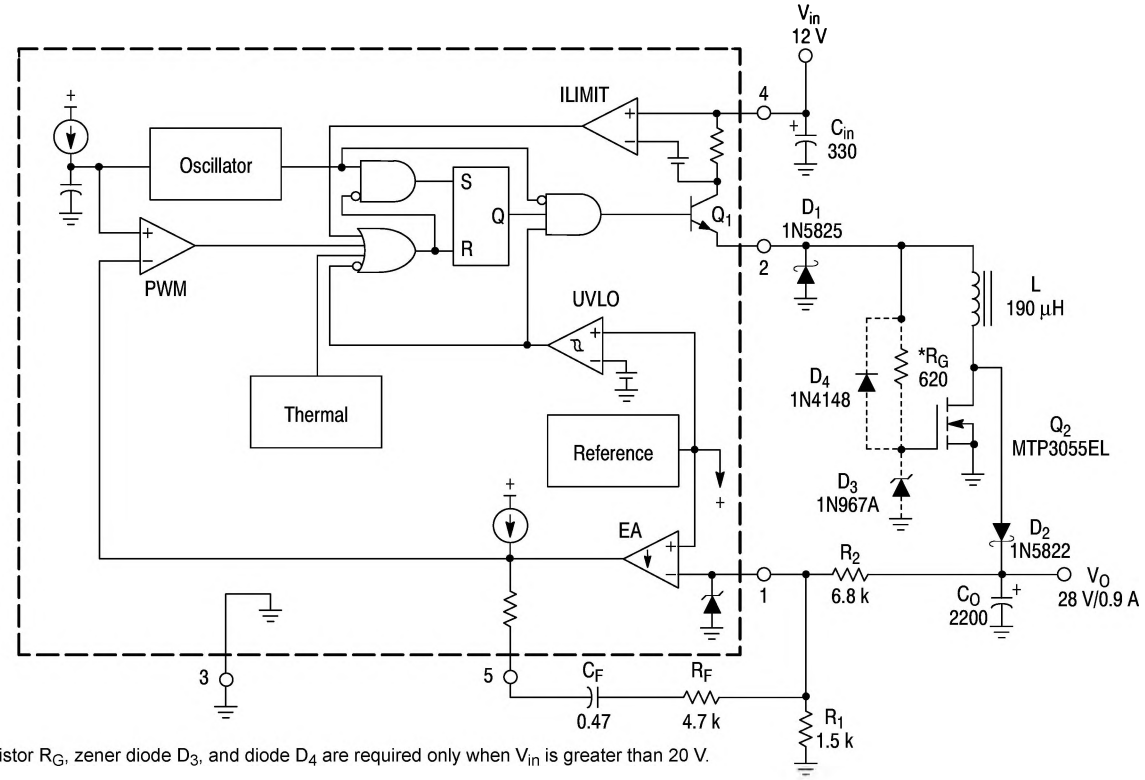


Figure 20. Step–Down Converter Printed Circuit Board and Component Layout



*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 0.9 A	10 mV = ± 0.017%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.9 A	30 mV = ± 0.053%
Output Ripple	V_{in} = 12 V, I_O = 0.9 A	140 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.0 A
Efficiency	V_{in} = 12 V, I_O = 0.9 A V_{in} = 24 V, I_O = 0.9 A	80.1% 87.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc. MC34167: 5903B, or 5930B MTP3055EL: 5925B

Figure 21 shows that the MC34167 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors Q_1 and Q_2. During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the OFF time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G, D_3, and D_4.

Figure 21. Step–Up/Down Converter

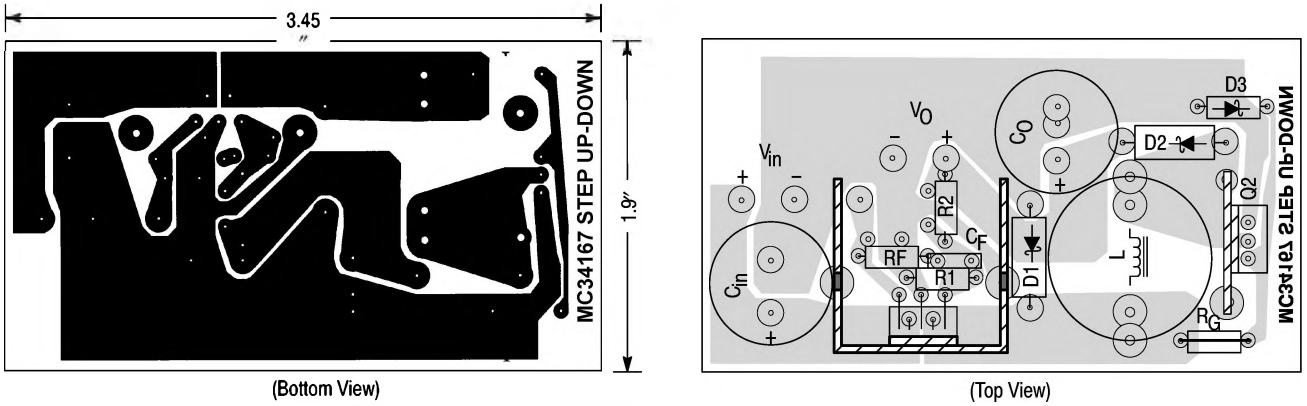
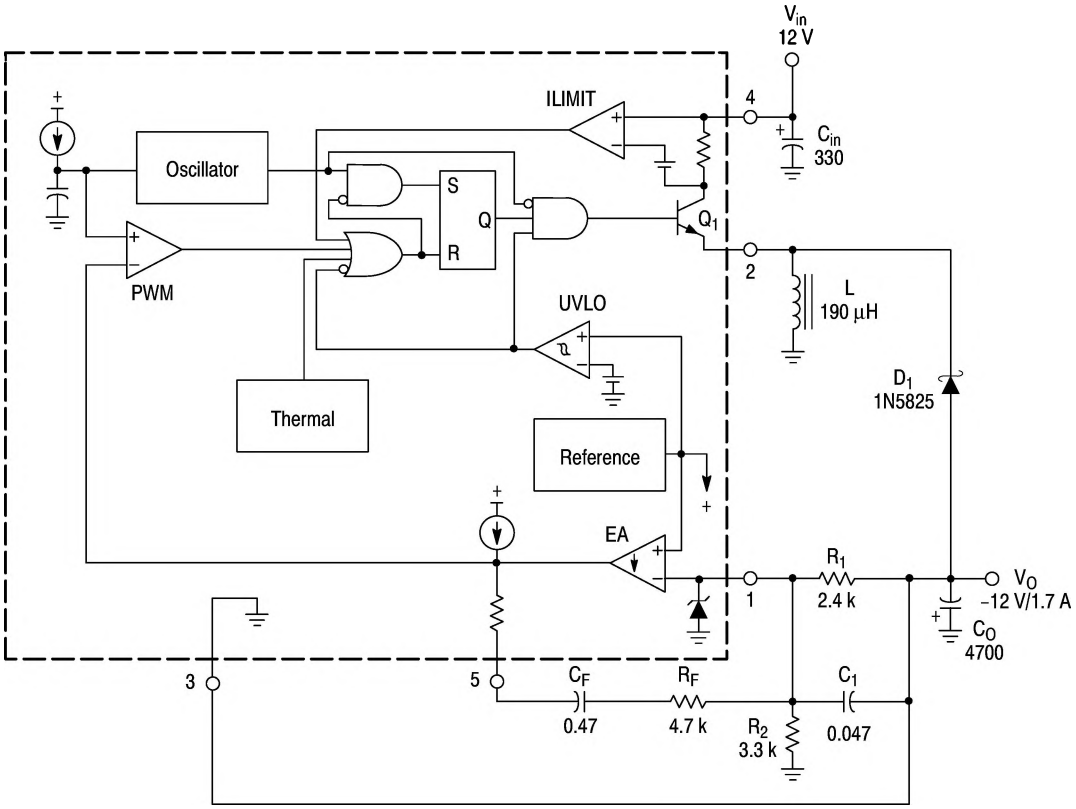


Figure 22. Step–Up/Down Converter Printed Circuit Board and Component Layout



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 1.7 A	15 mV = ± 0.61%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.7 A	4.0 mV = ± 0.020%
Output Ripple	V_{in} = 12 V, I_O = 1.7 A	78 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	5.7 A
Efficiency	V_{in} = 12 V, I_O = 1.7 A V_{in} = 24 V, I_O = 1.7 A	79.5% 86.2%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the MC34167. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 23. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage–Inverting Converter

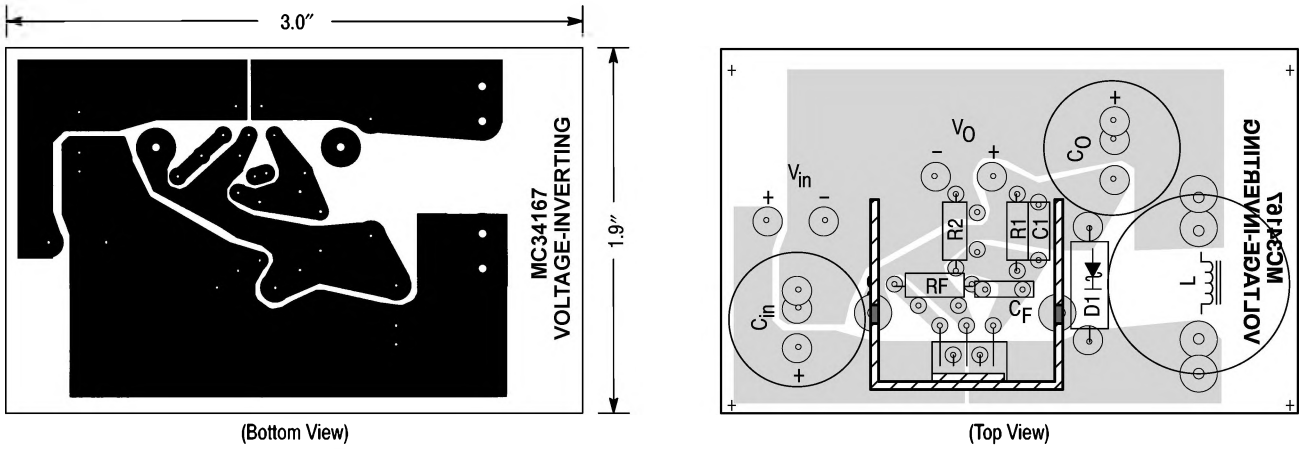


Figure 24. Voltage–Inverting Converter Printed Circuit Board and Component Layout

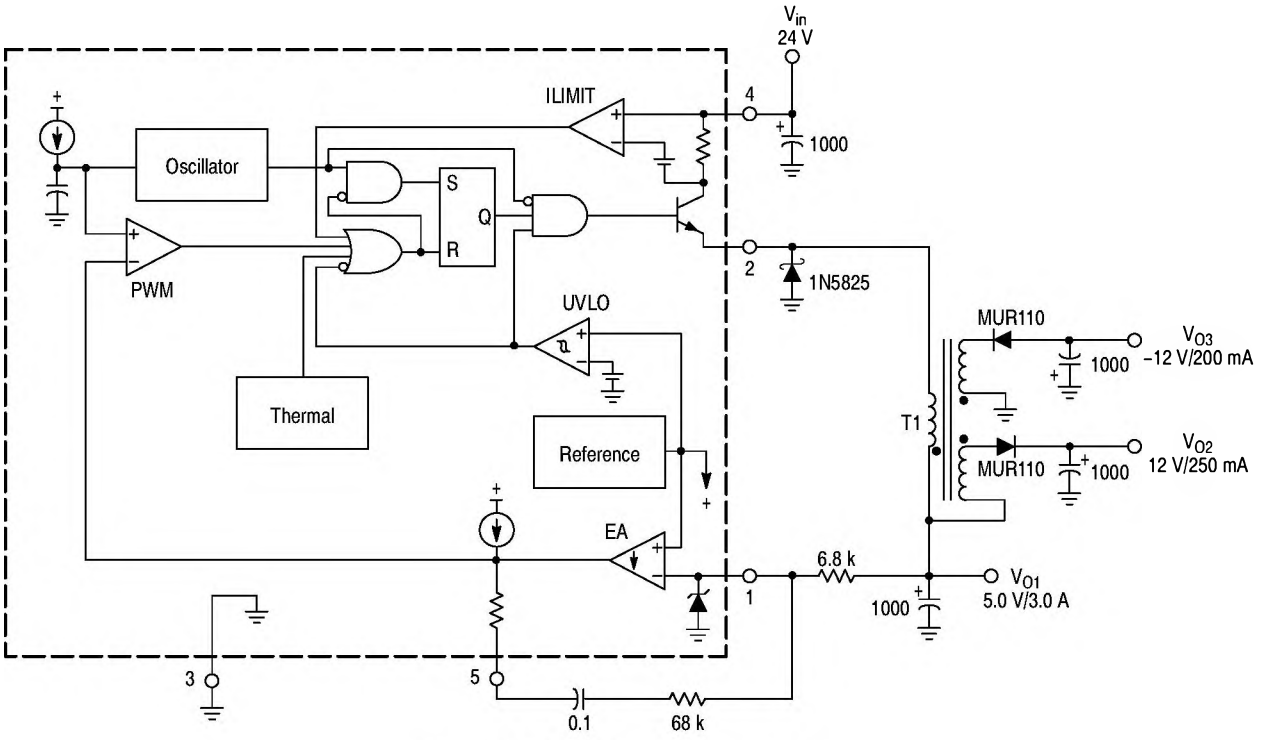


Figure 25. Triple Output Converter

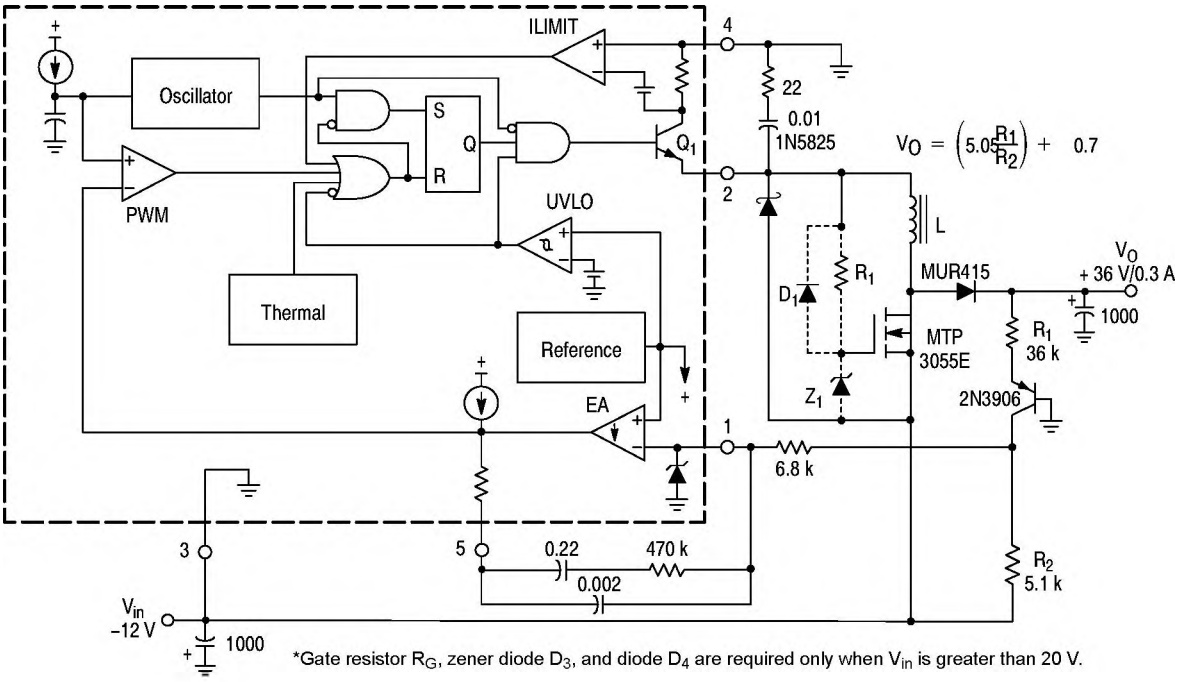
Tests		Conditions	Results
Line Regulation	5.0 V 12 V −12 V	V_{in} = 15 V to 30 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	3.0 mV = ± 0.029% 572 mV = ± 2.4% 711 mV = ± 2.9%
Load Regulation	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 30 mA to 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 100 mA to 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 75 mA to 200 mA	1.0 mV = ± 0.009% 409 mV = ±1.5% 528 mV = ± 2.0%
Output Ripple	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	75 mV_{pp} 20 mV_{pp} 20 mV_{pp}
Short Circuit Current	5.0 V 12 V −12 V	V_{in} = 24 V, R_L = 0.1 Ω	6.5 A 2.7 A 2.2 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	84.2%

T1 = Primary: Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Secondary: V_{O2} – 69 turns of #26 AWG
V_{O3} – 104 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\,TURNS_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\frac{V_{O(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

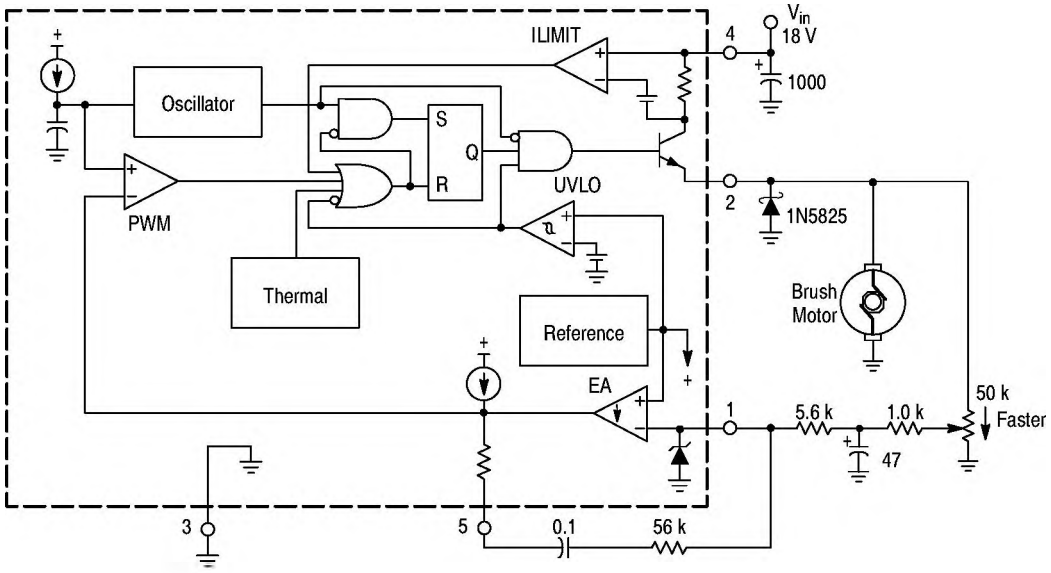
Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.



Test	Conditions	Results
Line Regulation	V_{in} = –10 V to – 20 V, I_O = 0.3 A	266 mV = ± 0.38%
Load Regulation	V_{in} = –12 V, I_O = 0.03 A to 0.3 A	7.90 mV = ±1.1%
Output Ripple	V_{in} = –12 V, I_O = 0.3 A	100 mV_{pp}
Efficiency	V_{in} = –12 V, I_O = 0.3 A	78.4%

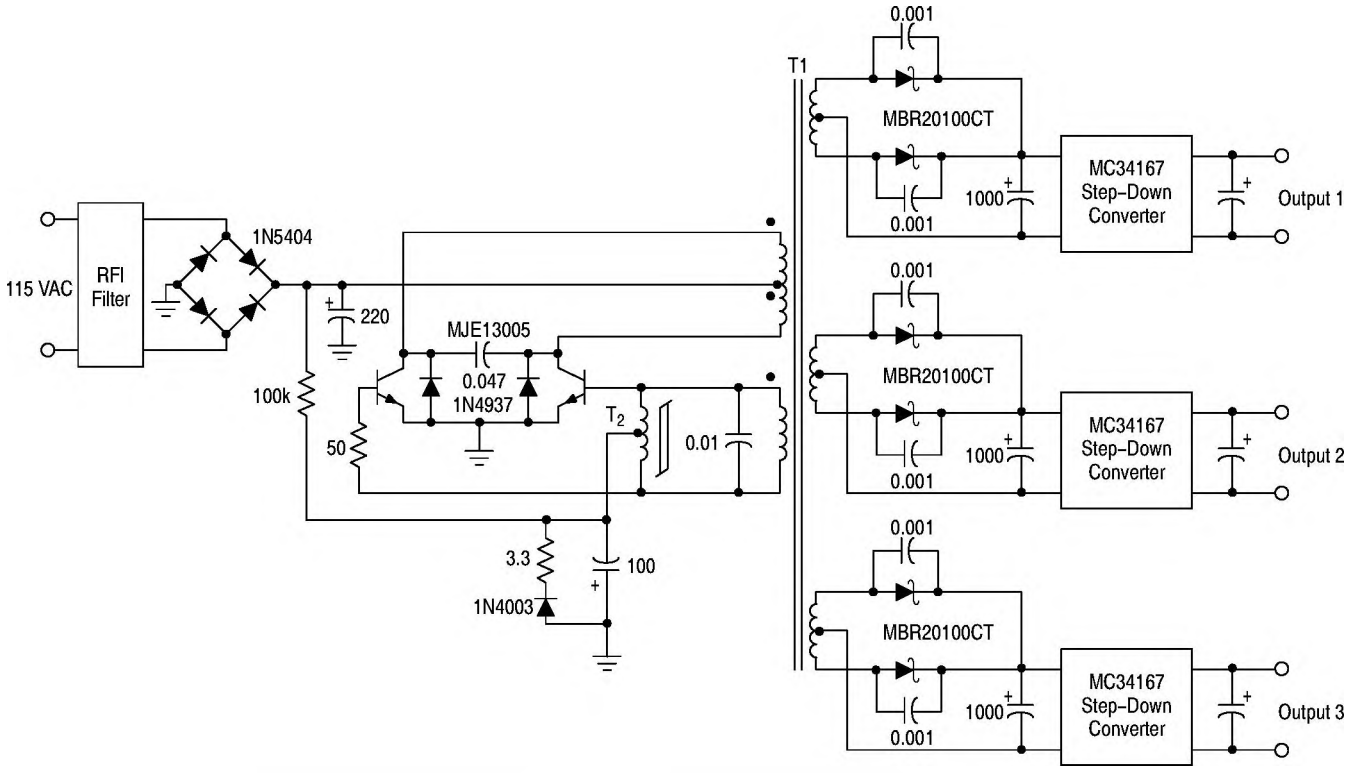
L = General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 26. Negative Input/Positive Output Regulator



Test	Conditions	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

Figure 27. Variable Motor Speed Control with EMF Feedback Sensing



T_1 = Core and Bobbin – Coilcraft PT3595
Primary – 104 turns #26 AWG
Base Drive – 3 turns #26 AWG
Secondaries – 16 turns #16 AWG
Total Gap – 0.002,

T_2 = Core – TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
MC34167 and MJE13005 – 5903B
MBR20100CT – 5925B

The MC34167 can be used cost effectively in off–line applications even though it is limited to a maximum input voltage of 40 V. Figure 28 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self–oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. Off–Line Preconverter

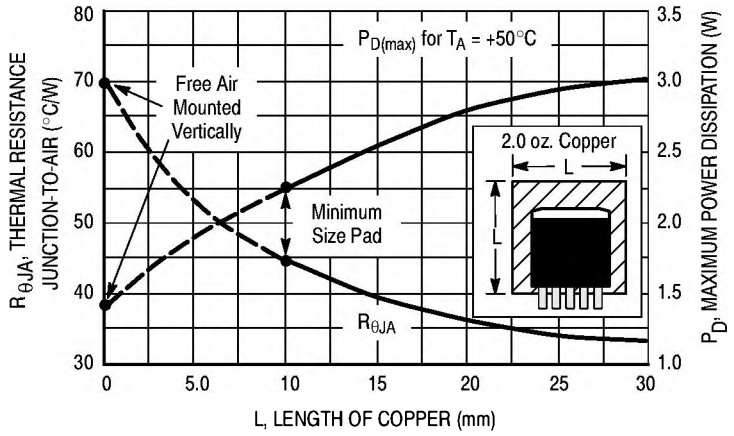


Figure 29. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

Table 1. Design Equations

Calculation	Step–Down	Step–Up/Down	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$
Duty Cycle (Note 3)	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right)t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

1. V_{sat} – Switch Output source saturation voltage, refer to Figure 8.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.35 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.

I_{out} – Desired output current.

ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 5.5 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_{L\ avg})$. This will proportionally reduce the converter's output current capability.

$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
MC33167D2T	T_A = –40° to +85°C	D^2PAK (Surface Mount)	50 Units/Rail
MC33167T		TO–220 (Straight Lead)	
MC33167TH		TO–220 (Horizontal Mount)	
MC33167TV		TO–220 (Vertical Mount)	
MC34167D2T	T_A = 0° to +70°C	D^2PAK (Surface Mount)	
MC34167T		TO–220 (Straight Lead)	
MC34167TH		TO–220 (Horizontal Mount)	
MC34167TV		TO–220 (Vertical Mount)	

CS51031

Fast PFET Buck Controller

The CS51031 is a switching controller for use in DC–DC converters. It can be used in the buck topology with a minimum number of external components. The CS51031 consists of a V_{CC} monitor for controlling the state of the device, 1.0 A power driver for controlling the gate of a discrete P–channel transistor, fixed frequency oscillator, short circuit protection timer, programmable soft start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable soft start reduces current surges at start up. The short circuit protection timer significantly reduces the duty cycle to approximately 1/30 of its cycle during short circuit conditions.

The CS51031 is available in 8 Lead SO and 8 Lead PDIP plastic packages.

Features

- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- V_{CC} Monitor
- 2.0% Precision Reference
- Programmable Soft Start
- Wide Ambient Temperature Range:
  - Industrial Grade: –40°C to 85°C
  - Commercial Grade: 0°C to 70°C

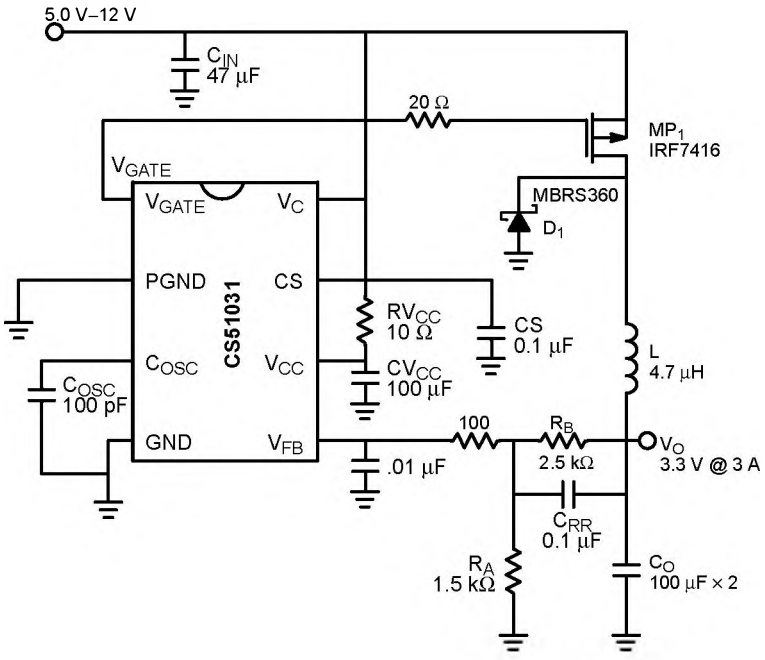


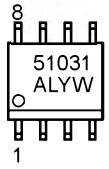
Figure 1. Typical Application Diagram

ON Semiconductor™

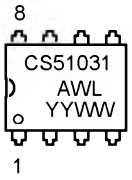
http://onsemi.com

MARKING DIAGRAMS

SO–8
D SUFFIX
CASE 751

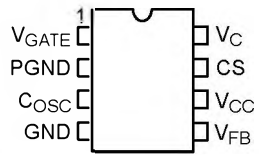


DIP–8
N SUFFIX
CASE 626



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Package	Shipping
CS51031YD8	SO–8	95 Units/Rail
CS51031YDR8	SO–8	2500 Tape & Reel
CS51031YN8	DIP–8	50 Units/Rail
CS51031GD8	SO–8	95 Units/Rail
CS51031GDR8	SO–8	2500 Tape & Reel

*Additional ordering information can be found on page 1571 of this data sheet.

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
Power Supply Voltage, V_{CC}		20	V
Driver Supply Voltage, V_C		20	V
Driver Output Voltage, V_{GATE}		20	V
C_{OSC}, CS, V_{FB} (Logic Pins)		6.0	V
Peak Output Current		1.0	A
Steady State Output Current		200	mA
Operating Junction Temperature, T_J		150	°C
Operating Temperature Range, T_A		–40 to 85	°C
Storage Temperature Range, T_S		–65 to 150	°C
ESD (Human Body Model)		2.0	kV
Lead Temperature Soldering:	Wave Solder: (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C

1. 10 sec. maximum.
2. 60 sec. max above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (Specifications apply for $4.5 \le V_{CC} \le 16$ V, $3.0 \text{ V} \le V_C \le 16$ V; Industrial Grade: –40°C < T_A < 85°C; –40°C < T_J < 125°C: Commercial Grade: 0°C < T_A < 70°C; 0°C < T_J < 125°C, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator	**V_{FB} = 1.2 V**				
Frequency	C_{OSC} = 470 pF	160	200	240	kHz
Charge Current	1.4 V < V_{COSC} < 2.0 V	–	110	–	μA
Discharge Current	2.7 V > V_{COSC} > 2.0 V	–	660	–	μA
Maximum Duty Cycle	1 – (t_{OFF}/t_{ON})	80.0	83.3	–	%
Short Circuit Timer	**V_{FB} = 1.0 V; CS = 0.1 μF; V_{COSC} = 2.0 V**				
Charge Current	1.0 V < V_{CS} < 2.0 V	175	264	325	μA
Fast Discharge Current	2.55 V > V_{CS} > 2.4 V	40	66	80	μA
Slow Discharge Current	2.4 V > V_{CS} > 1.5 V	4.0	6.0	10	μA
Start Fault Inhibit Time	0 V < V_{CS} < 2.5 V	0.70	0.85	1.40	ms
Valid Fault Time	2.6 V > V_{CS} > 2.4 V	0.2	0.3	0.45	ms
GATE Inhibit Time	2.4 V > V_{CS} > 1.5 V	9.0	15	23	ms
Fault Duty Cycle	–	2.5	3.1	4.6	%
CS Comparator	**V_{FB} = 1.0 V**				
Fault Enable CS Voltage	–	–	2.5	–	V
Max. CS Voltage	V_{FB} = 1.5 V	–	2.6	–	V
Fault Detect Voltage	V_{CS} when GATE goes high	–	2.4	–	V
Fault Inhibit Voltage	Minimum V_{CS}	–	1.5	–	V
Hold Off Release Voltage	V_{FB} = 0 V	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	V_{CS} = 1.5 V	0.725	0.866	1.035	V

ELECTRICAL CHARACTERISTICS (continued) (Specifications apply for $4.5 \le V_{CC} \le 16$ V, $3.0\ V \le V_C \le 16$ V; Industrial Grade: $-40°C < T_A < 85°C$; $-40°C < T_J < 125°C$: Commercial Grade: $0°C < T_A < 70°C$; $0°C < T_J < 125°C$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{FB} Comparators	**$V_{COSC} = V_{CS} = 2.0$ V**				
Regulator Threshold Voltage	$T_J = 25°C$ (Note 3) $T_J = -40$ to $125°C$	1.225 1.210	1.250 1.250	1.275 1.290	V V
Fault Threshold Voltage	$T_J = 25°C$ (Note 3) $T_J = -40$ to $125°C$	1.12 1.10	1.15 1.15	1.17 1.19	V V
Threshold Line Regulation	$4.5\ V \le V_{CC} \le 16$ V	–	6.0	15	mV
Input Bias Current	$V_{FB} = 0$ V	–	1.0	4.0	μA
Voltage Tracking	(Regulator Threshold – Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage	–	–	4.0	20	mV
Power Stage	**$V_{CC} = V_C = 10$ V; $V_{FB} = 1.2$ V**				
GATE DC Low Saturation Voltage	$V_{COSC} = 1.0$ V; 200 mA Sink	–	1.2	1.5	V
GATE DC High Saturation Voltage	$V_{COSC} = 2.7$ V; 200 mA Source; $V_C = V_{GATE}$	–	1.5	2.1	V
Rise Time	$C_{GATE} = 1.0$ nF; $1.5\ V < V_{GATE} < 9.0$ V	–	25	60	ns
Fall Time	$C_{GATE} = 1.0$ nF; $9.0\ V > V_{GATE} > 1.5$ V	–	25	60	ns
V_{CC} Monitor					
Turn On Threshold	–	4.200	4.400	4.600	V
Turn Off Threshold	–	4.085	4.300	4.515	V
Hysteresis	–	65	130	200	mV
Current Drain					
I_{CC}	$4.5\ V < V_{CC} < 16$ V, Gate switching	–	4.5	6.0	mA
I_C	$3.0\ V < V_C < 16$ V, Gate non–switching	–	2.7	4.0	mA
Shutdown I_{CC}	$V_{CC} = 4.0$	–	500	900	μA

3. Guaranteed by design, not 100% tested in production.

PACKAGE LEAD DESCRIPTION

PACKAGE PIN NUMBER		PIN SYMBOL	FUNCTION
SO–8	DIP–8		
1	1	V_{GATE}	Driver pin to gate of external PFET.
2	2	PGND	Output power stage ground connection.
3	3	C_{OSC}	Oscillator frequency programming capacitor.
4	4	GND	Logic ground.
5	5	V_{FB}	Feedback voltage input.
6	6	V_{CC}	Logic supply voltage.
7	7	CS	Soft start and fault timing capacitor.
8	8	V_C	Driver supply voltage.

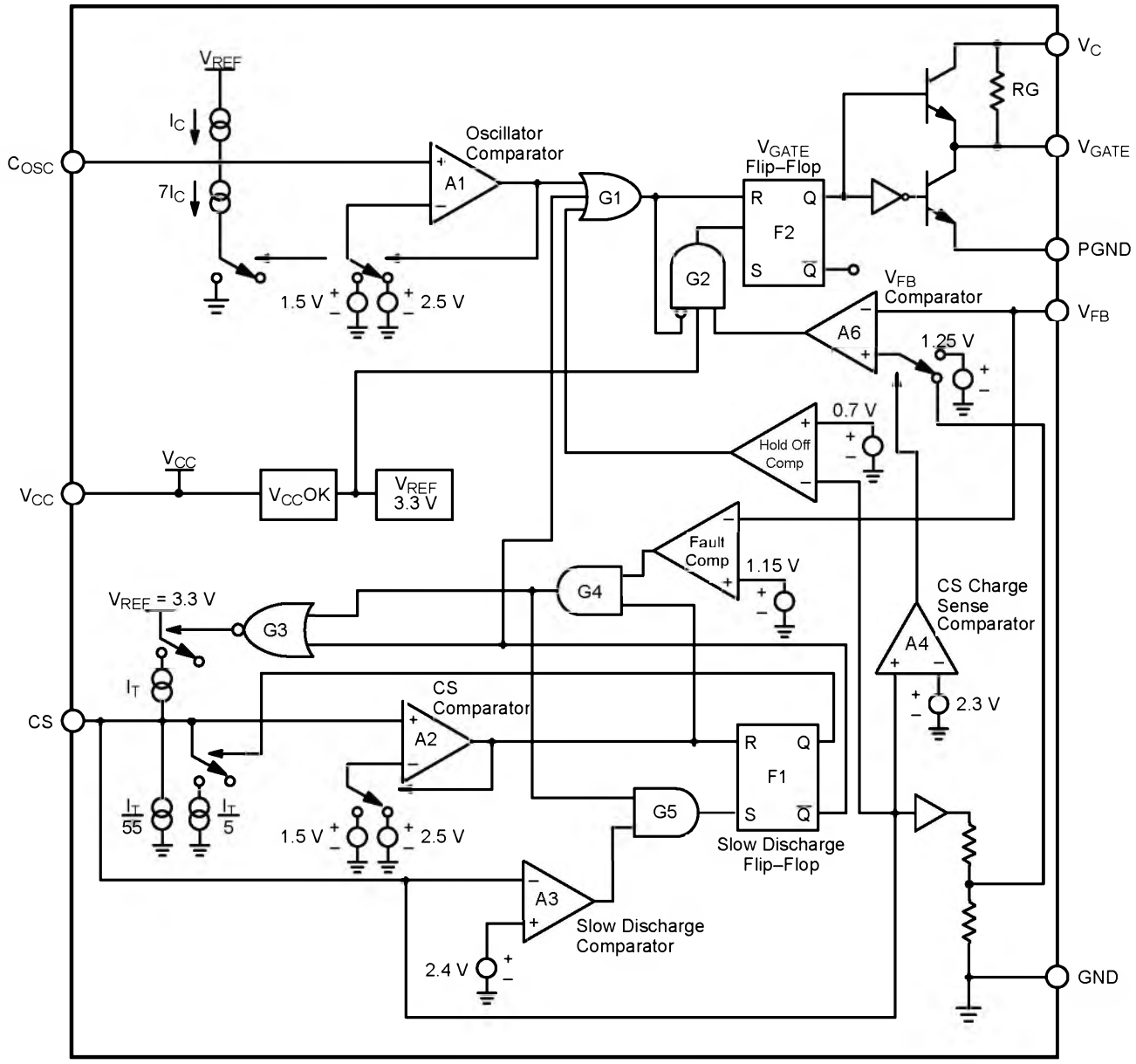


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

THEORY OF OPERATION

Control Scheme

The CS51031 monitors and the output voltage to determine when to turn on the PFET. If V_{FB} falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the PFET is turned on and remains on for the duration of the charge time. The PFET gets turned off and remains off during the oscillator's discharge time with the maximum duty cycle to 80%. It requires 7.0 mV typical, and 20 mV maximum ripple on the V_{FB} pin is required to operate. This method of control does not require any loop stability compensation.

Startup

The CS51031 has an externally programmable soft start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the PFET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft Start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source IC and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5}\right)$$

The internal Holdoff Comparator ensures that the external PFET is off until $V_{CS} > 0.7$ V, preventing the GATE flip–flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V, the low feedback to the V_{FB} Comparator sets the GATE flip–flop during C_{OSC} 's charge cycle. Once the GATE flip–flop is set, V_{GATE} goes low and turns on the PFET. When V_{CS} exceeds 2.4 V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25 V completing the startup cycle.

Lossless Short Circuit Protection

The CS51031 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5 V during startup, the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6 V. During a short circuit or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15 V, the output of the fault comparator goes high and the CS51031 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V. If the V_{FB} voltage is still below 1.15 V when the CS pin reaches 2.4 V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip flop. The V_{GATE} flip flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V. The CS51031 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V, the fast and slow discharge cycles repeat as shown in figure 3.

If the V_{FB} voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V. This reduces the chance of erroneously detecting a load transient as a fault condition.

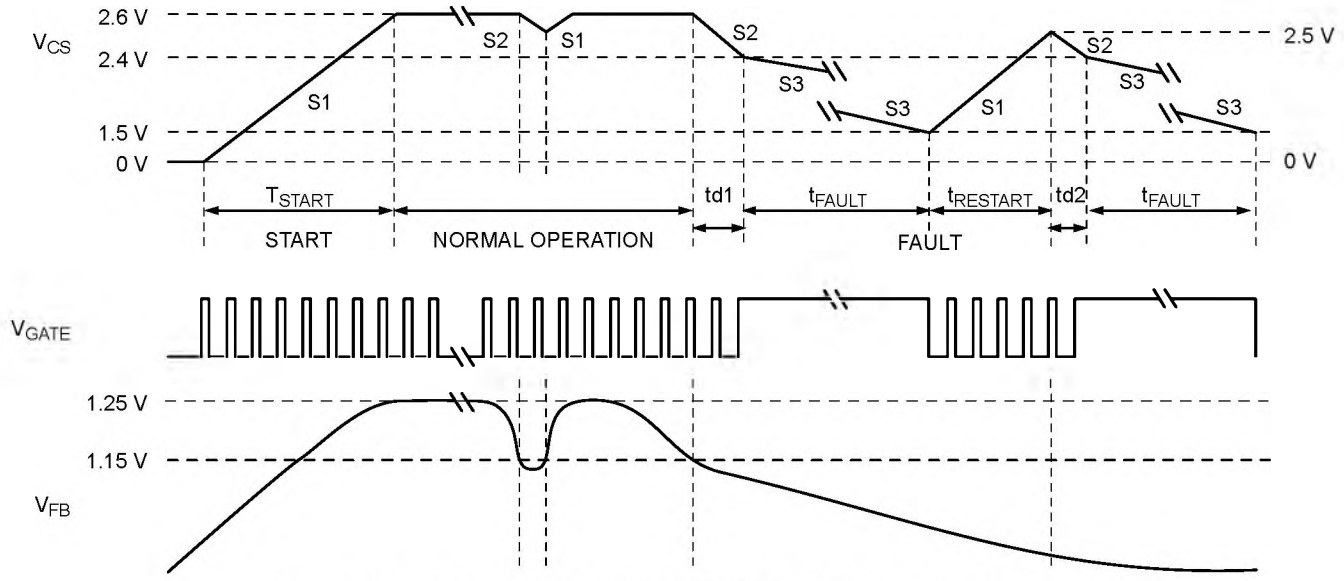


Figure 3. Voltage on Start Capacitor (V_{GS}), the Gate (V_{GATE}), and in the Feedback Loop (V_{FB}), During Startup, Normal and Fault Conditions.

Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O. When the voltage across C_O drops below the threshold established by the feedback resistors R1 and R2 and the reference voltage V_{REF}, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN} - V_{OUT})/L$. The duty cycle (or "on" time) for the CS51031 is limited to 80%. If output voltage remains higher than nominal during the entire C_{OSC} change time, the Q1 does not turn on, skipping the pulse.

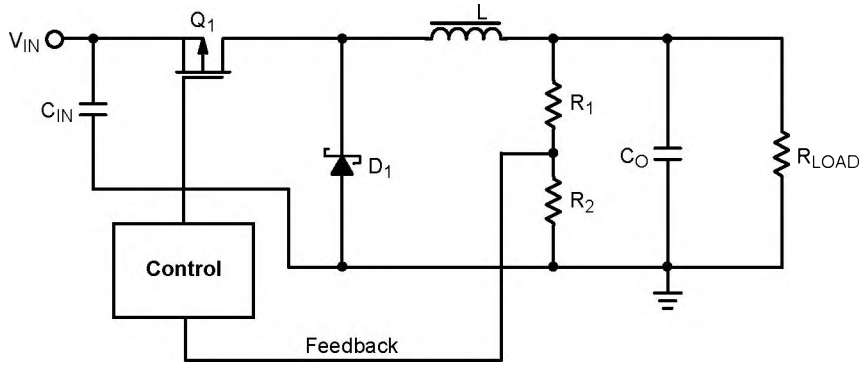


Figure 4. Buck Regulator Block Diagram.

APPLICATIONS INFORMATION

CS51031 DESIGN EXAMPLE

Specifications 12 V to 5.0 V, 3.0 A Buck Controller

- V_{IN} = 12 V ±20% (i.e. 14.4 V max., 12 V nom., 9.6 V min.)
- V_{OUT} = 5.0 V ±2%
- I_{OUT} = 0.3 A to 3.0 A
- Output ripple voltage < 50 mV max.
- Efficiency > 80%
- f_{SW} = 200 kHz

1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51031 is limited to 80% min., it is necessary to estimate the duty cycle for the various input conditions over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_F}{V_{IN} - V_{SAT}}$$

where:

$V_{SAT} = R_{ds(on)} \times I_{OUT}$ max. and $R_{ds(on)}$ is the value at T_J 100°C.

If V_F = 0.60 V and V_{SAT} = 0.60 V then the above equation becomes:

$$D_{MAX} = \frac{5.6}{9.0} = 0.62$$

$$D_{MIN} = \frac{5.6}{13.8} = 0.40$$

2) Switching Frequency and On and Off Time Calculations

Given that f_{SW} = 200 kHz and D_{MAX} = 0.80

$$T = \frac{1.0}{f_{SW}} = 5.0\ \mu s$$

$$T_{ON(max)} = T \times D_{MAX} = 5.0\ \mu s \times 0.62 \cong 3.0\ \mu s$$

$$T_{ON(min)} = T \times D_{MIN} = 5.0\ \mu s \times 0.40 \cong 2.0\ \mu s$$

$$T_{OFF(max)} = T_{ON(min)} = 5.0\ \mu s - 2.0\ \mu s = 3.0\ \mu s$$

3) Oscillator Capacitor Selection

The switching frequency is set by C_{OSC}, whose value is given by:

$$C_{OSC}\ \text{in pF} = \frac{95 \times 10^{-6}}{F_{SW}\left(1 + \frac{F_{SW}}{3 \times 10^6} - \left(\frac{30 \times 10^3}{F_{SW}}\right)^2\right)}$$

4) Inductor Selection

The inductor value is chosen for continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUT}min = 2 \times 0.3\ A = 0.6\ A$.

$$L_{min} = \frac{(V_{OUT} + V_D) \times T_{OFF(max)}}{\Delta I} = \frac{5.6\ V \times 3.0\ \mu s}{0.6\ A} = 28\ \mu H$$

This is the minimum value of inductor to keep the ripple current < 0.6 A during normal operation.

A smaller inductor will result in larger ripple current. Ripple current at a minimum off time is

$$\Delta I = \frac{(V_{OUT} + V_F) \times T_{OFF(min)}}{L_{MIN}} = \frac{5.6\ V \times 2.0\ \mu s}{28\ \mu H} = 0.4\ A$$

The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = I_{OUT} + \Delta I/2 = 3.0\ A + 0.4\ A/2 = 3.2\ A$$

5) Output Capacitor

The output capacitor and the inductor form a low pass filter. The output capacitor should have a low ESL and ESR. Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are less expensive. Solid tantalum chip capacitors are available from a number of suppliers and are the best choice for surface mount applications.

The output capacitor limits the output ripple voltage. The CS51031 needs a maximum of 20 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak to peak is given by:

$$C = \frac{\Delta I}{8.0 \times f_{SW} \times \Delta V} = \frac{0.6\ A}{8.0 \times (200 \times 10^3 Hz) \times (50 \times 10^{-3}\ V)} = 7.5 \mu F$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak to peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6\ A} = 83\ m\Omega$$

The output capacitor should be chosen so that its ESR is less than 83 mΩ.

During the minimum off time, the ripple current is 0.4 A and the output voltage ripple will be:

$$\Delta V = ESR \times \Delta I = 83 m\Omega \times 0.4 = 33\ mV$$

6) V_{FB} Divider

$$V_{OUT} = 1.25\ V\left(\frac{R1 + R2}{R2}\right) = 1.25\ V\left(\frac{R1}{R2} + 1.0\right)$$

The input bias current to the comparator is 4.0 µA. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this permits a divider current of 1mA and simplifies the calculations.

$$\frac{5.0\ V}{1.0\ mA} = R1 + R2 = 5.0\ K\Omega$$

Let R2 = 1.0 K

Rearranging the divider equation gives:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1.0\right) = 1.0\ k\Omega\left(\frac{5.0\ V}{1.25} - 1.0\right) = 3.0\ k\Omega$$

7) Divider Bypass Capacitor C_{RR}

Since the feedback resistors divide the output voltage by a factor of 4.0, i.e. 5.0 V/1.25 V= 4.0, it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60 mV (4.0 × 15 mV) to trip the feedback comparator. We use a capacitor C_{RR} to act as an AC short.

The ripple voltage frequency is equal to the switching frequency so we choose C_{RR} = 1.0 nF.

8) Soft Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a delay time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides soft start by clamping the reference voltage during startup, allowing it to rise slowly, and, finally it controls the hiccup short circuit protection circuitry. This reduces the duty cycle to approximately 0.035 during short circuit conditions.

An important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15 V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15 V, the fault timing comparator will discharge CS and the supply will not start. For the V_{FB} voltage to reach 1.15 V the output voltage must be at least 4 × 1.15 = 4.6 V.

If we choose an arbitrary startup time of 900 µs, the value of CS is:

$$t_{Startup} = \frac{CS \times 2.5\ V}{I_{Charge}}$$

$$CS_{min} = \frac{900\ \mu s \times 264\ \mu A}{2.5\ V} = 950\ nF \cong 0.1\ \mu F$$

The fault time is the sum of the slow discharge time the fast discharge time and the recharge time. It is dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$t_{SlowDischarge(t)} = \frac{CS \times (2.4\ V - 1.5\ V)}{I_{Discharge}}$$

where $I_{Discharge}$ is 6.0 μA typical.

$$t_{SlowDischarge(t)} = CS \times 1.5 \times 10^5$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V.

$$t_{FastDischarge(t)} = \frac{CS \times (2.5\ V - 2.4\ V)}{I_{FastDischarge}}$$

where $I_{FastDischarge}$ is 66 μA typical.

$$t_{FastDischarge(t)} = CS \times 1515$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V.

$$t_{Charge(t)} = \frac{CS \times (2.5\ V - 1.5\ V)}{I_{Charge}}$$

where I_{Charge} is 264 μA typical.

$$t_{Charge(t)} = CS \times 3787$$

The fault time is given by:

$$t_{Fault} = CS \times (3787 + 1515 + 1.5 \times 10^5)$$

$$t_{Fault} = CS \times (1.55 \times 10^5)$$

For this circuit

$$t_{Fault} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 15.5\ \mu s$$

A larger value of CS will increase the fault time out time but will also increase the soft start time.

9) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. A low ESR capacitor of at least 100 μF is good. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to filter high frequency noise.

10) MOSFET Selection

The CS51031 drives a P–channel MOSFET. The V_{GATE} pin swings from GND to V_C. The type of PFET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

A PFET with a continuous drain current (I_D) rating greater than the maximum output current is required.

The Gate–to–Source voltage V_{GS} and the Drain–to Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = I_{OUT}^2 \times R_{DS(ON)} \times D$$

where

$R_{DS(ON)}$ is the value at $T_J = 100°C$

The power dissipation of the PFET due to the switching losses is given by:

$$P_D = 0.5 \times V_{IN} \times I_{OUT} \times (t_r) \times f_{SW}$$

where t_r = Rise Time.

11) Diode Selection

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$P_D = I_{OUT} \times V_D \times (1.0 - D_{min})$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
CS51031YD8	–40°C < T_A < 85°C	SO–8	95 Units/Rail
CS51031YDR8	–40°C < T_A < 85°C	SO–8	2500 Tape & Reel
CS51031YN8	–40°C < T_A < 85°C	DIP–8	50 Units/Rail
CS51031GD8	0°C < T_A < 70°C	SO–8	95 Units/Rail
CS51031GDR8	0°C < T_A < 70°C	SO–8	2500 Tape & Reel

PACKAGE THERMAL DATA

Parameter		SO–8	DIP–8	Unit
$R_{\Theta JC}$	Typical	45	52	°C/W
$R_{\Theta JA}$	Typical	165	100	°C/W