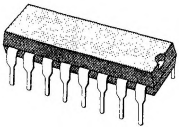
SGS-THOMSON MICROELECTRONICS

MC3479C

STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION + 7.2 V TO + 16 V
- 350 mA/ COIL DRIVE CAPABILITY
- BUILT IN FAST PROTECTION DIODES
- SELECTABLE $\overline{CW}$/CCW AND $\overline{FULL}$/HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS : 250 mV TYP.
- $\overline{PHASE}$ LOGIC CAN BE INITIALIZED TO $\overline{PHASE\ A}$
- $\overline{PHASE\ A}$ OUTPUT DRIVE STATE INDICATION



Powerdip
12 + 2 + 2

ORDER CODE : MC3479C

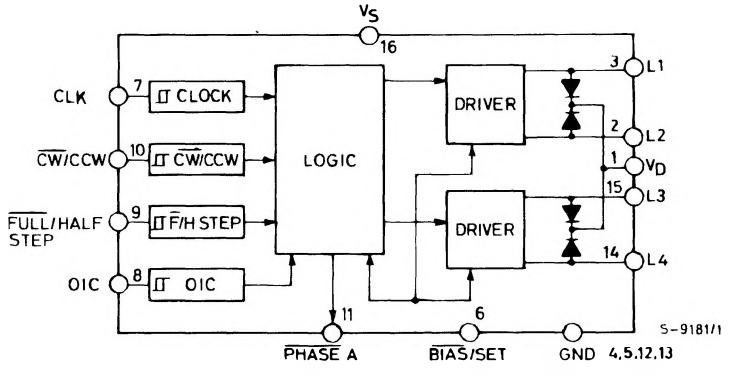
DESCRIPTION

The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.

INPUT TRUTH TABLE

	INPUT LOW	INPUT HIGH
CW/CCW	CW	CCW
F/HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	

BLOCK DIAGRAM



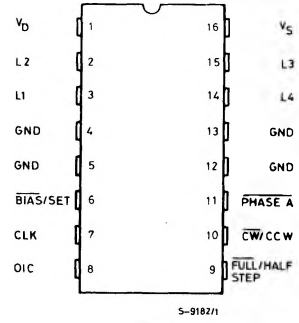
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V_{DC}
V_D	Clamp Diode Cathode Voltage (pin 1)	V_S	V_{DC}
V_{OD}	Driver Output Voltage (pins 2, 3, 14, 15)	V_S	V_{DC}
I_{OD-}	Driver Output Current/Coil	± 500	mA
V_{IN}	Input Voltage (pins 7, 8, 9, 10)	– 0.5 to 7	V_{DC}
I_{BS}	Bias/Set Current (pin 6)	10	mA
V_{OA}	Phase A Output Voltage (pin 11)	16	V_{DC}
I_{OA}	Phase A Sink Current (pin 11)	20	mA
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature range	– 55 to 150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage (DC)	7.2	16	V
V_D	Clamp Diode Cathode Voltage (DC)	–	V_S	V
I_{OD}	Driver Output Current (per coil)	–	350	mA
V_I	DC Input Voltage (pin 7, 8, 9, 10)	0	5.5	V
I_{BS}	Bias/Set Current (outputs active)	– 300	75	µA
I_{OA}	Phase A Sink Current	0	8	mA
T_{amb}	Operating Ambient Temperature	0	70	°C

CONNECTION DIAGRAMS



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

PIN DESCRIPTION

Symbol	Name	Pins	Description
V_S	POWER SUPPLY	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2 V to 16 V.
GND	GROUND	4-5-12-13	Ground Pins for the Logic Circuit and the Motor Coil Current. The physical configuration of the pins dissipating heat from within the package.
V_D	CLAMP DIODE	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and pin 16. See figure 5.
L1, L2, L3, L4	DRIVER OUTPUTS	2-3 14-15	High Current Outputs for the Motor Coils. L1 and L2 are connected to one coil and L3 and L4 to the other coil.
$\overline{B/S}$	$\overline{BIAS/SET}$	6	This pins is typically 0.7 V below V_S. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CK	CLOCK	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if pin 6 is open.
$\overline{F/HS}$	$\overline{FULL/HALF\ STEP}$	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. (see figure 4 for sequence).
$\overline{CW/CCW}$	$\overline{CLOCKWISE}$ COUNTERCLOCKWISE	10	This input allows reversing the rotation of the rotation of the motor. (see figure 4 for sequence).
OIC	OUT IMPEDANCE CONTROL	8	This input is relevant only in the half step mode (pin 9 > 2 V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S. (see figure 4).
$\overline{Ph\ A}$	$\overline{PHASE\ A}$	11	This outputs indicate (when low) that the driver outputs are in the phase A condition (L1 = L3 = V_{OHD} ; L2 = L4 = V_{OLD}).

DC ELECTRICAL CHARACTERISTICS(Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT LOGIC LEVEL						
V_{TLH}	Threshold Voltage (low to high)				2	V
V_{THL}	Threshold Voltage (high to low)		0.8			V
V_{HYS}	Hysteresis		0.4			V
I_{IL} I_{IH1} I_{IH2}	Current	V_I = 0.4 V V_I = 5.5 V V_I = 2.7 V	– 100		 100 20	 µA
DRIVER OUTPUT LEVELS						
V_{OHD}	Output High Voltage	I_{OD} = – 350 mA I_{OD} = – 0.1 mA I_{BS} = – 300 µA	V_S – 2.0 V_S – 1.2			V V
V_{OLD}	Output Low Voltage	I_{BS} = – 300 µA I_{OD} = – 350 mA			0.8	V
D_{VOD}	Difference Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = 350 mA			0.15	V
C_{VOD}	Common Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = – 0.1 mA			0.15	V
I_{OZ1}	Out Leakage-HiZ State	0 < V_D < V_M, I_{BS} = 5 µA	– 100		+ 100	µA
I_{OZ2}	Out Leakage-HiZ state	0 < V_{OD} < V_M, I_{BS} = – 300 µA Pin 9 = 2 V Pin 8 = 0.8 V	– 100		+ 100	µA
CLAMP DIODES						
V_{DF}	Forward Voltage	I_D = 350 mA		2.5	3	V
I_{DR}	Leakage Current	V_R = 21 V			100	µA
PHASE A OUTPUT						
V_{OLA}	Out Low Voltage	I_{OA} = 8 mA			0.4	V
	Off State Leakage Current	V_{OA} = 16.5 V			100	µA
POWER SUPPLY						
I_{SSB}	Power Supply Current in Stand by State	V_{BS} = V_S			12	mA
I_S	Power Supply Current (I_{OD} = 0) ; I_{BS} = – 300 µA)	L1 = V_{OHD} L2 = V_{OLD} L3 = V_{OHD} L4 = V_{OHD}			75	mA

BIAS SET CURRENT

I_{BS}	Bias Set Current	to set $\overline{\text{PHASE A}}$	– 5			µA

Notes : 3. DVOD = | VOD1.2 - VOD3.4 |
VOD1.2 = (VOHD1 - VOHD2) or (VOHD2 - VOLD1) AND VOD3.4 = (VOHD3 - VOHD4) OR (VOHD4 - VOHD3)
4. CVOD = | VOHD1 - VOHD2 or VOHD3 - VOHD4 |

AC SWITCHING CHARACTERISTICS (T_{amb} = 25 °C ; V_M = 12 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CK}	Clock Frequency		0		30	KHz
PWCKH	Clock Pulse Width	HIGH	10			µs
PWCKL	Clock Pulse Width	LOW	20			µs
t_{SU}	Set-up Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		5			µs
t_{HO}	Hold Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		10			µs
t_{PCD}	Propagation Delay CLK-to Driver Out			8		µs
t_{PBSD}	Propagation Delay $\overline{\text{Bias}}$/Set to Driver Output			1		µs
t_{PHLA}	Propagation Delay CLK-to Phase A LOW			12		µs
t_{PLHA}	Propagation Delay CLK-to Phase A HIGH			5		µs

Figure 1: AC Test Circuit.

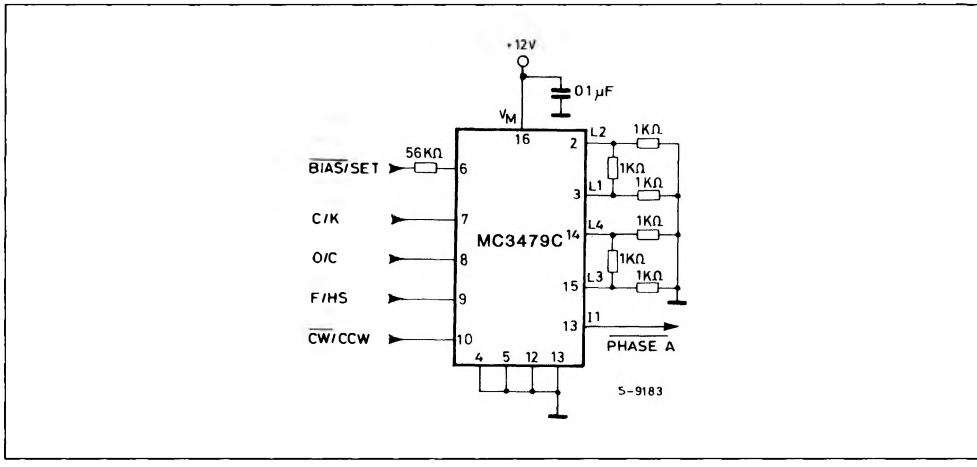


Figure 2 : Typical Application Circuit.

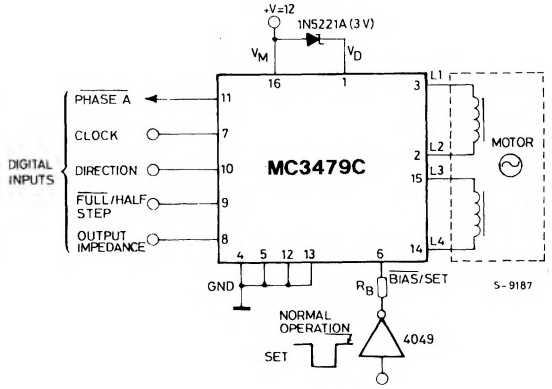


Figure 3 : Bias/Set Timing (refer to fig.1).

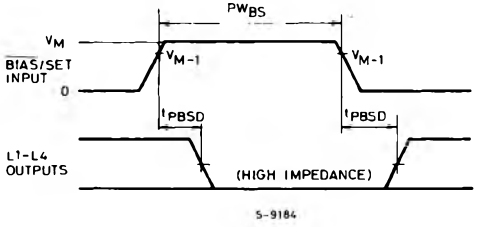


Figure 4 : Clock Timing (refer to fig.1).

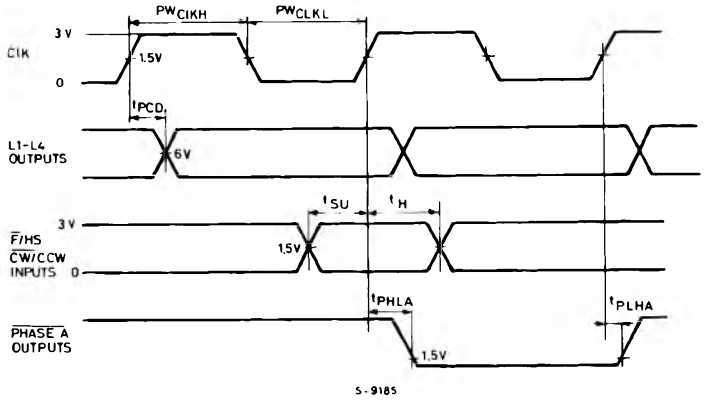


Figure 5 : Output Sequence.