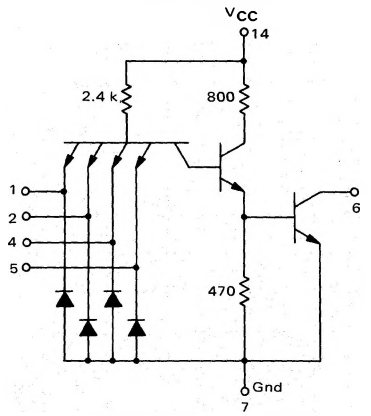
DUAL 4-INPUT "NAND" GATE
(Open Collector)

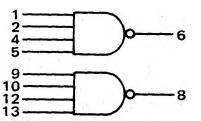
MC3112F • MC3012F
MC3112L • MC3012L,P

(54H22J) (74H22J,N)

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.



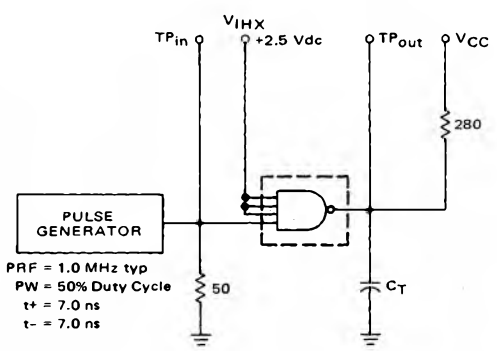
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

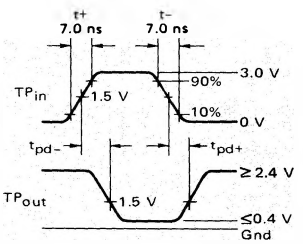
Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

Pin numbers for the 54H22F/74H22F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3112F,L/3012F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H22F/74H22F	1	12	3	13	14	2	11	10	6	7	14	8	9	4

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



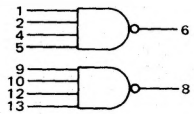


C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3112 Test Limits −55°C Min	MC3112 Test Limits −55°C Max	MC3112 Test Limits +25°C Min	MC3112 Test Limits +25°C Max	MC3112 Test Limits +125°C Min	MC3112 Test Limits +125°C Max	MC3012 Test Limits 0°C Min	MC3012 Test Limits 0°C Max	MC3012 Test Limits +25°C Min	MC3012 Test Limits +25°C Max	MC3012 Test Limits +75°C Min	MC3012 Test Limits +75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{in} (mA)	I_D (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{CEX} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{IHX} (Volts)	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	-	7*
Output Leakage Current	I_{CEX}	-	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	1	2,4,5	-	-	-	6	-	-	14	-	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12.5	-	-	-	-	-	12.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	20	-	20	-	20	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	-	-	-	14	-	7
	I_{PDL}	14	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	-	5.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	14	-	-	-	-	-	14	-	-	ns	Pulse In: 1	Pulse Out: 6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	6	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CEX}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3112	−55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5
	+125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-
MC3012	0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-
	+25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5
	+75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.