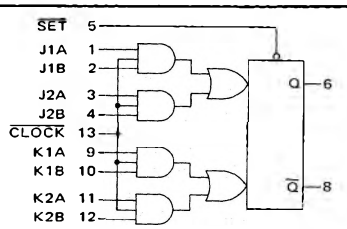
"OR" INPUT
J-K FLIP-FLOP

MC3154F • MC3054F
MC3154L • MC3054L, P
(54H71J) (74H71J, N)



t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

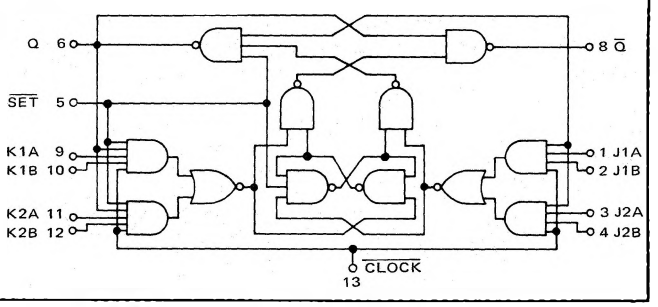
$J = J1A \cdot J1B + J2A \cdot J2B$
$K = K1A \cdot K1B + K2A \cdot K2B$

Input Loading Factor:
J, K = 1
CLOCK = 2
SET = 3

Output Loading Factor = 10

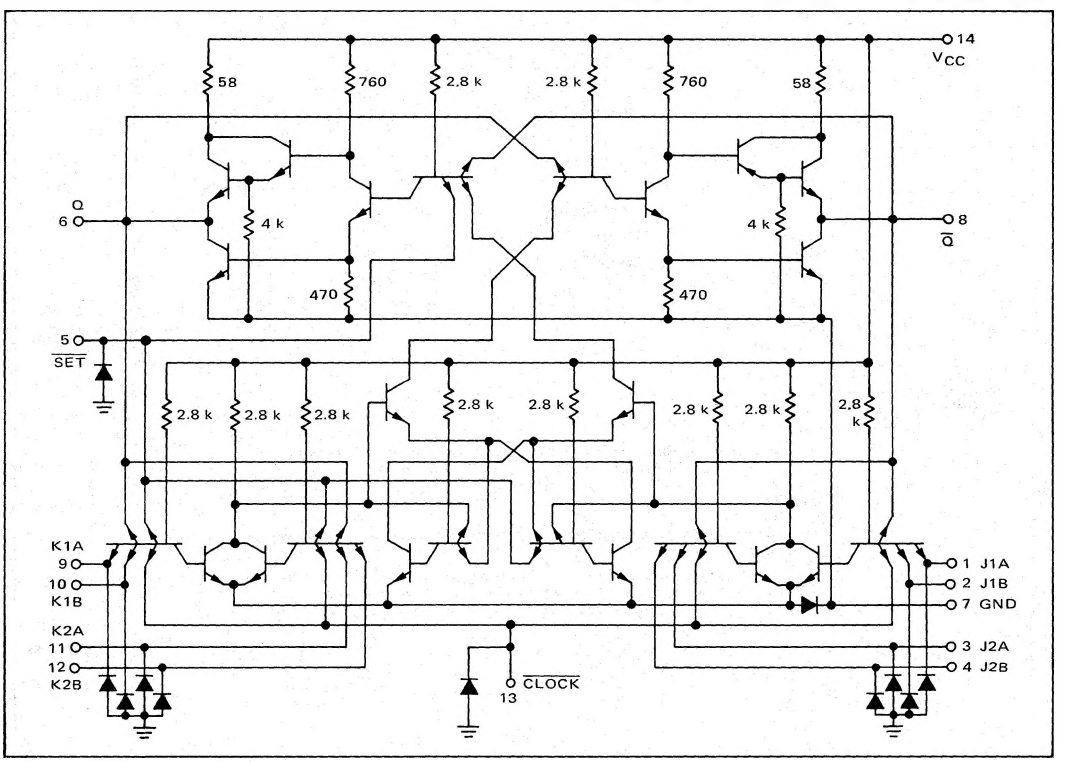
Total Power Dissipation = 95 mW typ/pkg
Propagation Delay Time = 20 ns typ
Operating Frequency = 30 MHz typ

This negative-edge clocked J-K Flip-Flop operates on the master-slave principle. AND-OR gate inputs enter data into the master section on the positive edge of the clock. This data is transferred to the slave section of the Flip-Flop on the negative edge of the clock. In order to assure entry of information into the Flip-Flop, data must not change after the positive edge of the clock.



Pin numbers for the 54H71F/74H71F device are shown in the chart. These devices are available on special request.

DEVICE	PIN NUMBERS													
MC3154F,L/3054F,L,P	1	2	3	4	5	6	7	8	9	10	11	12	13	14
54H71F/74H71F	5	6	7	8	9	10	11	12	1	2	13	14	3	4



See General Information section for packaging.

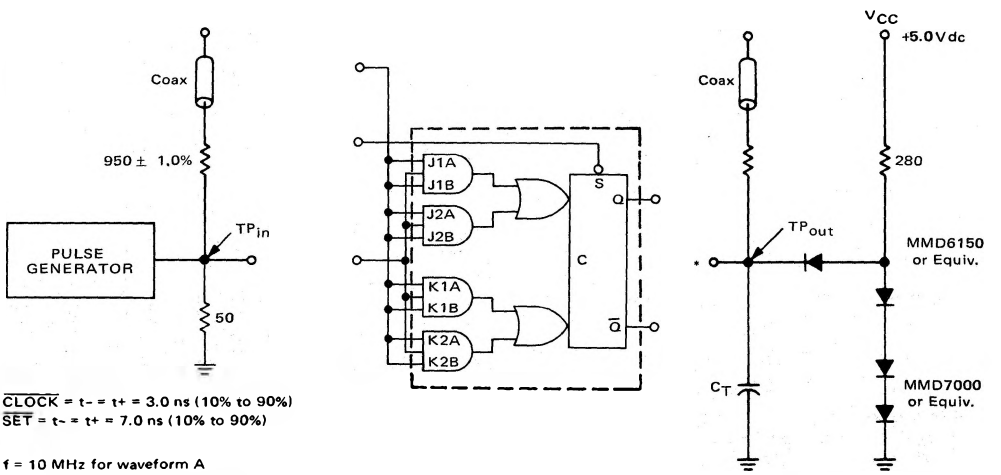
OPERATING CHARACTERISTICS

Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{SET}$ input will force the Q output to the logic "1" state. The $\overline{SET}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 12 ns minimum.

SWITCHING TIME TEST CIRCUIT



$\overline{CLOCK}$ = t- = t+ = 3.0 ns (10% to 90%)
$\overline{SET}$ = t- = t+ = 7.0 ns (10% to 90%)

f = 10 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{SET}$. Only one pulse generator is required for J, K, and $\overline{CLOCK}$ tests.

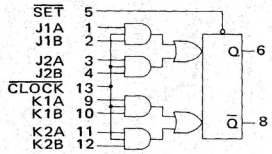
*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input on each AND gate, plus the SET and CLOCK inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
	mA			Volts							
	I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	
MC3154	20	-1.5	1.0	0.4	2.4	4.5	2.0	0.8	4.5	5.5	
MC3054	20	-1.5	1.0	0.4	2.4	4.5	2.0	0.8	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC3154 Test Limits −55 to +125°C Min	Max	Unit	MC3054 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_F	V_R	V_{RH}	V_{IH}	V_{IL}	V_{CCL}	V_{CCH}	P_A**	Gnd
Input																				
Forward Current J1A	I_F	1	-	-2.0	mAdc	-	-2.0	mAdc	-	-	-	1	-	2,13	-	-	-	14	-	7,6
K1A		11	-	-2.0	↓	-	-2.0	↓	-	-	-	11	-	5**,12,13	-	-	-	↓	-	7
Set		5	-	-6.0		-	-6.0		-	-	-	5	-	1,2,3,4,9,10,11,12,13	-	-	-		-	7
Clock		13	-	-4.0		-	-4.0		-	-	-	13	-	1,2,3,4,5**,9,10,11,12	-	-	-		-	7
Clock		13	-	-4.0	↓	-	-4.0	↓	-	-	-	13	-	1,2,3,4,5,9,10,11,12	-	-	-	↓	-	7,6
Leakage Current J1A	I_{R1}	1	-	50	μAdc	-	50	μAdc	-	-	-	-	1	-	-	-	-	14	-	2,5,7,13
K1A		11	-	50	↓	-	50	↓	-	-	-	-	11	-	-	-	-	↓	-	5,6,7,12,13
Set		5	-	150		-	150		-	-	-	-	5	-	-	-	-		-	6,7,9,10,11,12,13
Clock		13	-	100		-	100		-	-	-	-	13	-	-	-	-		-	1,2,3,4,5,7,9,10,11,12
Clock		13	-	100	↓	-	100	↓	-	-	-	-	13	-	-	-	-	↓	-	1,2,3,4,5,6,7,9,10,11,12
J1A	BV_{in}	1	5.5*	-	Vdc	5.5*	-	Vdc	-	-	1	-	-	-	-	-	-	14	-	2,5,7,13
K1A		11	↓	-	↓	↓	-	↓	-	-	11	-	-	-	-	-	-	↓	-	5,6,7,12,13
Set		5		-			-		-	-	5	-	-	-	-	-	-		-	6,7,9,10,11,12,13
Clock		13		-			-		-	-	13	-	-	-	-	-	-			1,2,3,4,5,7,9,10,11,12
Clock		13	↓	-	↓	↓	-	↓	-	-	13	-	-	-	-	-	-	↓		1,2,3,4,5,6,7,9,10,11,12
Output																				
Output Voltage	V_{OL}	8	-	0.4	Vdc	-	0.4	Vdc	8	-	-	-	-	-	-	5	14	-	-	7,13
		6	-	0.4	Vdc	-	0.4	Vdc	6	-	-	-	-	-	9,10,11,12	1,2,3,4	14	-	13	7
	V_{OH}	6	2.4	-	Vdc	2.4	-	Vdc	-	6	-	-	-	-	-	5	14	-	-	7,13
		8	2.4	-	Vdc	2.4	-	Vdc	-	8	-	-	-	-	9,10,11,12	1,2,3,4	14	-	13	7
Short-Circuit Current	I_{SC}	6	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,2,3,4,9,10,11,12,13	-	-	-	14	-	5,6,7
		8	-40	-100	mAdc	-40	-100	mAdc	-	-	-	-	-	1,2,3,4,5,9,10,11,12,13	-	-	-	14	-	6,7,8†
Power Requirements																				
Power Supply Drain	I_{PD}	14	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,3,4,5,7,9,10,11,12,13
		14	-	30	mAdc	-	30	mAdc	-	-	-	-	-	1,2,3,4,5,9,10,11,12	-	-	-	14	-	7,13††

*Tested at 25°C only.

**Momentarily ground pin prior to taking measurement, then apply 4.5 volts. P_A = 4.5 V / 0 V

† Limit duration of test to 100 ns.

†† Momentary 4.5 V then apply gnd.

TEST PROCEDURES

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT			Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{S}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	A	2.4 V	2.4 V	†	†	25	–	MHz
Turn-On Delay	t_{pd-}	B	B	2.4 V	C	C	–	27	ns
Turn-Off Delay	t_{pd+}	B	B	2.4 V	D	D	–	21	ns
Turn-On Delay	t_{sd-}	E	2.4 V	F	G	H	–	24	ns
Turn-Off Delay	t_{sd+}	E	2.4 V	F	G	H	–	13	ns

†Output shall toggle with each input pulse.

VOLTAGE WAVEFORMS AND DEFINITIONS