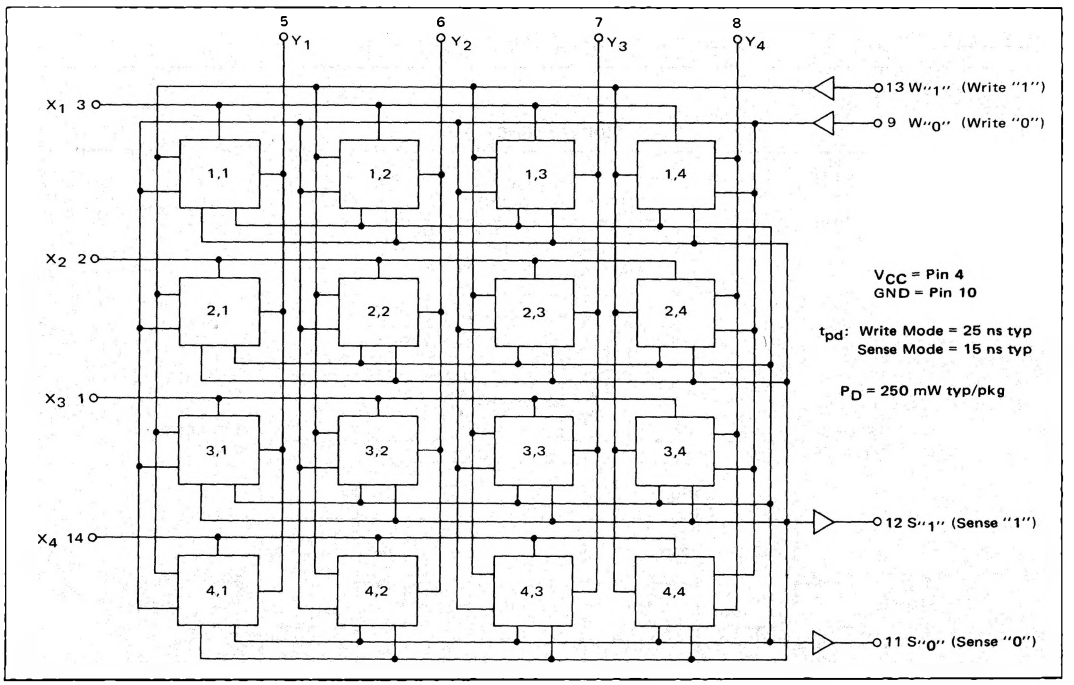
MC4304F,L • MC4305F,L*
MC4004F,L,P • MC4005F,L,P*

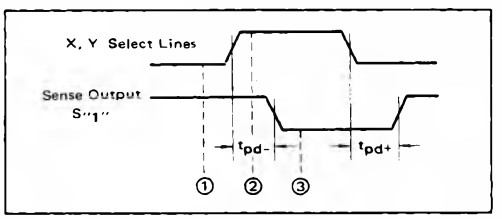
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM



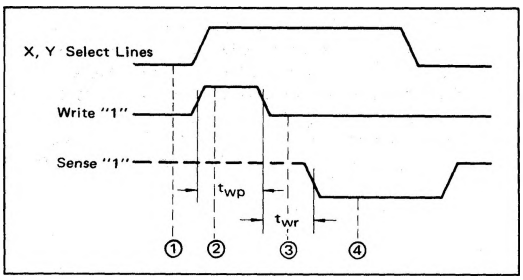
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

FIGURE 2 – WRITE MODE TIMING DIAGRAM



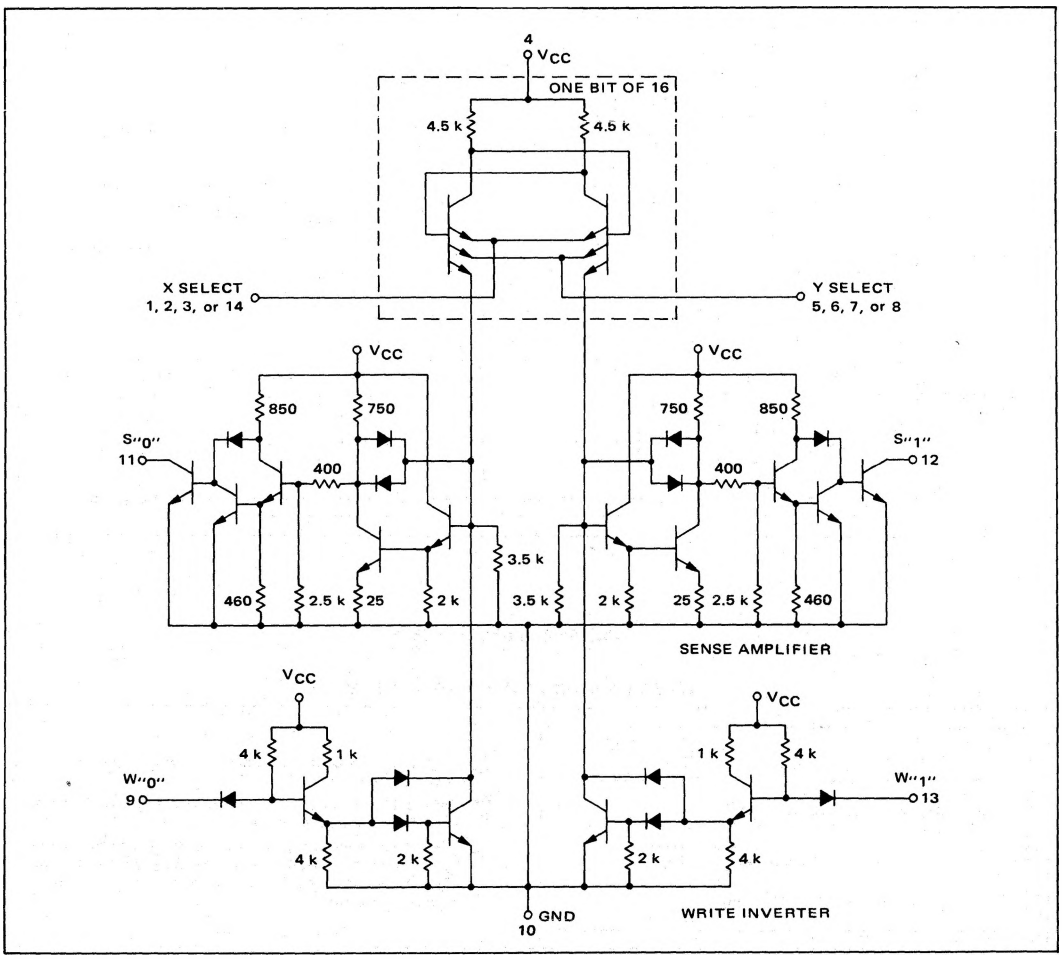
① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

④ The stored bit can be read after the write recovery time (t_{wr}) of 40 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one bit.
Other bits are tested in the same manner.

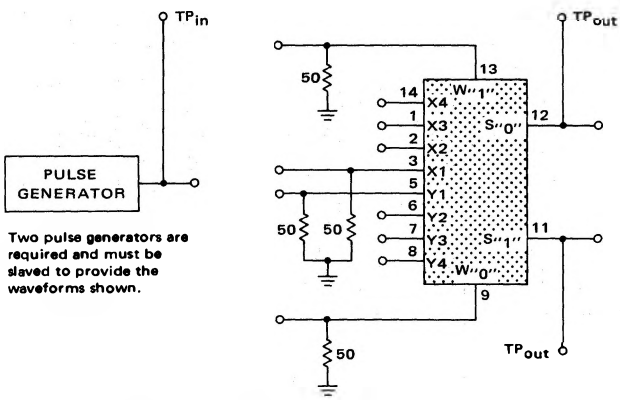
@ Test Temperature		$I_{s"0"}$ Pr* (mA)	$I_{s"0"}$ Std (mA)	I_W (mA)	I_{XY} (mA)	$V_{in\,1}$ (Volts)	$V_{in\,2}$ (Volts)	$V_{in\,3}$ (Volts)	V_F (Volts)	V_R (Volts)	V_{th} (Volts)	V_{out} (Volts)	V_{CC} (Volts)	BV_{ckt} (Volts)
MC4304*, MC4305	−55°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-
	+25°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	7.0
	+125°C	40	20	1.0	3.0	0.75	0.85	0.9	0	4.5	2.2	5.5	5.0	-
MC4004*, MC4005	0°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-
	+25°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	7.0
	+75°C	40	20	1.0	3.0	0.8	1.0	1.0	0	4.5	2.1	5.5	5.0	-

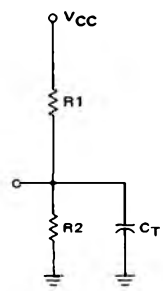
Characteristic	Symbol	Pin Under Test	MC4304, MC4305 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4004, MC4005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{s"0"}$	I_W	I_{XY}	$V_{in\,1}$	$V_{in\,2}$	$V_{in\,3}$	V_F	V_R	V_{th}	V_{out}	V_{CC}	BV_{ckt}	Gnd
Input																												
Forward Current Address Lines	I_F	3	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	3	5,6,7,8	-	-	4	-	1,2,9,10,13,14
		5	-	-11	-	-11	-	-11	-	-13.5	-	-13.5	-	-13.5	mAdc	-	-	-	-	-	-	5	1,2,3,14	-	-	4	-	6,7,8,9,10,13
Write Inputs		9	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	9	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	13	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Leakage Current Address Lines	I_R	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	3	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	mAdc	-	-	-	-	-	-	-	5	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	9	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	-	0.1	mAdc	-	-	-	-	-	-	-	13	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Breakdown Voltage Address Lines	BV_{in}	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	3	-	-	-	-	-	-	-	4	-	1,2,5,6,7,8,9,10,13,14
		5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	-	4	-	1,2,3,6,7,8,9,10,13,14
Write Inputs		9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	9	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,10,13,14
		13	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	13	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Output (Note 1)																												
Output Voltage Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	13	9	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1" Inhibit	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3,5	-	-	9	13	-	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Logic "0" Level	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	3,5	-	4	-	1,2,6,7,8,9,10,13,14
Leakage Current Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	-	-	3,5,13	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	12	4	-	1,2,6,7,8,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	-	-	3,5,9	-	4	-	1,2,6,7,8,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	3,5	-	-	-	-	11	4	-	1,2,6,7,9,10,13,14
Write "1"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	13	3,5,6,7,8	-	4	-	1,2,9,10,14
Leakage Current	I_{OLK}	11	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	11	4	-	1,2,9,10,13,14
Write "0"	**	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	9	3,5,6,7,8	-	4	-	1,2,10,13,14
Leakage Current	I_{OLK}	12	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	mAdc	-	-	-	-	-	-	-	-	3,5,6,7,8	-	4	-	1,2,9,10,13,14
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	4	-	65	-	65	-	65	-	72	-	72	-	72	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,13,14
Power Supply Breakdown Current	I_{ckt}	4	-	-	-	95	-	-	-	-	-	105	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14

*Prime Fan-Out

Note 1. Output logic "0" voltage and leakage current measurements are made as part of a functional test of a memory. Procedures identified by a double asterisk (**) are preconditioning procedures for the subsequent test. All power supply and input voltages must be maintained between tests.

SWITCHING TIME TEST CIRCUIT

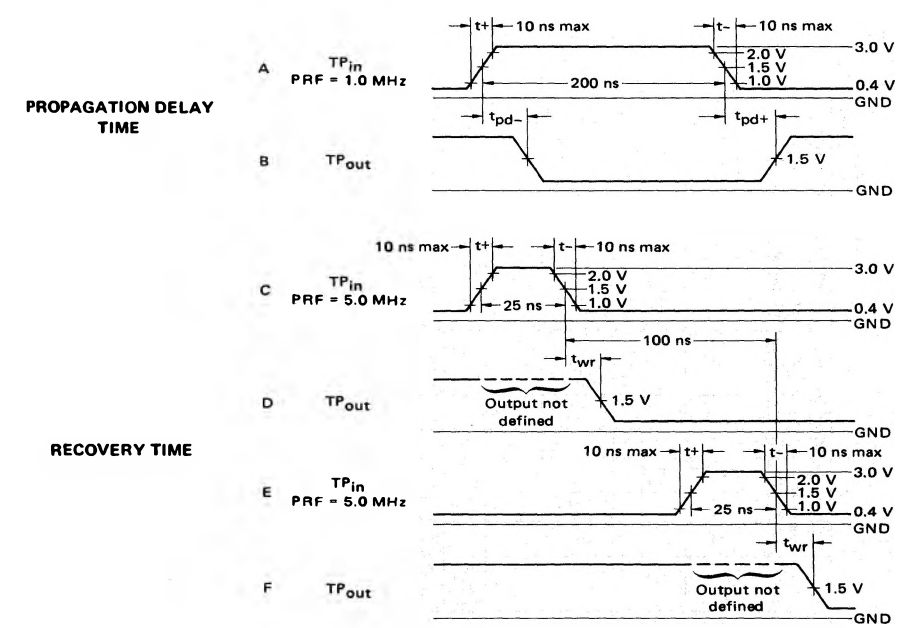




DEVICE UNDER TEST	R1 OHMS	R2 OHMS
MC4304, MC4004	120	330
MC4305, MC4005	240	560

See Switching Time Test Procedures table for value of C_T.

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIME TEST PROCEDURES

(Letters shown in test columns refer to waveforms)

Test	Symbol	Pin Under Test	Input Pin										Output		C_T* pF	Limits	
			3 X_1	2 X_2	1 X_3	14 X_4	5 Y_1	6 Y_2	7 Y_3	8 Y_4	9 W"0"	13 W"1"	11 S"0"	12 S"1"		MC4304-5 ns max	MC4004-5 ns max
Turn-Off Delay Time (Address Lines to Sense "0" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-Off Delay Time (Address Lines to Sense "1" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-On Delay Time (Address Lines to Sense "0" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	–	–	–	–	–
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	30	23	23
	t_{pd-}	11	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	B	–	200	35	35
Turn-On Delay Time (Address Lines to Sense "1" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	Gnd	3.0 V	–	–	–	–	–
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	30	23	23
	t_{pd-}	12	A	Gnd	Gnd	Gnd	A	Gnd	Gnd	Gnd	Gnd	Gnd	–	B	200	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "0" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	t_{pd+}	11	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	B	–	30	35	35
Turn-Off Delay Time (4 Bits) (Address Lines to Sense "1" Output)	••	–	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	–	–	–	–	–
	••	–	3.0 V	Gnd	Gnd	Gnd	3.0 V	3.0 V	3.0 V	3.0 V	Gnd	3.0 V	–	–	–	–	–
	t_{pd+}	12	A	Gnd	Gnd	Gnd	A	A	A	A	Gnd	Gnd	–	B	30	35	35
Write Recovery Time	t_{wr}	12	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	–	D	30	40	40
		11	3.0 V	Gnd	Gnd	Gnd	3.0 V	Gnd	Gnd	Gnd	E	C	F	–	30	40	40
																ns min	ns min
Write Pulse Width	t_{wp}	–	Tested during t_{wr} tests.													25	25

*Capacitance value for load of the Switching Time Test Circuit

**Preconditioning procedures for subsequent test.